



512Kx32 3.3V SRAM MODULE PRELIMINARY*

FEATURES

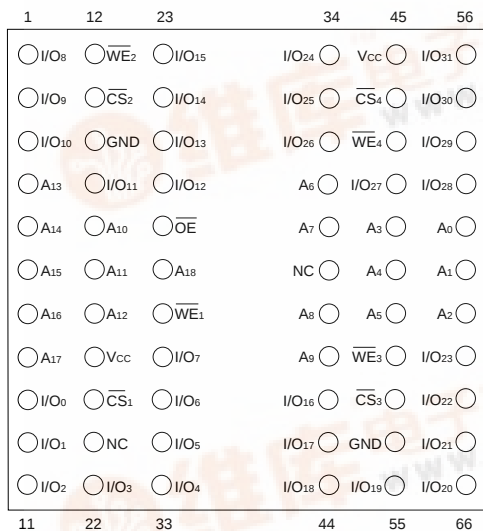
- Access Times of 15[†], 17, 20ns
- MIL-STD-883 Compliant Devices Available
- Low Voltage Operation
- Packaging
 - 66-pin, PGA Type, 1.385 inch square Hermetic Ceramic HIP (Package 402)
 - 68 lead, Hermetic CQFP (G2), 22mm (0.880 inch) square (Package 500). Designed to fit JEDEC 68 lead 0.990" CQFPJ footprint
- Organized as 512Kx32; User Configurable as 1Mx16 or 2Mx8
- Radiation Tolerant with Epitaxial Layer Die
- Commercial, Industrial and Military Temperature Ranges
- 3.3 Volt Power Supply
- BiCMOS
- TTL Compatible Inputs and Outputs
- Built-in Decoupling Caps and Multiple Ground Pins for Low Noise Operation
- Weight
 - WS512K32BV-XG2XE - 8 grams typical
 - WS512K32NBV-XH2XE - 13 grams typical

* This data sheet describes a product under development, not fully characterized, and is subject to change without notice.

† This speed is Advanced information.

PIN CONFIGURATION FOR WS512K32NBV-XH2XE

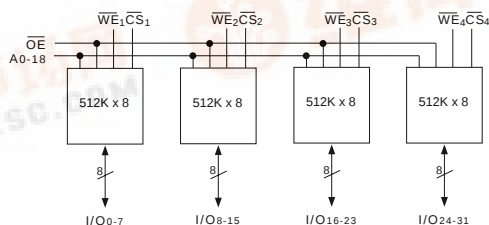
TOP VIEW



PIN DESCRIPTION

I/O ₀₋₃₁	Data Inputs/Outputs
A ₀₋₁₈	Address Inputs
$\overline{\text{WE}}_{1-4}$	Write Enables
$\overline{\text{CS}}_{1-4}$	Chip Selects
$\overline{\text{OE}}$	Output Enable
V _{CC}	Power Supply
GND	Ground
NC	Not Connected

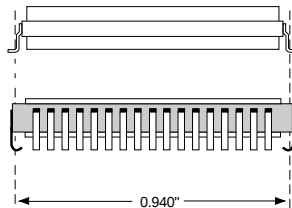
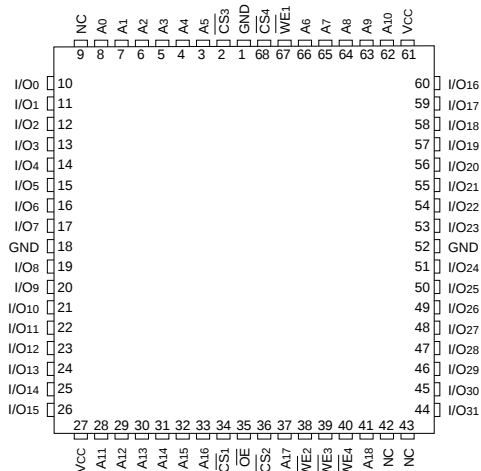
BLOCK DIAGRAM





PIN CONFIGURATION FOR WS512K32BV-XG2XE

TOP VIEW

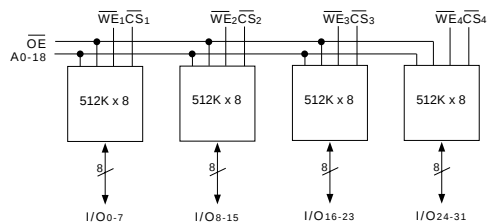


The White 68 lead G2 CQFP fills the same fit and function as the JEDEC 68 lead CQFJ or 68 PLCC. But the G2 has the TCE and lead inspection advantage of the CQFP form.

PIN DESCRIPTION

I/O ₀ -31	Data Inputs/Outputs
A ₀ -18	Address Inputs
$\overline{WE}_1$ -4	Write Enables
$\overline{CS}_1$ -4	Chip Selects
$\overline{OE}$	Output Enable
Vcc	Power Supply
GND	Ground
NC	Not Connected

BLOCK DIAGRAM



**ABSOLUTE MAXIMUM RATINGS**

Parameter	Symbol	Min	Max	Unit
Operating Temperature	T _A	-55	+125	°C
Storage Temperature	T _{STG}	-65	+150	°C
Signal Voltage Relative to GND	V _G	-0.5	4.6	V
Junction Temperature	T _J		150	°C
Supply Voltage	V _{CC}	-0.5	4.6	V

RECOMMENDED OPERATING CONDITIONS

Parameter	Symbol	Min	Max	Unit
Supply Voltage	V _{CC}	3.0	3.6	V
Input High Voltage	V _{IH}	2.2	V _{CC} + 0.3	V
Input Low Voltage	V _{IL}	-0.3	+0.8	V

TRUTH TABLE

$\overline{\text{CS}}$	$\overline{\text{OE}}$	$\overline{\text{WE}}$	Mode	Data I/O	Power
H	X	X	Standby	High Z	Standby
L	L	H	Read	Data Out	Active
L	X	L	Write	Data In	Active
L	H	H	Out Disable	High Z	Active

CAPACITANCE(T_A = +25°C)

Parameter	Symbol	Conditions	Max	Unit
$\overline{\text{OE}}$ capacitance	C _{OE}	V _{IN} = 0 V, f = 1.0 MHz	50	pF
$\overline{\text{WE}}$ ₁₋₄ capacitance HIP (PGA) CQFP G2	C _{WE}	V _{IN} = 0 V, f = 1.0 MHz	20 20	pF
$\overline{\text{CS}}$ ₁₋₄ capacitance	C _{CS}	V _{IN} = 0 V, f = 1.0 MHz	20	pF
Data I/O capacitance	C _{I/O}	V _{I/O} = 0 V, f = 1.0 MHz	20	pF
Address input capacitance	C _{AD}	V _{IN} = 0 V, f = 1.0 MHz	50	pF

This parameter is guaranteed by design but not tested.

DC CHARACTERISTICS(V_{CC} = 3.3V ± 0.3V, V_{SS} = 0V, T_A = -55°C to +125°C)

Parameter	Sym	Conditions	Min	Max	Units
Input Leakage Current	I _{LI}	V _{IN} = GND to V _{CC}		10	μA
Output Leakage Current	I _{LO}	$\overline{\text{CS}}$ = V _{IH} , $\overline{\text{OE}}$ = V _{IH} , V _{OUT} = GND to V _{CC}		10	μA
Operating Supply Current (x 32 Mode)	I _{CC} x 32	$\overline{\text{CS}}$ = V _{IL} , $\overline{\text{OE}}$ = V _{IH} , f = 5MHz, V _{CC} = 3.6V		480	mA
Standby Current	I _{SB}	$\overline{\text{CS}}$ = V _{IH} , $\overline{\text{OE}}$ = V _{IH} , f = 5MHz, V _{CC} = 3.6V		110	mA
Output Low Voltage	V _{OL}	I _{OL} = 8mA		0.4	V
Output High Voltage	V _{OH}	I _{OH} = -4.0mA	2.4		V

NOTE: DC test conditions: V_{IH} = V_{CC} - 0.3V, V_{IL} = 0.3V

**AC CHARACTERISTICS**
($V_{CC} = 3.3V$, $T_A = -55^{\circ}C$ to $+125^{\circ}C$)

Parameter	Symbol	-15*		-17		-20		Units
		Min	Max	Min	Max	Min	Max	
Read Cycle								
Read Cycle Time	t_{RC}	15		17		20		ns
Address Access Time	t_{AA}		15		17		20	ns
Output Hold from Address Change	t_{OH}	0		0		0		ns
Chip Select Access Time	t_{ACS}		15		17		20	ns
Output Enable to Output Valid	t_{OE}		7		8		10	ns
Chip Select to Output in Low Z	t_{CLZ}^1	2		2		2		ns
Output Enable to Output in Low Z	t_{OLZ}^1	0		0		0		ns
Chip Disable to Output in High Z	t_{CHZ}^1		7		8		10	ns
Output Disable to Output in High Z	t_{OHZ}^1		7		8		10	ns

1. This parameter is guaranteed by design but not tested.

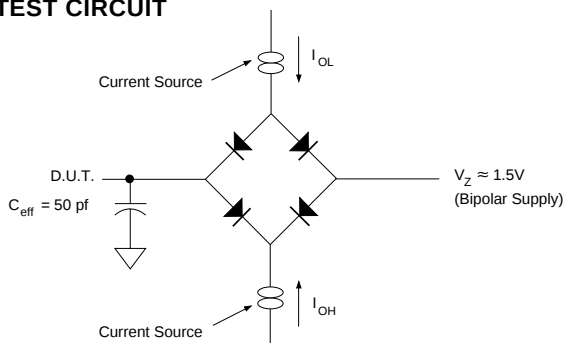
* Advanced information.

AC CHARACTERISTICS
($V_{CC} = 3.3V$, $T_A = -55^{\circ}C$ to $+125^{\circ}C$)

Parameter	Symbol	-15*		-17		-20		Units
		Min	Max	Min	Max	Min	Max	
Write Cycle								
Write Cycle Time	t_{WC}	15		17		20		ns
Chip Select to End of Write	t_{CW}	10		12		14		ns
Address Valid to End of Write	t_{AW}	10		12		14		ns
Data Valid to End of Write	t_{DW}	8		9		10		ns
Write Pulse Width	t_{WP}	12		14		14		ns
Address Setup Time	t_{AS}	0		0		0		ns
Address Hold Time	t_{AH}	0		0		0		ns
Output Active from End of Write	t_{OW}^1	2		3		3		ns
Write Enable to Output in High Z	t_{WHZ}^1		8		8		9	ns
Data Hold Time	t_{DH}	0		0		0		ns

1. This parameter is guaranteed by design but not tested.

* Advanced information.

AC TEST CIRCUIT**AC TEST CONDITIONS**

Parameter	Typ	Unit
Input Pulse Levels	$V_{IL} = 0$, $V_{IH} = 2.5$	V
Input Rise and Fall	5	ns
Input and Output Reference Level	1.5	V
Output Timing Reference Level	1.5	V

NOTES:

V_Z is programmable from -2V to +7V.

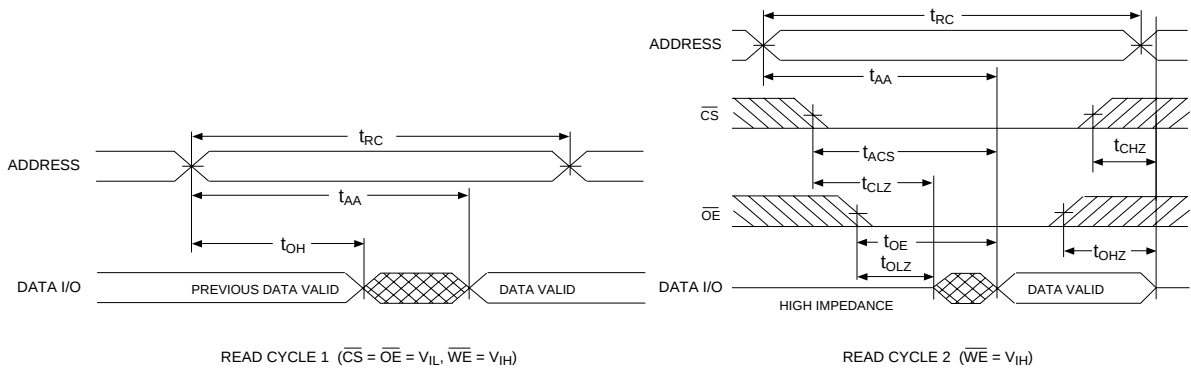
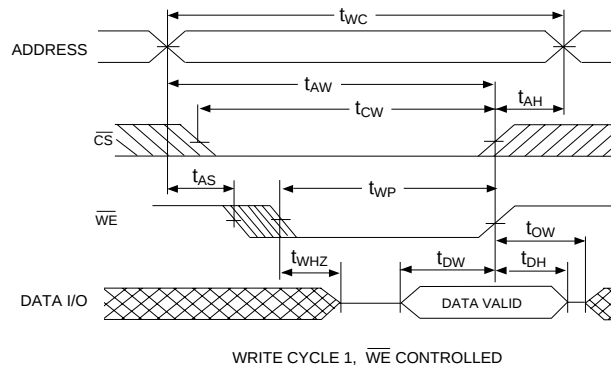
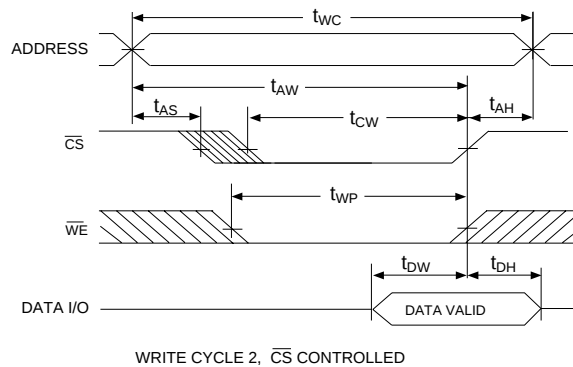
I_{OL} & I_{OH} programmable from 0 to 16mA.

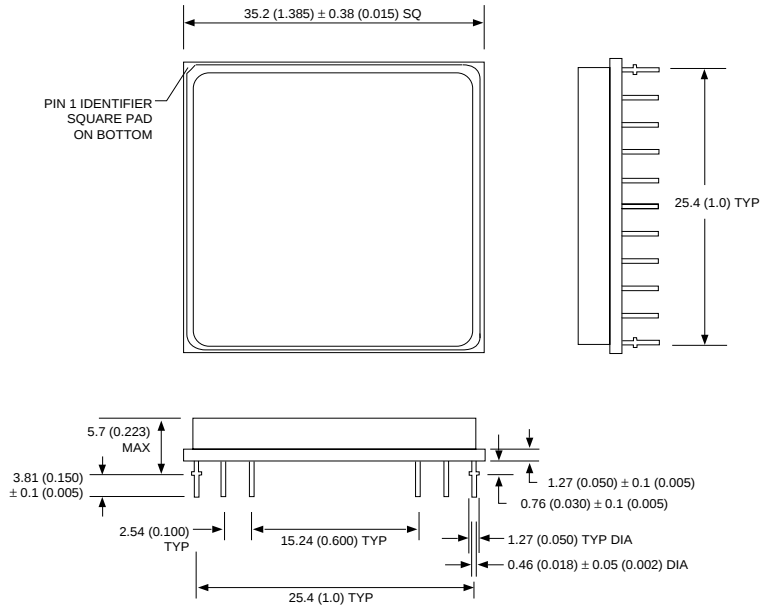
Tester Impedance $Z_0 = 75 \Omega$.

V_Z is typically the midpoint of V_{OH} and V_{OL} .

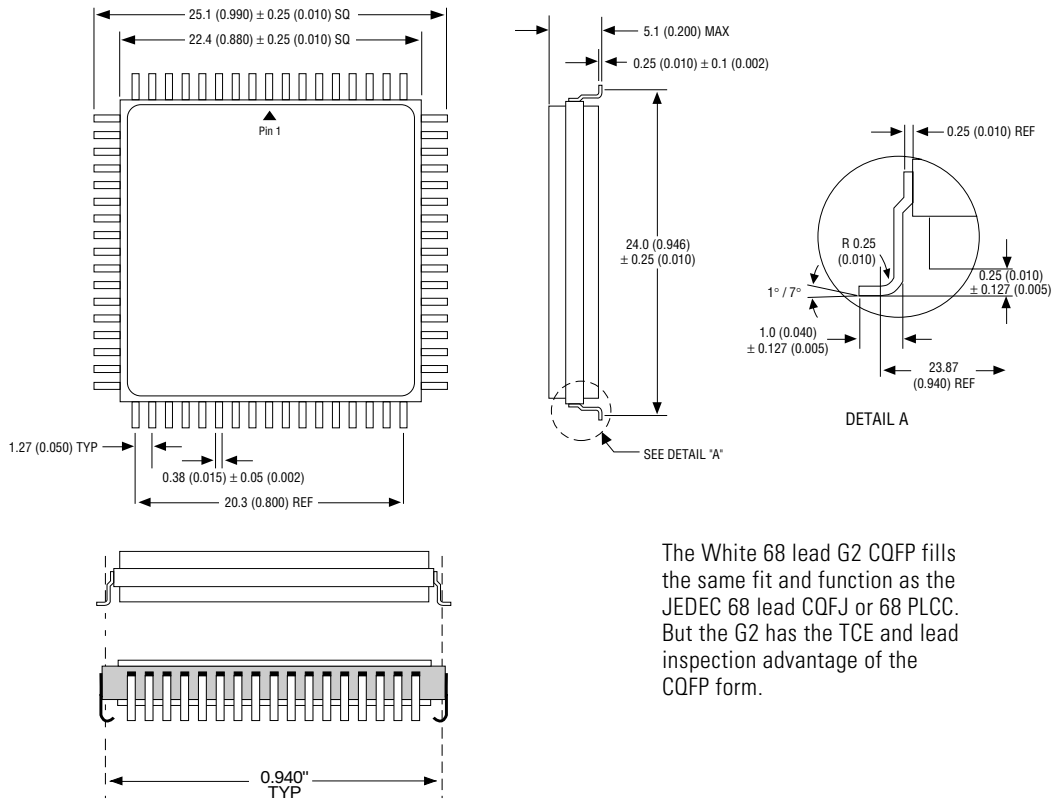
I_{OL} & I_{OH} are adjusted to simulate a typical resistive load circuit.

ATE tester includes jig capacitance.

**TIMING WAVEFORM - READ CYCLE****WRITE CYCLE - $\overline{WE}$ CONTROLLED****WRITE CYCLE - $\overline{CS}$ CONTROLLED**

**PACKAGE 402: 66 PIN, PGA TYPE, CERAMIC HEX-IN-LINE PACKAGE, HIP (H2)**

ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

**PACKAGE 500: 68 LEAD, CERAMIC QUAD FLAT PACK, CQFP (G2)**

The White 68 lead G2 CQFP fills the same fit and function as the JEDEC 68 lead CQFJ or 68 PLCC. But the G2 has the TCE and lead inspection advantage of the CQFP form.

ALL LINEAR DIMENSIONS ARE MILLIMETERS AND PARENTHETICALLY IN INCHES

**ORDERING INFORMATION****W S 512K 32 X B V - XXX X X E X****LEAD FINISH:**

Blank = Gold plated leads

A = Solder dip leads

E = Epitaxial Layer

DEVICE GRADE:

M = Military Screened -55°C to +125°C

I = Industrial -40°C to +85°C

C = Commercial 0°C to +70°C

PACKAGE TYPE:

H2 = Ceramic Hex-In-line Package, HIP (Package 402)

G2 = 22 mm Ceramic Quad Flat Pack, CQFP (Package 500)

ACCESS TIME (ns)**Low Voltage Supply 3.3V ± 10%****BiCMOS****IMPROVEMENT MARK:**

N = No Connect at pin 21 and 39 in HIP for Upgrades

ORGANIZATION, 512Kx32

User configurable as 1Mx16 or 2Mx8

SRAM**WHITE MICROELECTRONICS**