INTEGRATED CIRCUITS
UNITRODE

UC1526
UC2526
UC3526

Regulating Pulse Width Modulator

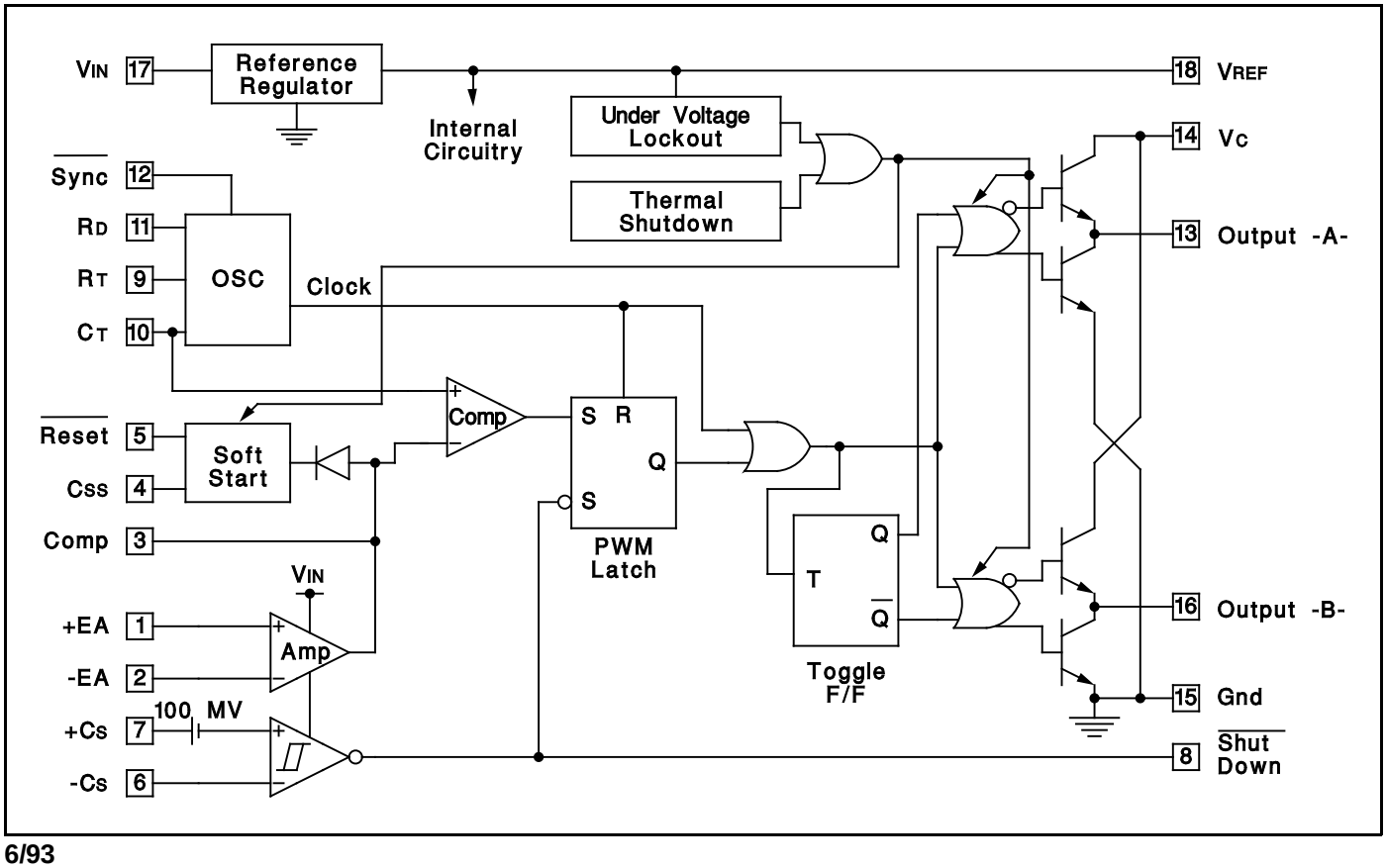
FEATURES

- 8 To 35V Operation
- 5V Reference Trimmed To ±1%
- 1Hz To 400kHz Oscillator Range
- Dual 100mA Source/Sink Outputs
- Digital Current Limiting
- Double Pulse Suppression
- Programmable Deadtime
- Under-Voltage Lockout
- Single Pulse Metering
- Programmable Soft-Start
- Wide Current Limit Common Mode Range
- TTL/CMOS Compatible Logic Ports
- Symmetry Correction Capability
- Guaranteed 6 Unit Synchronization

DESCRIPTION

The UC1526 is a high performance monolithic pulse width modulator circuit designed for fixed-frequency switching regulators and other power control applications. Included in an 18-pin dual-in-line package are a temperature compensated voltage reference, sawtooth oscillator, error amplifier, pulse width modulator, pulse metering and setting logic, and two low impedance power drivers. Also included are protective features such as soft-start and under-voltage lockout, digital current limiting, double pulse inhibit, a data latch for single pulse metering, adjustable deadtime, and provision for symmetry correction inputs. For ease of interface, all digital control ports are TTL and B-series CMOS compatible. Active LOW logic design allows wired-OR connections for maximum flexibility. This versatile device can be used to implement single-ended or push-pull switching regulators of either polarity, both transformerless and transformer coupled. The UC1526 is characterized for operation over the full military temperature range of -55°C to +125°C. The UC2526 is characterized for operation from -25°C to +85°C, and the UC3526 is characterized for operation from 0° to +70°C.

BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (Note 1, 2)

Input Voltage (+V_{IN}) . . . . . +40V
Collector Supply Voltage (+V_C) . . . . . +40V
Logic Inputs . . . . . -0.3V to +5.5V
Analog Inputs . . . . . -0.3V to +V_{IN}
Source/Sink Load Current (each output) 200mA
Reference Load Current 50mA
Logic Sink Current 15mA
Power Dissipation at T_A = +25°C (Note 2) 1000mW
Power Dissipation at T_C = +25°C (Note 2) 3000mW
Operating Junction Temperature . . . . . +150°C
Storage Temperature Range . . . . . -65°C to +150°C
Lead Temperature (soldering, 10 seconds) . . . . . +300°C

Note 1: Values beyond which damage may occur.
Note 2: Consult packaging section of databook for thermal limitations and considerations of package.

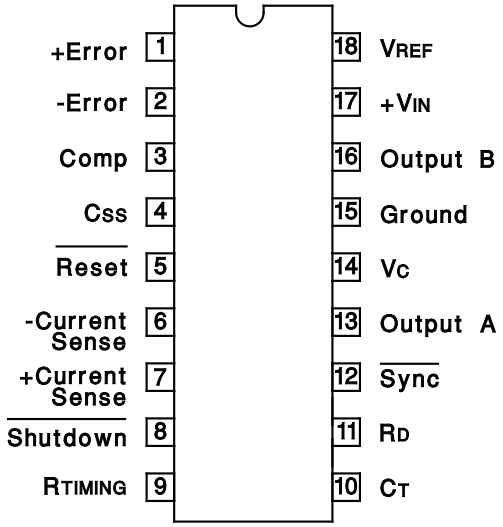
RECOMMENDED OPERATING CONDITIONS (Note 3)

Input Voltage . . . . . +8V to +35V
Collector Supply Voltage . . . . . +4.5V to +35V
Sink/Source Load Current (each output) . . . . . 0 to 100mA
Reference Load Current . . . . . 0 to 20mA
Oscillator Frequency Range . . . . . 1Hz to 400kHz
Oscillator Timing Resistor . . . . . 2kΩ to 150kΩ
Oscillator Timing Capacitor . . . . . 1nF to 20µF
Available Deadtime Range at 40kHz . . . . . 3% to 50%
Operating Ambient Temperature Range
UC1526 . . . . . -55°C to +125°C
UC2526 . . . . . -25°C to +85°C
UC3526 . . . . . -0°C to +70°C

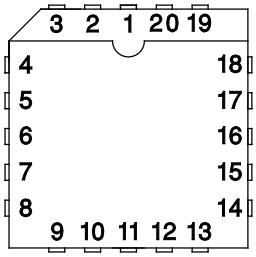
Note 3: Range over which the device is functional and parameter limits are guaranteed.

CONNECTION DIAGRAMS

DIL-18, SOIC-18 (TOP VIEW)
J or N Package, DW Package



PLCC-20, LCC-20
(TOP VIEW)
Q and L Packages



PACKAGE PIN FUNCTION	
FUNCTION	**PIN**
N/C	1
+Error	2
-Error	3
Comp.	4
C_{SS}	5
$\overline{\text{Reset}}$	6
- Current Sense	7
+ Current Sense	8
$\overline{\text{Shutdown}}$	9
R_{TIMING}	10
C_T	11
R_D	12
Sync	13
Output A	14
V_C	15
N/C	16
Ground	17
Output B	18
+V_{IN}	19
V_{REF}	20

ELECTRICAL CHARACTERISTICS: +V_{IN} = 15V, and over operating ambient temperature, unless otherwise specified, $T_A = T_J$.

PARAMETER	TEST CONDITIONS	UC1526 / UC2526			UC3526			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Reference Section (Note 4)								
Output Voltage	T_J = + 25°C	4.95	5.00	5.05	4.90	5.00	5.10	V
Line Regulation	+V_{IN} = 8 to 35V		10	20		10	30	mV
Load Regulation	I_L = 0 to 20mA		10	30		10	50	mV
Temperature Stability	Over Operating T_J		15	50		15	50	mV
Total Output Voltage Range	Over Recommended Operating Conditions	4.90	5.00	5.10	4.85	5.00	5.15	V
Short Circuit Current	V_{REF} = 0V	25	50	100	25	50	100	mA
Under -Voltage Lockout								
$\overline{\text{RESET}}$ Output Voltage	V_{REF} = 3.8V		0.2	0.4		0.2	0.4	V
	V_{REF} = 4.8V	2.4	4.8		2.4	4.8		V

Note 4: I_L = 0mA.

ELECTRICAL CHARACTERISTICS: $+V_{IN}$ = 15V, and over operating ambient temperature, unless otherwise specified, $T_A = T_J$.

PARAMETER	TEST CONDITIONS	UC1526 / UC2526			UC3526			UNITS
		MIN	TYP	MAX	MIN	TYP	MAX	
Oscillator Section (Note 5)								
Initial Accuracy	T_J = + 25°C		±3	±8		±3	±8	%
Voltage Stability	$+V_{IN}$ = 8 to 35V		0.5	1		0.5	1	%
Temperature Stability	Over Operating T_J		7	10		3	5	%
Minimum Frequency	R_T = 150kΩ, C_T = 20µF			1			1	Hz
Maximum Frequency	R_T = 2kΩ, C_T = 1.0nF	400			400			kHz
Sawtooth Peak Voltage	$+V_{IN}$ = 35V		3.0	3.5		3.0	3.5	V
Sawtooth Valley Voltage	$+V_{IN}$ = 8V	0.5	1.0		0.5	1.0		V
Error Amplifier Section (Note 6)								
Input Offset Voltage	$R_S \leq$ 2kΩ		2	5		2	10	mV
Input Bias Current			-350	-1000		-350	-2000	nA
Input Offset Current			35	100		35	200	nA
DC Open Loop Gain	$R_L \geq$ 10MΩ	64	72		60	72		dB
HIGH Output Voltage	V_{PIN1}-$V_{PIN2} \geq$ 150mV, I_{SOURCE} = 100µA	3.6	4.2		3.6	4.2		V
LOW Output Voltage	V_{PIN2}-$V_{PIN1} \geq$ 150mV, I_{SINK} = 100µA		0.2	0.4		0.2	0.4	V
Common Mode Rejection	$R_S \leq$ 12kΩ	70	94		70	94		dB
Supply Voltage Rejection	$+V_{IN}$ = 12 to 18V	66	80		66	80		dB
PWM Comparator (Note 5)								
Minimum Duty Cycle	$V_{COMPENSATION}$ = +0.4V			0			0	%
Maximum Duty Cycle	$V_{COMPENSATION}$ = +3.6V	45	49		45	49		%
Digital Ports ($\overline{\text{SYNC}}$, $\overline{\text{SHUTDOWN}}$, and $\overline{\text{RESET}}$)								
HIGH Output Voltage	I_{SOURCE} =40µA	2.4	4.0		2.4	4.0		V
LOW Output Voltage	I_{SINK} = 3.6mA		0.2	0.4		0.2	0.4	V
HIGH Input Current	V_{IH} = +2.4V		-125	-200		-125	-200	µA
LOW Input Current	V_{IL} = +0.4V		-225	-360		-225	-360	µA
Current LImit Comparator (Note 7)								
Sense Voltage	$R_S \leq$ 50Ω	90	100	110	80	100	120	mV
Input Bias Current			-3	-10		-3	-10	µA
Soft-Start Section								
Error Clamp Voltage	$\overline{\text{RESET}}$ = +0.4V		0.1	0.4		0.1	0.4	V
Cs Charging Current	$\overline{\text{RESET}}$ =+2.4V	50	100	150	50	100	150	µA
Output Drivers (Each Output) (Note 8)								
HIGH Output Voltage	I_{SOURCE} = 20mA	12.5	13.5		12.5	13.5		V
	I_{SOURCE} = 100mA	12	13		12	13		V
LOW Output Voltage	I_{SINK} = 20mA		0.2	0.3		0.2	0.3	V
	I_{SINK} = 100mA		1.2	2.0		1.2	2.0	V
Collector Leakage	V_C = 40V		50	150		50	150	µA
Rise Time	C_L = 1000pF		0.3	0.6		0.3	0.6	µs
Fall Time	C_L = 1000pF		0.1	0.2		0.1	0.2	µs
Power Consumption (Note 9)								
Standby Current	$\overline{\text{SHUTDOWN}}$ = +0.4V		18	30		18	30	mA

Note 4: I_L = 0mA.
Note 5: F_{OSC} = 40kHz (R_T = 4.12kΩ ± 1%, C_T = 0.1µF ± 1%, R_D = 0Ω)
Note 6: V_{CM} = 0 to +5.2V
Note 8: V_C = +15V
Note 9: $+V_{IN}$ = +35V, R_T = 4.12kΩ

APPLICATIONS INFORMATION

Voltage Reference

The reference regulator of the UC1526 is based on a temperature compensated zener diode. The circuitry is fully active at supply voltages above +8V, and provides up to 20mA of load current to external circuitry at +5.0V. In systems where additional current is required, an external PNP transistor can be used to boost the available current. A rugged low frequency audio-type transistor should be used, and lead lengths between the PWM and transistor should be as short as possible to minimize the risk of oscillations. Even so, some types of transistors may require collector-base capacitance for stability. Up to 1 amp of load current can be obtained with excellent regulation if the device selected maintains high current gain.

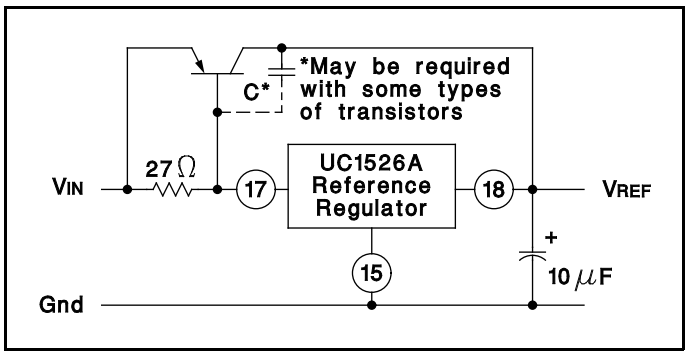


Figure 1. Extending Reference Output Current

Under-Voltage Lockout

The under-voltage lockout circuit protects the UC1526 and the power devices it controls from inadequate supply voltage, If $+V_{IN}$ is too low, the circuit disables the output drivers and holds the $\overline{\text{RESET}}$ pin LOW. This prevents spurious output pulses while the control circuitry is stabilizing, and holds the soft-start timing capacitor in a discharged state.

The circuit consists of a +1.2V bandgap reference and comparator circuit which is active when the reference voltage has risen to $3V_{BE}$ or +1.8V at 25°C. When the reference voltage rises to approximately +4.4V, the circuit enables the output drivers and releases the $\overline{\text{RESET}}$ pin, allowing a normal soft-start. The comparator has 200mV of hysteresis to minimize oscillation at the trip point. When $+V_{IN}$ to the PWM is removed and the reference drops to +4.2V, the under-voltage circuit pulls $\overline{\text{RESET}}$ LOW again. The soft-start capacitor is immediately discharged, and the PWM is ready for another soft-start cycle.

The UC1526 can operate from a +5V supply by connecting the V_{REF} pin to the $+V_{IN}$ pin and maintaining the supply between +4.8 and +5.2V.

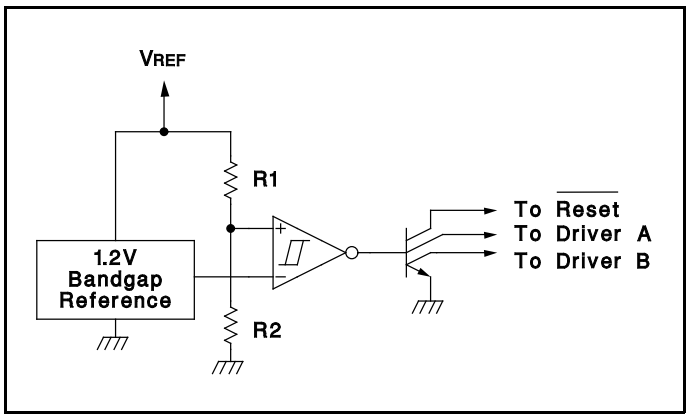


Figure 2. Under-Voltage Lockout Schematic

Soft-Start Circuit

The soft-start circuit protects the power transistors and rectifier diodes from high current surges during power supply turn-on. When supply voltage is first applied to the UC1526, the under-voltage lockout circuit holds $\overline{\text{RESET}}$ LOW with Q_3. Q_1 is turned on, which holds the soft-start capacitor voltage at zero. The second collector of Q_1 clamps the output of the error amplifier to ground, guaranteeing zero duty cycle at the driver outputs. When the supply voltage reaches normal operating range, $\overline{\text{RESET}}$ will go HIGH. Q_1 turns off, allowing the internal 100mA current source to charge C_S. Q_2 clamps the error amplifier output to $1V_{BE}$ above the voltage on C_S. As the soft-start voltage ramps up to +5V, the duty cycle of the PWM linearly increases to whatever value the voltage regulation loop requires for an error null.

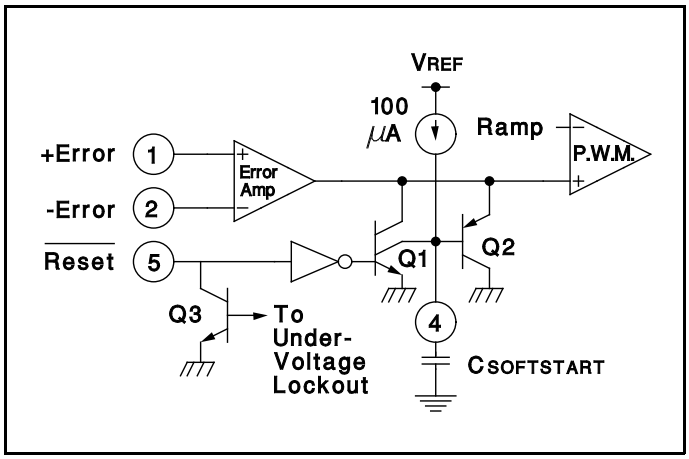


Figure 3. Soft-Start Circuit Schematic

Digital Control Ports

The three digital control ports of the UC1526 are bi-directional. Each pin can drive TTL and 5V CMOS logic directly, up to a fan-out of 10 low-power Schottky gates. Each pin can also be directly driven by open-collector

APPLICATIONS INFORMATION (cont.)

TTL, open-drain CMOS, and open-collector voltage comparators; fan-in is equivalent to 1 low-power Schottky gate. Each port is normally HIGH; the pin is pulled LOW to activate the particular function. Driving $\overline{\text{SYNC}}$ LOW initiates a discharge cycle in the oscillator. Pulling $\overline{\text{SHUTDOWN}}$ LOW immediately inhibits all PWM output pulses. Holding $\overline{\text{RESET}}$ LOW discharges the soft-start capacitor. The logic threshold is +1.1V at +25°C. Noise immunity can be gained at the expense of fan-out with an external 2k pull-up resistor to +5V.

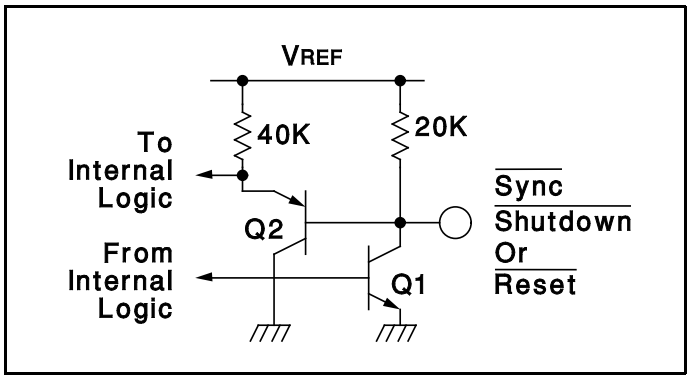


Figure 4. Digital Control Port Schematic

Oscillator

The oscillator is programmed for frequency and dead time with three components: R_T, C_T and R_D. Two waveforms are generated: a sawtooth waveform at pin 10 for pulse width modulation, and a logic clock at pin 12. The following procedure is recommended for choosing timing values:

1. With R_D = 0 (pin 11 shorted to ground) select values for R_T and C_T from Figure 7 to give the desired oscillator period. Remember that the frequency at each driver output is half the oscillator frequency, and the frequency at the $+V_C$ terminal is the same as the oscillator frequency.

2. If more dead time is required, select a large value of R_D. At 40kHz dead time increases by 400ns/Ω .

3. Increasing the dead time will cause the oscillator frequency to decrease slightly. Go back and decrease the value of R_T slightly to bring the frequency back to the nominal design value.

The UC1526 can be synchronized to an external logic clock by programming the oscillator to free-run at a frequency 10% slower than the sync frequency. A periodic LOW logic pulse approximately 0.5µs wide at the $\overline{\text{SYNC}}$ pin will then lock the oscillator to the external frequency.

Multiple devices can be synchronized together by programming one master unit for the desired frequency and then sharing its sawtooth and clock waveforms with the slave units. All C_T terminals are connected to the C_T pin of the master, and all $\overline{\text{SYNC}}$ terminals are likewise connected to the $\overline{\text{SYNC}}$ pin of the master. Slave R_T terminals are left open or connected to V_{REF}. Slave R_D terminals may be either left open or grounded.

Error Amplifier

The error amplifier is a transconductance design, with an output impedance of 2MΩ . Since all voltage gain takes place at the output pin, the open-loop gain/frequency characteristics can be controlled with shunt reactance to ground. When compensated for unity-gain stability with 100pF, the amplifier has an open-loop pole at 800Hz.

The input connections to the error amplifier are determined by the polarity of the switching supply output voltage. For positive supplies, the common-mode voltage is +5.0V and the feedback connections in Figure 6A are used. With negative supplies, the common-mode voltage is ground and the feedback divider is connected between the negative output and the +5.0V reference voltage, as shown in Figure 6B.

Output Drivers

The totem-pole output drivers of the UC1526 are designed to source and sink 100mA continuously and 200mA peak. Loads can be driven either from the output pins 13 and 16, or from the $+V_C$, as required.

Since the bottom transistor of the totem-pole is allowed to saturate, there is a momentary conduction path from the $+V_C$ terminal to ground during switching. To limit the resulting current spikes a small resistor in series with pin 14 is always recommended. The resistor value is determined by the driver supply voltage, and should be chosen for 200mA peak currents.

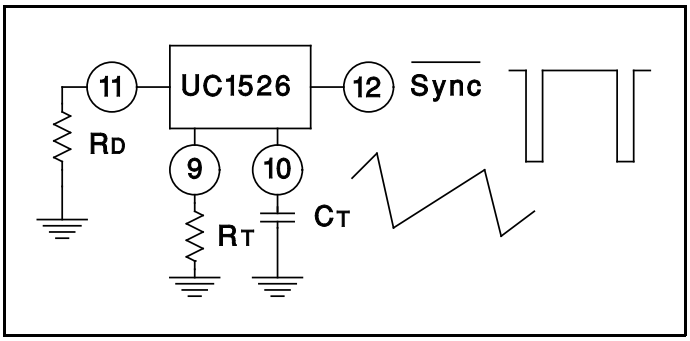


Figure 5. Oscillator Connections and Waveforms

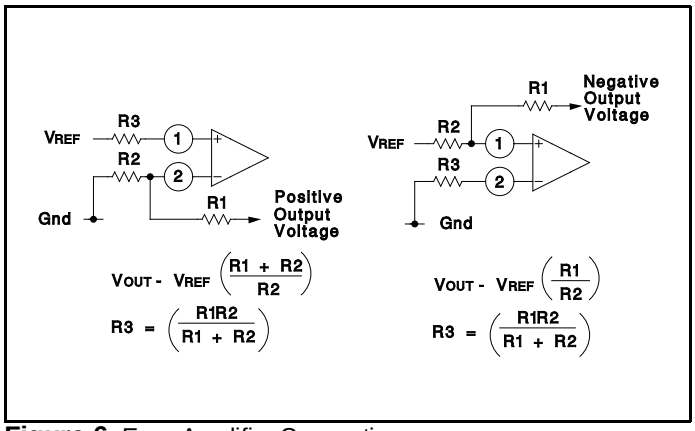


Figure 6. Error Amplifier Connections

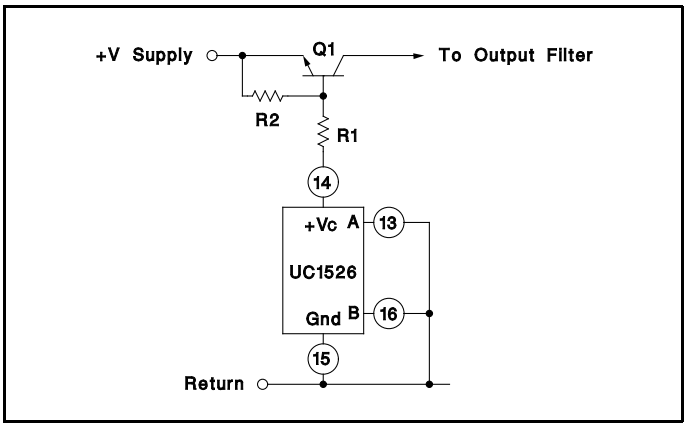


Figure 8. Single-Ended Configuration

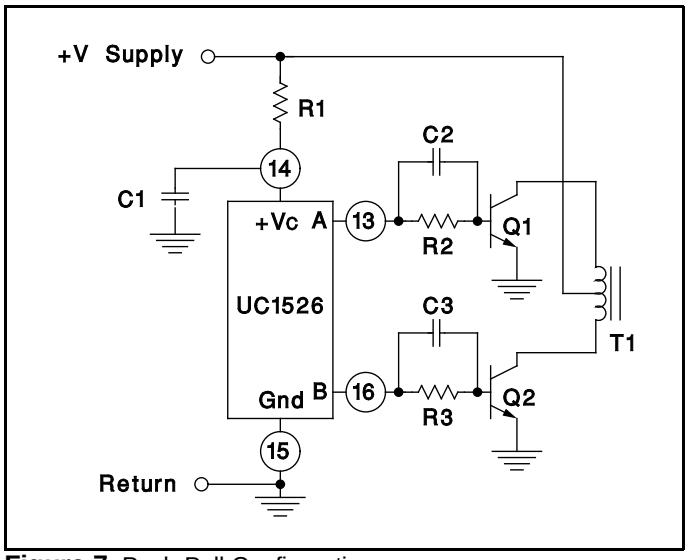


Figure 7. Push-Pull Configuration

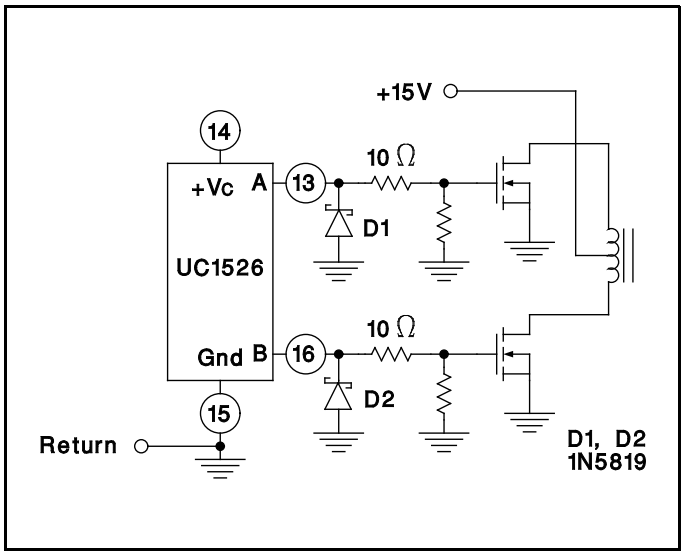
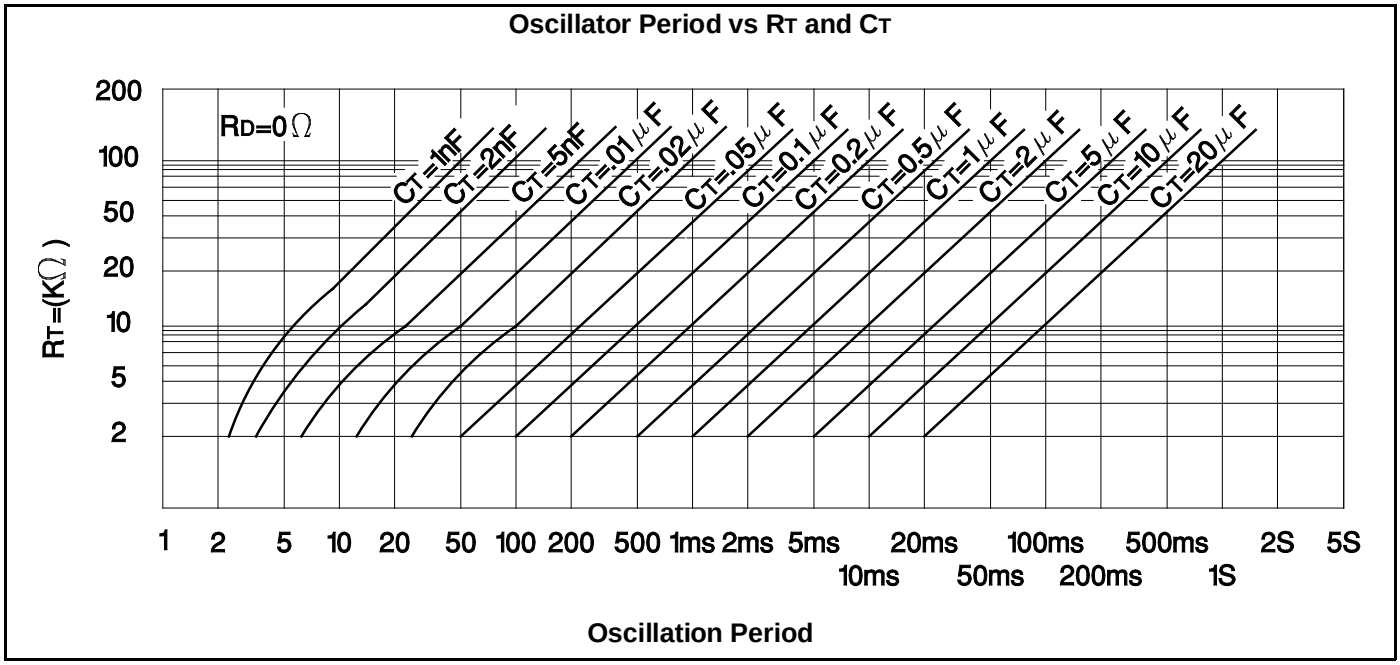


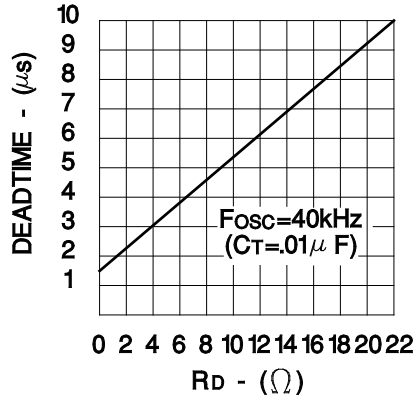
Figure 9. Driving N-channel Power Mosfets

TYPICAL CHARACTERISTICS

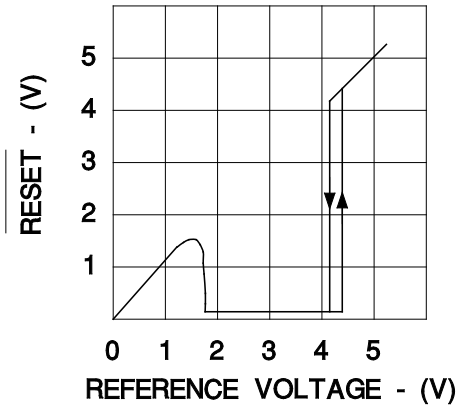


TYPICAL CHARACTERISTICS

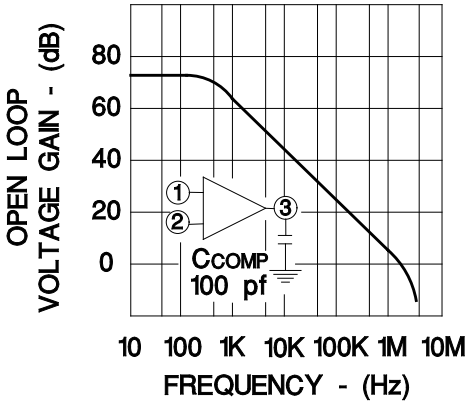
Output Driver Deadtime vs RD Value



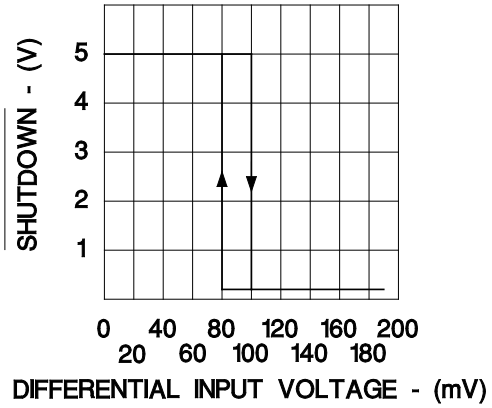
Under Voltage Lockout Characteristic



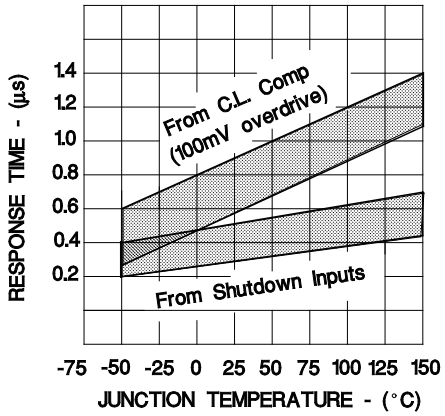
Error Amplifier Open Loop Gain vs Frequency



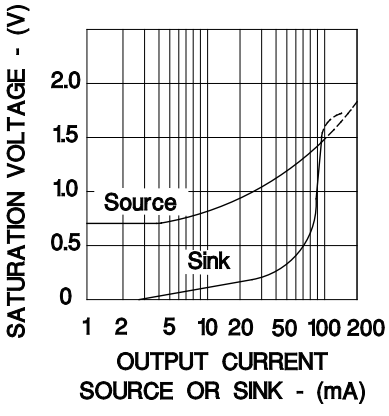
Current Limit Transfer Function



Shutdown Delay



Output Driver Saturation Voltage



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7 CONTINENTAL BLVD. • MERRIMACK, NH 03054
TEL. (603) 424-2410 • FAX (603) 424-3460

In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/Ball Finish	MSL Peak Temp (3)
85515012A	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	Level-NC-NC-NC
8551501VA	ACTIVE	CDIP	J	18	1	TBD	A42 SNPB	Level-NC-NC-NC
UC1526J	ACTIVE	CDIP	J	18	1	TBD	A42 SNPB	Level-NC-NC-NC
UC1526J883B	ACTIVE	CDIP	J	18	1	TBD	A42 SNPB	Level-NC-NC-NC
UC1526L	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	Level-NC-NC-NC
UC1526L883B	ACTIVE	LCCC	FK	20	1	TBD	POST-PLATE	Level-NC-NC-NC
UC2526J	ACTIVE	CDIP	J	18	1	TBD	A42 SNPB	Level-NC-NC-NC
UC2526N	ACTIVE	PDIP	N	18	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-NC-NC-NC
UC2526NG4	ACTIVE	PDIP	N	18	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-NC-NC-NC
UC3526DW	ACTIVE	SOIC	DW	18	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UC3526DWG4	ACTIVE	SOIC	DW	18	40	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UC3526DWTR	ACTIVE	SOIC	DW	18	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UC3526DWTRG4	ACTIVE	SOIC	DW	18	2000	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-2-260C-1 YEAR
UC3526J	ACTIVE	CDIP	J	18	1	TBD	A42 SNPB	Level-NC-NC-NC
UC3526N	ACTIVE	PDIP	N	18	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-NC-NC-NC
UC3526NG4	ACTIVE	PDIP	N	18	20	Green (RoHS & no Sb/Br)	CU NIPDAU	Level-NC-NC-NC

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
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(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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Mailing Address: Texas Instruments
Post Office Box 655303 Dallas, Texas 75265