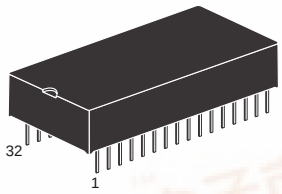
M48T512Y
M48T512V

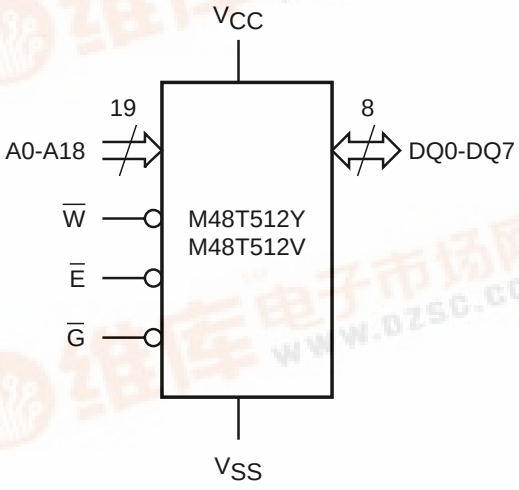
3.3V-5V 4 Mbit (512Kb x8) TIMEKEEPER® SRAM

- INTEGRATED ULTRA LOW POWER SRAM, REAL TIME CLOCK, POWER-FAIL CONTROL CIRCUIT, BATTERY, and CRYSTAL
- BCD CODED YEAR, MONTH, DAY, DATE, HOURS, MINUTES, and SECONDS
- AUTOMATIC POWER-FAIL CHIP DESELECT and WRITE PROTECTION
- WRITE PROTECT VOLTAGES: (V_{PFD} = Power-fail Deselect Voltage)
  - M48T512Y: 4.2V ≤ V_{PFD} ≤ 4.5V
  - M48T512V: 2.7V ≤ V_{PFD} ≤ 3.0V
- CONVENTIONAL SRAM OPERATION; UNLIMITED WRITE CYCLES
- SOFTWARE CONTROLLED CLOCK CALIBRATION FOR HIGH ACCURACY APPLICATIONS
- 10 YEARS of DATA RETENTION and CLOCK OPERATION in the ABSENCE OF POWER
- PIN and FUNCTION COMPATIBLE with INDUSTRY STANDARD 512K X 8 SRAMS
- SELF-CONTAINED BATTERY and CRYSTAL in DIP PACKAGE



PMDIP32 (PM)
Module

Figure 1. Logic Diagram



DESCRIPTION

The M48T512Y/V TIMEKEEPER RAM is a 512Kb x 8 non-volatile static RAM and real time clock organized as 524,288 words by 8 bits. The special DIP package provides a fully integrated battery back-up memory and real time clock solution.

Table 1. Signal Names

A0-A18	Address Inputs
DQ0-DQ7	Data Inputs / Outputs
$\overline{E}$	Chip Enable Input
$\overline{G}$	Output Enable Input
$\overline{W}$	Write Enable Input
V_{CC}	Supply Voltage
V_{SS}	Ground

Table 2. Absolute Maximum Ratings (1)

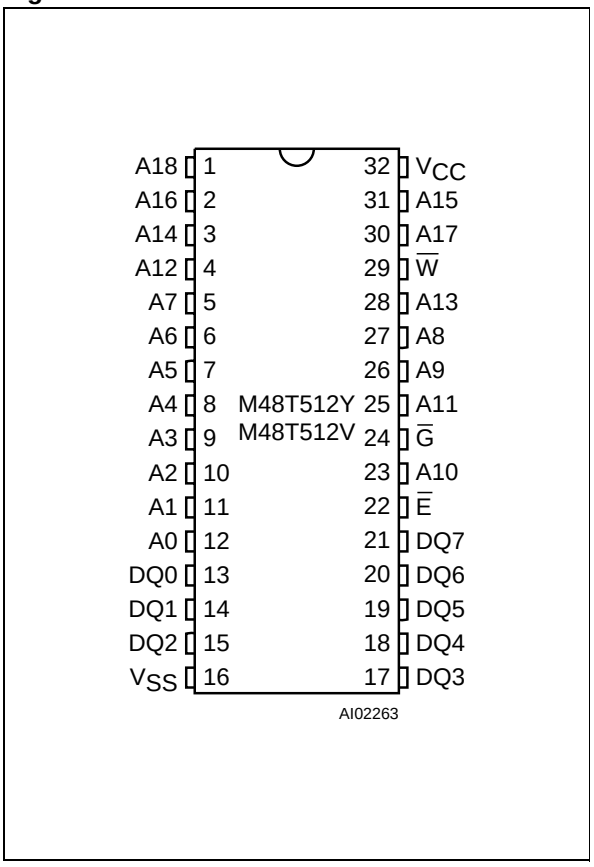
Symbol	Parameter		Value	Unit
T_A	Ambient Operating Temperature		0 to 70	°C
T_{STG}	Storage Temperature (V_{CC} Off, Oscillator Off)		–40 to 85	°C
T_{SLD} (2)	Lead Solder Temperature for 10 seconds		260	°C
V_{IO}	Input or Output Voltages		–0.3 to V_{CC} +0.3	V
V_{CC}	Supply Voltage	M48T512Y	–0.3 to 7.0	V
		M48T512V	–0.3 to 4.6	V
I_O	Output Current		20	mA
P_D	Power Dissipation		1	W

Note: 1. Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to the absolute maximum rating conditions for extended periods of time may affect reliability.

2. Soldering temperature not to exceed 260°C for 10 seconds (total thermal budget not to exceed 150°C for longer than 30 seconds).

CAUTION: *Negative undershoots below –0.3V are not allowed on any pin while in the Battery Back-up mode.*

Figure 2. DIP Connections



The M48T512Y/V directly replaces industry standard 512Kb x 8 SRAMs. It also provides the nonvolatility of Flash without any requirement for special write timing or limitations on the number of writes that can be performed.

The 32 pin 600 mil DIP Hybrid houses a controller chip, SRAM, quartz crystal, and a long life lithium button cell in a single package. Figure 3 illustrates the static memory array and the quartz controlled clock oscillator. The clock locations contain the year, month, date, day, hour, minute, and second in 24 hour BCD format. Corrections for 28, 29 (leap year - compliant until the year 2100), 30, and 31 day months are made automatically. Byte 7FFF8h is the clock control register. This byte controls user access to the clock information and also stores the clock calibration setting. The seven clock bytes (7FFFFh-7FFF9h) are not the actual clock counters, they are memory locations consisting of BiPORT™ read/write memory cells within the static RAM array. The M48T512Y/V includes a clock control circuit which updates the clock bytes with current information once per second. The information can be accessed by the user in the same manner as any other location in the static memory array. The M48T512Y/V also has its own Power-Fail Detect circuit. This control circuitry constantly monitors the supply voltage for an out of tolerance condition. When V_{CC} is out of tolerance, the circuit write protects the TIMEKEEPER register data and external SRAM, providing data security in the midst of unpredictable system operation. As V_{CC} falls, the control circuitry automatically switches to the battery, maintaining data and clock operation until valid power is restored.

READ MODE

The M48T512Y/V is in the Read Mode whenever $\overline{W}$ (Write Enable) is high and $\overline{E}$ (Chip Enable) is low. The unique address specified by the 19 Address Inputs defines which one of the 524,288 bytes of data is to be accessed. Valid data will be available at the Data I/O pins within Address Ac-

Table 3. Operating Modes (1)

Mode	V_{CC}	$\overline{E}$	$\overline{G}$	$\overline{W}$	DQ0-DQ7	Power
Deselect	4.5V to 5.5V or 3.0V to 3.6V	V_{IH}	X	X	High Z	Standby
Write		V_{IL}	X	V_{IL}	D_{IN}	Active
Read		V_{IL}	V_{IL}	V_{IH}	D_{OUT}	Active
Read		V_{IL}	V_{IH}	V_{IH}	High Z	Active
Deselect	V_{SO} to V_{PFD} (min) (2)	X	X	X	High Z	CMOS Standby
Deselect	$\leq V_{SO}$ (2)	X	X	X	High Z	Battery Back-up Mode

Note: 1. X = V_{IH} or V_{IL}.
2. See Table 7 for details.

cess Time (t_{AVQV}) after the last address input signal is stable, providing the $\overline{E}$ and $\overline{G}$ access times are also satisfied. If the $\overline{E}$ and $\overline{G}$ access times are not met, valid data will be available after the latter of the Chip Enable Access Times (t_{ELQV}) or Output Enable Access Time (t_{GLQV}). The state of the eight three-state Data I/O signals is controlled by $\overline{E}$ and $\overline{G}$. If the outputs are activated before t_{AVQV}, the data lines will be driven to an indeterminate state until t_{AVQV}. If the Address Inputs are changed while $\overline{E}$ and $\overline{G}$ remain active, output data will remain valid for Output Data Hold Time (t_{AXQX}) but will go indeterminate until the next Address Access.

WRITE MODE

The M48T512Y/V is in the Write Mode whenever $\overline{W}$ (Write Enable) and $\overline{E}$ (Chip Enable) are low state after the address inputs are stable. The start of a write is referenced from the latter occurring falling edge of $\overline{W}$ or $\overline{E}$. A write is terminated by the earlier rising edge of $\overline{W}$ or $\overline{E}$. The addresses must be held valid throughout the cycle. $\overline{E}$ or $\overline{W}$ must return high for a minimum of t_{EHAX} from Chip Enable or t_{WHAX} from Write Enable prior to the initiation of another read or write cycle. Data-in must be valid t_{DVWH} prior to the end of write and remain valid for t_{WHDX} afterward. $\overline{G}$ should be kept high during write cycles to avoid bus contention; although, if the output bus has been activated by a low on $\overline{E}$ and $\overline{G}$ a low on $\overline{W}$ will disable the outputs t_{WLQZ} after $\overline{W}$ falls.

Table 4. AC Measurement Conditions

Input Rise and Fall Times	≤ 5ns
Input Pulse Voltages	0 to 3V
Input and Output Timing Ref. Voltages	1.5V

Note that Output Hi-Z is defined as the point where data is no longer driven.

Figure 3. AC Testing Load Circuit

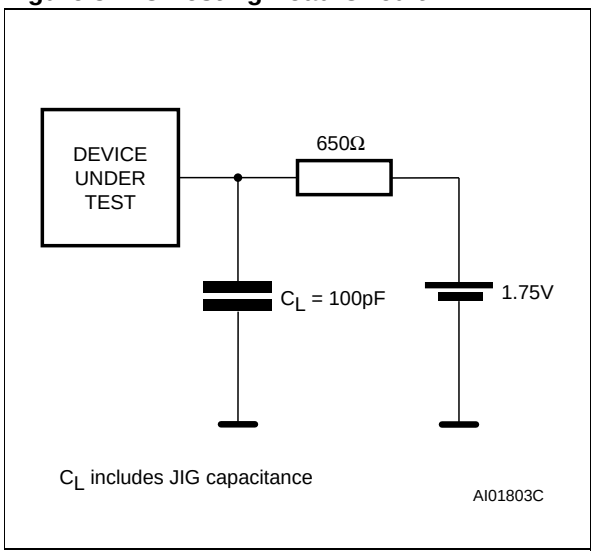
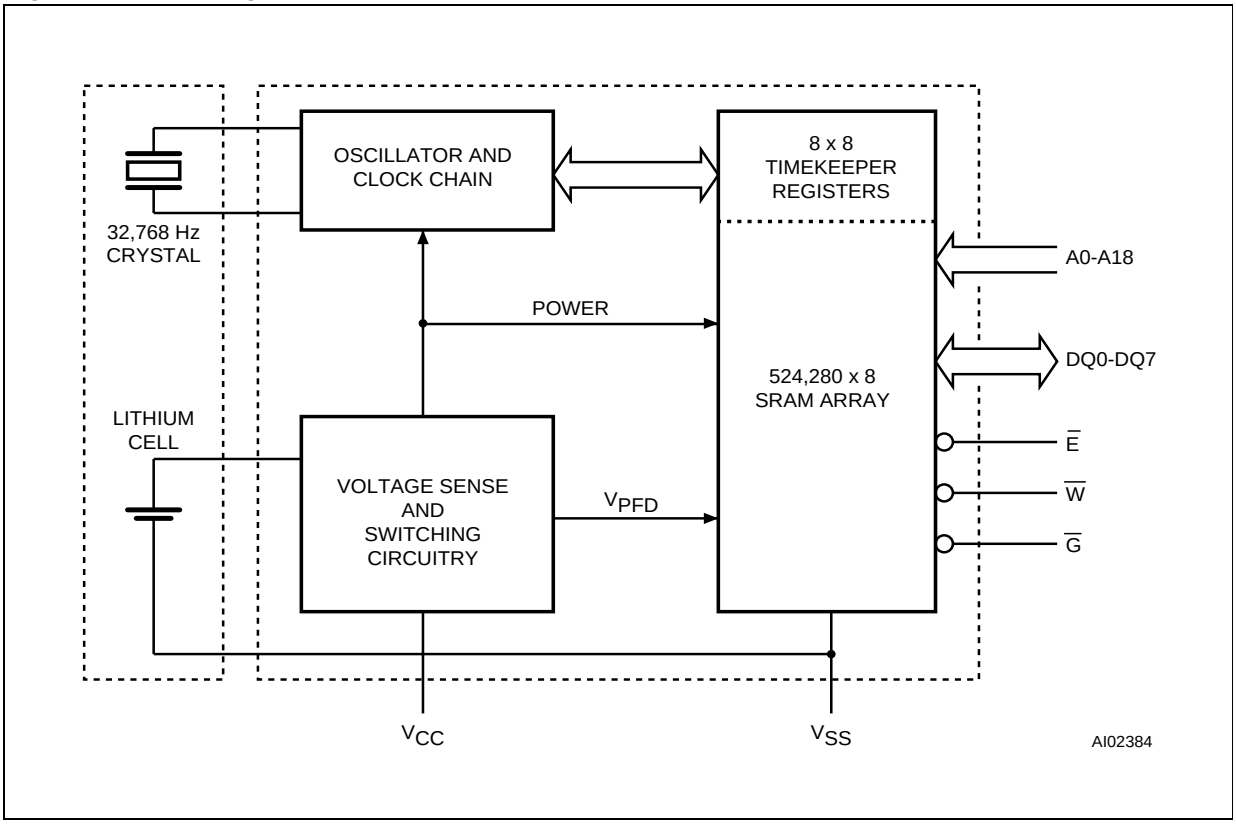


Figure 4. Block Diagram



DATA RETENTION MODE

With valid V_{CC} applied, the M48T512Y/V operates as a conventional BYTEWIDE™ static RAM. Should the supply voltage decay, the RAM will automatically deselect, write protecting itself when V_{CC} falls between V_{PFD} (max), V_{PFD} (min) window. All outputs become high impedance and all inputs are treated as "don't care".

Note: A power failure during a write cycle may corrupt data at the current addressed location, but does not jeopardize the rest of the RAM's content. At voltages below V_{PFD} (min), the memory will be in a write protected state, provided the V_{CC} fall time is not less than t_F. The M48T512Y/V may respond to transient noise spikes on V_{CC} that cross into the deselect window during the time the device is sampling V_{CC}.Therefore, decoupling of the power supply lines is recommended. When V_{CC} drops below V_{SO}, the control circuit switches power to the internal battery, preserving data and powering the clock. The internal energy source will maintain data in the M48T512Y/V for an accumulated period of at least 10 years at room temperature. As system power rises above V_{SO}, the battery is disconnected, and the power supply is switched to external V_{CC}. Write protection continues until V_{CC} reaches V_{PFD} (min) plus t_{ER} (min). Normal RAM operation can resume t_{ER} after V_{CC} exceeds V_{PFD} (max). Refer to Application Note (AN1012) on the ST Web Site for more information on battery life.

CLOCK OPERATIONS

Reading the Clock Updates to the TIMEKEEPER registers should be halted before clock data is read to prevent reading data in transition. Because the BiPORT TIMEKEEPER cells in the RAM array are only data registers, and not the actual clock counters, updating the registers can be halted without disturbing the clock itself. Updating is halted when a '1' is written to the READ bit, D6 in the Control Register (7FFF8h). As long as a '1' remains in that position, updating is halted. After a halt is issued, the registers reflect the count; that is, the day, date, and time that were current at the moment the halt command was issued. All of the TIMEKEEPER registers are updated simultaneously. A halt will not interrupt an update in progress. Updating occurs 1 second after the READ bit is reset to a '0'.

Table 5. Capacitance (1)
(T_A = 25 °C, f = 1 MHz)

Symbol	Parameter	Test Condition	Min	Max	Unit
C_{IN}	Input Capacitance	V_{IN} = 0V		20	pF
C_{IO} (2)	Input / Output Capacitance	V_{OUT} = 0V		20	pF

Note: 1. Effective capacitance measured with power supply at 5V (M48T512Y) or 3.3V (M48T512V). Sampled only, not 100% tested.
2. Outputs deselected.

Table 6A. DC Characteristics
(T_A = 0 to 70 °C; V_{CC} = 4.5V to 5.5V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI} (1)	Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}		±2	µA
I_{LO} (1)	Output Leakage Current	0V ≤ V_{OUT} ≤ V_{CC}		±2	µA
I_{CC}	Supply Current	Outputs open		115	mA
I_{CC1}	Supply Current (Standby) TTL	$\overline{E}$ = V_{IH}		8	mA
I_{CC2}	Supply Current (Standby) CMOS	$\overline{E}$ = V_{CC} – 0.2V		4	mA
V_{IL}	Input Low Voltage		–0.3	0.8	V
V_{IH}	Input High Voltage		2.2	V_{CC} + 0.3	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = –1mA	2.4		V

Note: 1. Outputs deselected.

Table 6B. DC Characteristics
(T_A = 0 to 70 °C; V_{CC} = 3.0V to 3.6V)

Symbol	Parameter	Test Condition	Min	Max	Unit
I_{LI} (1)	Input Leakage Current	0V ≤ V_{IN} ≤ V_{CC}		±2	µA
I_{LO} (1)	Output Leakage Current	0V ≤ V_{OUT} ≤ V_{CC}		±2	µA
I_{CC}	Supply Current	Outputs open		60	mA
I_{CC1}	Supply Current (Standby) TTL	$\overline{E}$ = V_{IH}		4	mA
I_{CC2}	Supply Current (Standby) CMOS	$\overline{E}$ = V_{CC} – 0.2V		3	mA
V_{IL}	Input Low Voltage		–0.3	0.4	V
V_{IH}	Input High Voltage		2.2	V_{CC} + 0.3	V
V_{OL}	Output Low Voltage	I_{OL} = 2.1mA		0.4	V
V_{OH}	Output High Voltage	I_{OH} = –1mA	2.2		V

Note: 1. Outputs deselected.

Figure 5. Power Down/Up Mode AC Waveforms

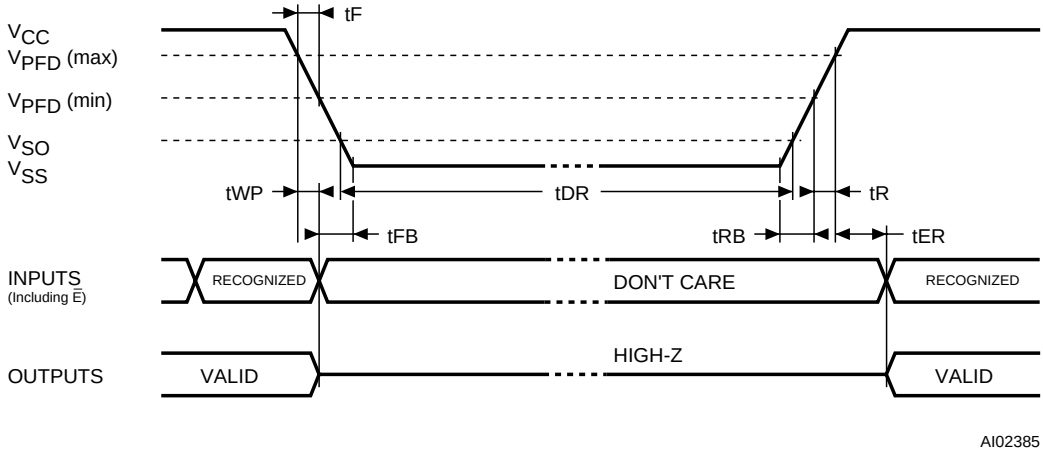


Table 7. Power Down/Up Trip Points DC Characteristics (1)
(T_A = 0 to 70 °C)

Symbol	Parameter		Min	Typ	Max	Unit
V_{PFD}	Power-fail Deselect Voltage	M48T512Y	4.2	4.35	4.5	V
		M48T512V	2.7	2.9	3.0	V
V_{SO}	Battery Back-up Switchover Voltage	M48T512Y		3.0		V
		M48T512V		V_{PFD} –100mV		
t_{DR} (2)	Expected Data Retention Time		10			YEARS

Note: 1. All voltages referenced to V_{SS}.
2. At 25°C.

Table 8. Power Down/Up AC Characteristics
(T_A = 0 to 70 °C)

Symbol	Parameter		Min	Max	Unit
t_F (1)	V_{PFD} (max) to V_{PFD} (min) V_{CC} Fall Time		300		µs
t_{FB} (2)	V_{PFD} (min) to V_{SS} V_{CC} Fall Time	M48T512Y	10		µs
		M48T512V	150		µs
t_R	V_{PFD} (min) to V_{PFD} (max) V_{CC} Rise Time		10		µs
t_{RB}	V_{SS} to V_{PFD} (min) V_{CC} Rise Time		1		µs
t_{WP}	Write Protect Time on V_{CC} = V_{PFD}		40	150	µs
t_{ER}	$\overline{E}$ Recovery Time		40	200	ms

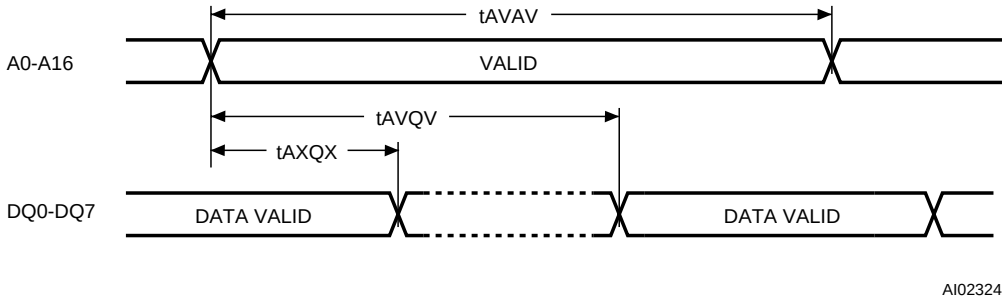
Note: 1. V_{PFD} (max) to V_{PFD} (min) fall time of less than t_F may result in deselection/write protection not occurring until 200µs after V_{CC} passes V_{PFD} (min).
2. V_{PFD} (min) to V_{SS} fall time of less than t_{FB} may cause corruption of RAM data.

Table 9. Read Mode AC Characteristics
(T_A = 0 to 70 °C)

Symbol	Parameter	M48T512Y		M48T512V		Unit
		-70		-85		
		Min	Max	Min	Max	
t_{AVAV}	Read Cycle Time	70		85		ns
t_{AVQV} (1)	Address Valid to Output Valid		70		85	ns
t_{ELQV} (1)	Chip Enable Low to Output Valid		70		85	ns
t_{GLQV} (1)	Output Enable Low to Output Valid		40		55	ns
t_{ELQX} (2)	Chip Enable Low to Output Transition	5		5		ns
t_{GLQX} (2)	Output Enable Low to Output Transition	5		5		ns
t_{EHQZ} (2)	Chip Enable High to Output Hi-Z		25		30	ns
t_{GHQZ} (2)	Output Enable High to Output Hi-Z		25		30	ns
t_{AXQX} (1)	Address Transition to Output Transition	10		5		ns

Note: 1. C_L = 100pF.
2. C_L = 5pF.

Figure 6. Address Controlled, Read Mode AC Waveforms



Setting the Clock. Bit D7 of the Control Register (7FFF8h) is the WRITE bit. Setting the WRITE bit to a '1', like the READ bit, halts updates to the TIMEKEEPER registers. The user can then load them with the correct day, date, and time data in 24 hour BCD format (see Table 11). Resetting the WRITE bit to a '0' then transfers the values of all time registers 7FFFFh-7FFF9h to the actual TIMEKEEPER counters and allows normal operation to resume. After the WRITE bit is reset, the next clock update will occur approximately one second later. See Application Note, AN923, (TIMEKEEPERS "ROLLING INTO" THE 21ST CENTURY) on the ST Web Site for more information on Century Rollover.

Note: Upon power-up, both the WRITE bit and the READ bit will be reset to '0'.

Stopping and Starting the Oscillator. The oscillator may be stopped at any time. If the device is going to spend a significant amount of time on the shelf, the oscillator can be turned off to minimize current drain on the battery. The STOP bit is located at Bit D7 within 7FFF9h. Setting it to a '1' stops the oscillator. The M48T512Y/V is shipped from STMicroelectronics with the STOP bit set to a '1'. When reset to a '0', the M48T512Y/V oscillator starts after approximately one second.

Note: It is not necessary to set the WRITE bit when setting or resetting the FREQUENCY TEST bit (FT) or the STOP bit (ST).

Table 10. Write Mode AC Characteristics
(T_A = 0 to 70 °C)

Symbol	Parameter	M48T512Y		M48T512V		Unit
		-70		-85		
		Min	Max	Min	Max	
t_{AVAV}	Write Cycle Time	70		85		ns
t_{AVWL}	Address Valid to Write Enable Low	0		0		ns
t_{AVEL}	Address Valid to Chip Enable Low	0		0		ns
t_{WLWH}	Write Enable Pulse Width	50		60		ns
t_{ELEH}	Chip Enable Low to Chip Enable High	55		65		ns
t_{WHAX}	Write Enable High to Address Transition	5		5		ns
t_{EHAX}	Chip Enable High to Address Transition	10		15		ns
t_{DVWH}	Input Valid to Write Enable High	30		35		ns
t_{DVEH}	Input Valid to Chip Enable High	30		35		ns
t_{WHDX}	Write Enable High to Input Transition	5		5		ns
t_{EHDX}	Chip Enable High to Input Transition	10		15		ns
t_{WLQZ} (1, 2)	Write Enable Low to Output Hi-Z		25		30	ns
t_{AVWH}	Address Valid to Write Enable High	60		70		ns
t_{AVE1H}	Address Valid to Chip Enable High	60		70		ns
t_{WHQX} (1, 2)	Write Enable High to Output Transition	5		5		ns

Note: 1. C_L = 5pF.
2. If $\overline{E}$ goes low simultaneously with $\overline{W}$ going low, the outputs remain in the high impedance state.

Calibrating the Clock. The M48T512Y/V is driven by a quartz controlled oscillator with a nominal frequency of 32,768Hz. The devices are factory calibrated at 25°C and tested for accuracy. Clock accuracy will not exceed 35 ppm (parts per million) oscillator frequency error at 25°C, which equates to about ±1.53 minutes per month. When the Calibration circuit is properly employed, accuracy improves to better than +4 ppm at 25°C. The oscillation rate of crystals changes with temperature. The M48T512Y/V design employs periodic counter correction. The calibration circuit adds or subtracts counts from the oscillator divider circuit at the divide by 256 stage, as shown in Figure 10. The number of times pulses which are blanked (subtracted, negative calibration) or split (added, positive calibration) depends upon the value loaded into the five Calibration bits found in the Control Register. Adding counts speeds the clock up, subtracting counts slows the clock down. The Calibration bits occupy the five lower order bits (D4-D0) in the Control Register 7FFF8h. These bits can be set to represent any value between 0 and 31 in binary form. Bit D5 is a Sign bit; '1' indicates positive calibration, '0' indicates negative calibration. Calibration occurs within a 64 minute cycle. The first 62 minutes in the cycle may, once per minute, have one second either shortened by 128 or lengthened by 256 oscillator cycles. If a binary '1' is loaded into the register, only the first 2 minutes in the 64 minute cycle will be modified; if a binary 6 is loaded, the first 12 will be affected, and so on. Therefore, each calibration step has the effect of adding 512 or subtracting 256 oscillator cycles for every 125, 829, 120 actual oscillator cycles; that is, +4.068 or –2.034 ppm of adjustment per calibration step in the calibration register.

Figure 7. Chip Enable or Output Enable Controlled, Read Mode AC Waveforms

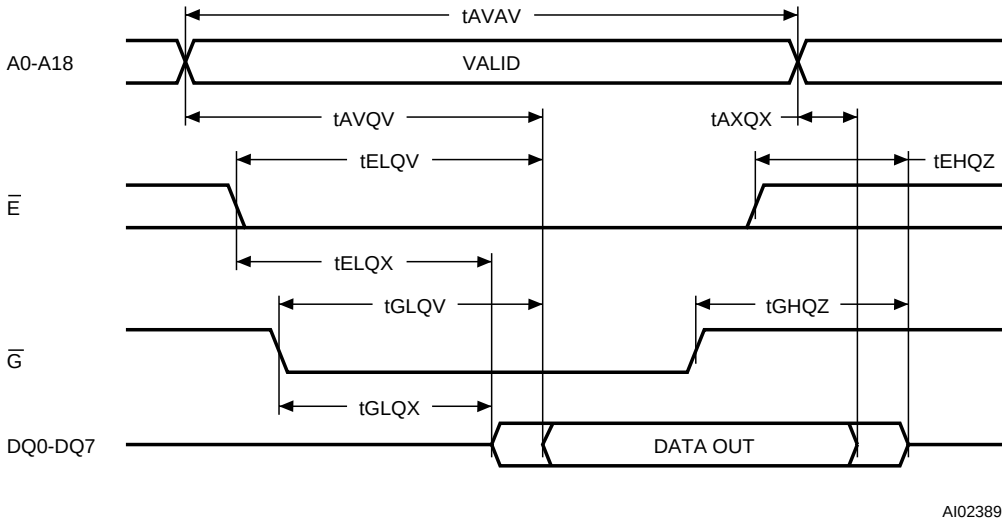


Figure 8. Write Enable Controlled, Write AC Waveforms

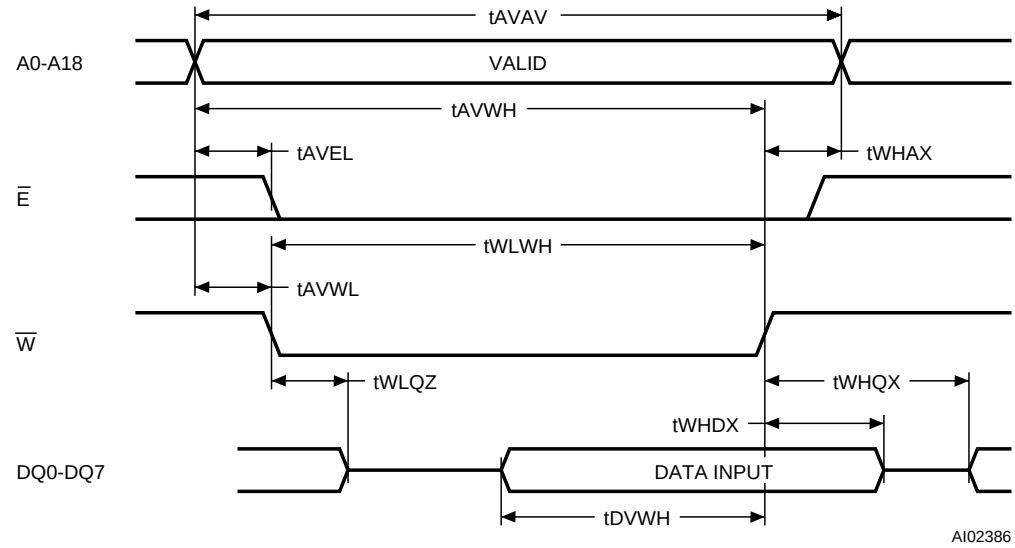
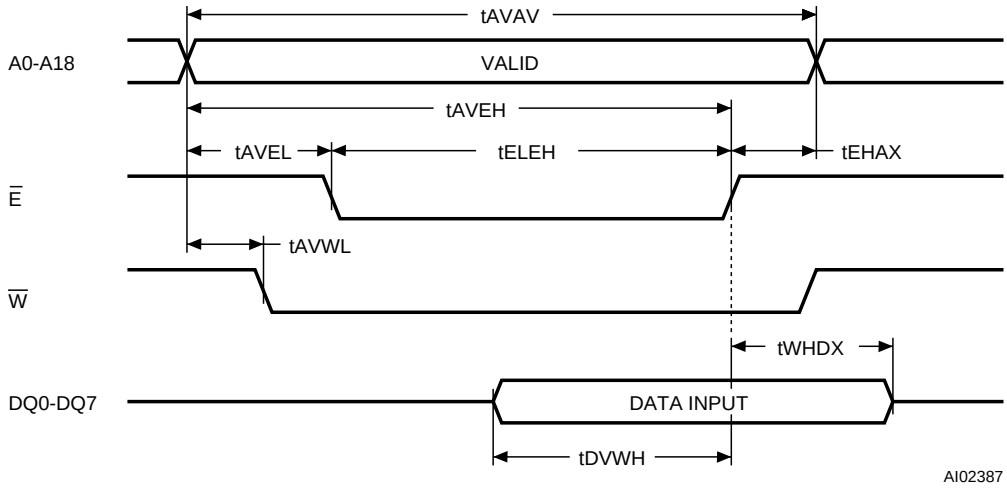


Figure 9. Chip Enable Controlled, Write AC Waveforms



Assuming that the oscillator is running at exactly 32,768Hz, each of the 31 increments in the Calibration byte would represent +10.7 or –5.35 seconds per month which corresponds to a total range of +5.5 or –2.75 minutes per month. Figure 10 illustrates a TIMEKEEPER calibration waveform.

One method for ascertaining how much calibration a given M48T512Y/V may require involves setting the clock, letting it run for a month and comparing it to a known accurate reference and recording deviation over a fixed period of time.

Calibration values, including the number of seconds lost or gained in a given period, can be found in STMicroelectronics Application Note: TIMEKEEPER CALIBRATION. This allows the designer to give the end user the ability to calibrate the clock as the environment requires, even if the final product is packaged in a non-user serviceable enclosure. The designer could provide a simple utility that accesses the Calibration bits. For more information on calibration, see Application Note (TIMEKEEPER CALIBRATION) on the ST Web Site.

POWER SUPPLY DECOUPLING and UNDERSHOOT PROTECTION

Note: I_{CC} transients, including those produced by output switching, can produce voltage fluctuations, resulting in spikes on the V_{CC} bus. These transients can be reduced if capacitors are used to store energy, which stabilizes the V_{CC} bus. The energy stored in the bypass capacitors will be released as low going spikes are generated or energy will be absorbed when overshoots occur. A ceramic bypass capacitor value of 0.1µF is recommended in order to provide the needed filtering. In addition to transients that are caused by normal SRAM operation, power cycling can generate negative voltage spikes on V_{CC} that drive it to values below V_{SS} by as much as one volt. These negative spikes can cause data corruption in the SRAM while in battery backup mode. To protect from these voltage spikes, ST recommends connecting a schottky diode from V_{CC} to V_{SS} (cathode connected to V_{CC}, anode to V_{SS}). (Schottky diode 1N5817 is recommended for through hole and MBRS120T3 is recommended for surface mount).

Table 11. Register Map

Address	Data								Function/Range BCD Format	
	D7	D6	D5	D4	D3	D2	D1	D0		
7FFFFh	10 Years				Year				Year	00-99
7FFFEh	0	0	0	10 M	Month				Month	01-12
7FFFDh	0	0	10 Date		Date				Date	01-31
7FFFCh	0	0	0	0	0	Day			Day	01-07
7FFFBh	0	0	10 Hours		Hours				Hour	00-23
7FFFAh	0	10 Minutes			Minutes				Minutes	00-59
7FFF9h	ST	10 Seconds			Seconds				Seconds	00-59
7FFF8h	W	R	S	Calibration					Control	

Keys: S = SIGN Bit
R = READ Bit
W = WRITE Bit
ST = STOP Bit
0 = Must be set to zero

Figure 10. Calibration Waveform

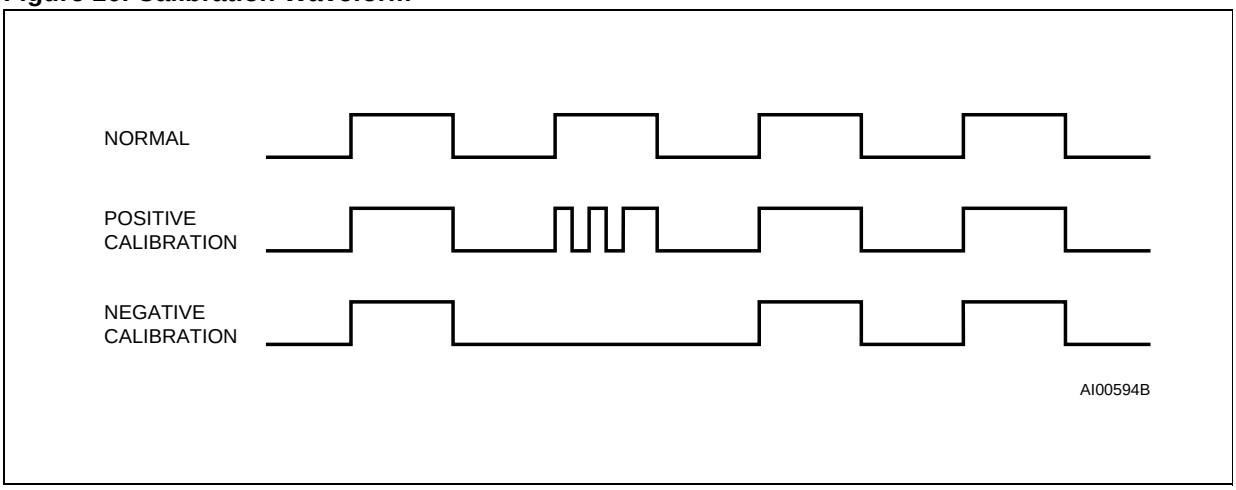


Table 12. Ordering Information Scheme

Example: M48T512Y -70 PM 1

Device Type
M48T

Supply Voltage and Write Protect Voltage
512Y = V_{CC} = 4.5V to 5.5V; V_{PFD} = 4.2V to 4.5V
512V = V_{CC} = 3.0V to 3.6V; V_{PFD} = 2.7V to 3.0V

Speed
-70 = 70ns
-85 = 85 ns

Package
PM = PMDIP32

Temperature Range
1 = 0 to 70 °C

For a list of available options (Speed, Package, etc...) or for further information on any aspect of this device, please contact the ST Sales Office nearest to you.

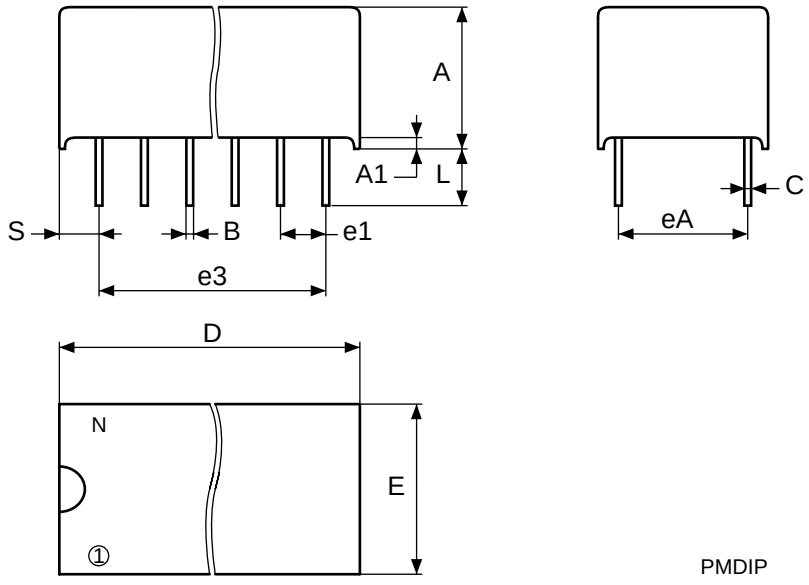
Table 13. Revision History

Date	Revision Details
June 1998	First Issue
12/03/99	M48T512Y: V_{PFD} (Min) changed Figure 3 changed t_{FB} changed (Figure 5, Table 8) t_{RB} changed (Figure 5, Table 8)

Table 14. PMDIP32 - 32 pin Plastic Module DIP, Package Mechanical Data

Symb	mm			inches		
	Typ	Min	Max	Typ	Min	Max
A		9.27	9.52		0.365	0.375
A1		0.38	–		0.015	–
B		0.43	0.59		0.017	0.023
C		0.20	0.33		0.008	0.013
D		42.42	43.18		1.670	1.700
E		18.03	18.80		0.710	0.740
e1		2.29	2.79		0.090	0.110
e3		34.29	41.91		1.350	1.650
eA		14.99	16.00		0.590	0.630
L		3.05	3.81		0.120	0.150
S		1.91	2.79		0.075	0.110
N	32			32		

Figure 11. PMDIP32 - 32 pin Plastic Module DIP, Package Outline



Drawing is not to scale.