PRELIMINARY **CY27H512**

64K x 8 High-Speed CMOS EPROM

Features

- CMOS for optimum speed/power
- High speed
  - t_{AA} = 25 ns max. (commercial)
  - t_{AA} = 35 ns max. (military)
- Low power
  - 275 mW max.
  - Less than 85 mW when deselected
- Byte-wide memory organization
- 100% reprogrammable in the windowed package
- EPROM technology
- Capable of withstanding >2001V static discharge
- Available in
  - 32-pin PLCC
  - 28-pin TSOP-I
  - 28-pin, 600-mil plastic or hermetic DIP
  - 32-pin hermetic LCC

Functional Description

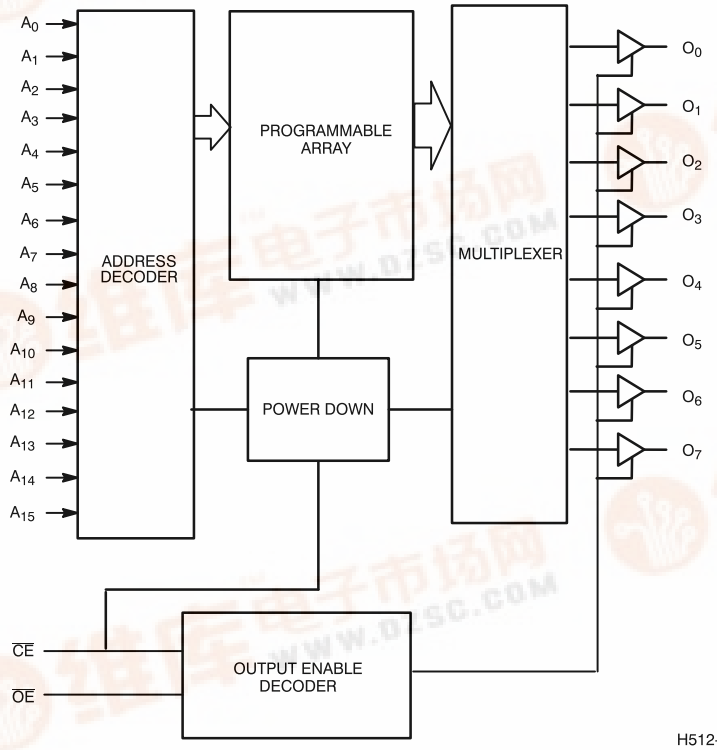
The CY27H512 is a high-performance, 512K CMOS EPROM organized in 64 Kbytes. It is available in industry-standard 28-pin, 600-mil DIP, 32-pin LCC and PLCC, and 28-pin TSOP-I packages. These devices offer high-density storage combined with 40-MHz performance. The CY27H512 is available in windowed and opaque packages. Windowed packages allow the device to be erased with UV light for 100% reprogrammability.

The CY27H512 is equipped with a power-down chip enable ($\overline{CE}$) input and output enable ($\overline{OE}$). When $\overline{CE}$ is deasserted, the device powers down to a low-power standby mode. The $\overline{OE}$ pin three-states the outputs without putting the device into standby mode. While $\overline{CE}$ offers lower power, $\overline{OE}$ provides a more rapid transition to and from three-stated outputs.

The memory cells utilize proven EPROM floating-gate technology and byte-wide intelligent programming algorithms. The EPROM cell requires only 12.75 V for the supervoltage and low programming current allows for gang programming. The device allows for each memory location to be tested 100%, because each location is written to, erased, and repeatedly exercised prior to encapsulation. Each device is also tested for AC performance to guarantee that the product will meet DC and AC specification limits after customer programming.

The CY27H512 is read by asserting both the $\overline{CE}$ and the $\overline{OE}$ inputs. The contents of the memory location selected by the address on inputs $A_{15}-A_0$ will appear at the outputs O_7-O_0.

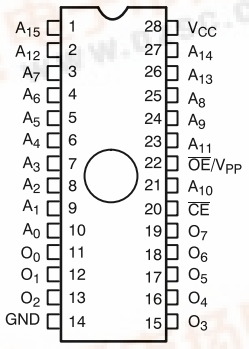
Logic Block Diagram



H512-1

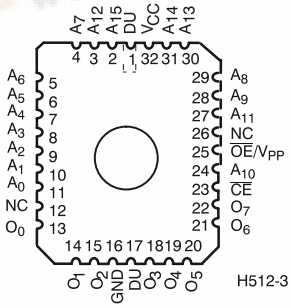
Pin Configurations

DIP
Top View



H512-2

LCC/PLCC[1]
Top View

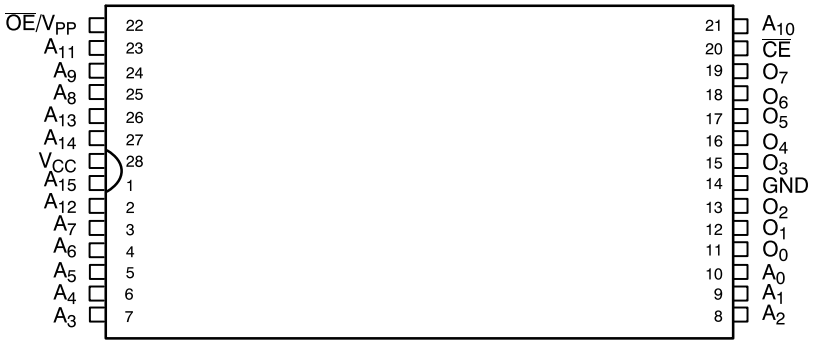


H512-3

Note:
1. For LCC/PLCC only: Pins 1 and 17 are common and tied to the die attach pad. They should not be used.

Pin Configurations (continued)

TSOP
Top View
Type 1



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Selection Guide

		27H512−25	27H512−30	27H512−35	27H512−45	27H512−55	27H512−70
Maximum Access Time (ns)		25	30	35	45	55	70
$\overline{CE}$ Access Time (ns)	Com'l	30	35	35	45	55	70
	Mil			40	45	55	70
$\overline{OE}$ Access Time (ns)	Com'l	12	15	15	15	20	25
	Mil			20	20	20	25
I_{CC}[2] (mA) Power Supply Current	Com'l	75	75	50	50	50	50
	Mil			85	60	60	60
I_{SB}[3] (mA) Stand-by Current	Com'l	15	15	15	15	15	15
	Mil			25	25	25	25

Maximum Ratings

(Above which the useful life may be impaired. For user guidelines, not tested.)

Storage Temperature ..... −65°C to +150°C

Ambient Temperature with Power Applied ..... −55°C to +125°C

Supply Voltage to Ground Potential ..... −0.5V to +7.0V

DC Voltage Applied to Outputs in High Z State ..... −0.5V to +5.5V

DC Input Voltage ..... −3.0V to +7.0V

Transient Input Voltage ..... −3.0V for <20 ns

DC Program Voltage 13.0V

UV Erasure ..... 7258 Wsec/cm^2

Static Discharge Voltage ..... >2001V (per MIL-STD-883, Method 3015)

Latch-Up Current ..... >200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	5V ± 10%
Industrial[4]	−40°C to +85°C	5V ± 10%
Military[5]	−55°C to +125°C	5V ± 10%

Notes:

2. V_{CC} = Max., I_{OUT} = 0 mA, f=10 MHz.
3. V_{CC} = Max., $\overline{CE}$ = V_{IH}.
4. Contact a Cypress representative for industrial temperature range specification.
5. T_A is the "instant on" case temperature.

Electrical Characteristics Over the Operating Range[6, 7]

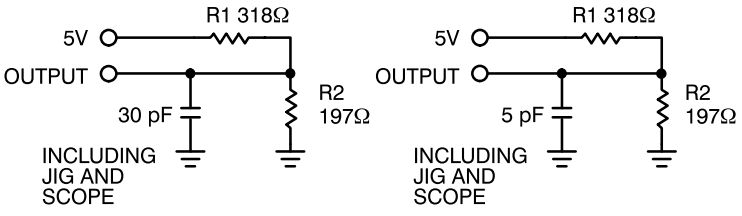
Parameter	Description	Test Conditions		27H512−25 27H512−30 Min.	27H512−25 27H512−30 Max.	27H512−35 Min.	27H512−35 Max.	27H512−45 27H512−55 27H512−70 Min.	27H512−45 27H512−55 27H512−70 Max.	Unit
V_{OH}	Output HIGH Voltage	V_{CC} = Min., I_{OH} = −4.0 mA		2.4		2.4		2.4		V
V_{OL}	Output LOW Voltage	V_{CC} = Min., I_{OL} = 12.0 mA			0.45		0.45		0.45	V
V_{IH}	Input HIGH Level	Guaranteed Input Logical HIGH Voltage for All Inputs		2.0	V_{CC}+0.5	2.0	V_{CC}+0.5	2.0	V_{CC}+0.5	V
V_{IL}	Input LOW Level	Guaranteed Input Logical LOW Voltage for All Inputs			0.8		0.8		0.8	V
I_{IX}	Input Leakage Current	GND ≤ V_{IN} ≤ V_{CC}		−10	+10	−10	+10	−10	+10	μA
I_{OZ}	Output Leakage Current	GND ≤ V_{OUT} ≤ V_{CC}, Output Disable		−10	+10	−10	+10	−10	+10	μA
I_{CC}	Power Supply Current	V_{CC}=Max., I_{OUT}=0 mA, f=10 MHz	Com'l		75		50		50	mA
			Mil				85		60	mA
I_{SB}	Stand-By Current	V_{CC}=Max., $\overline{CE}$ = V_{IH}	Com'l		15		15		15	mA
			Mil				25		25	mA

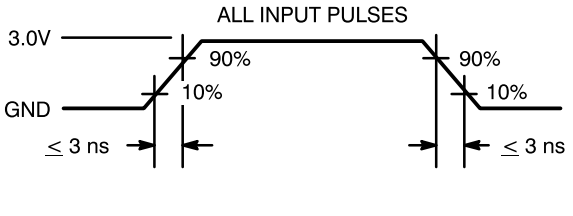
Capacitance[7]

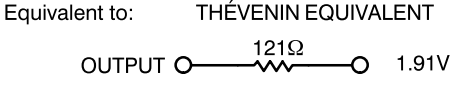
Parameter	Description	Test Conditions	Max.	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 5.0V	10	pF
C_{OUT}	Output Capacitance		10	pF

Notes:
6. See the last page of this specification for Group A subgroup testing information.
7. See Introduction to CMOS PROMs in this Data Book for general information on testing.

AC Test Loads and Waveforms



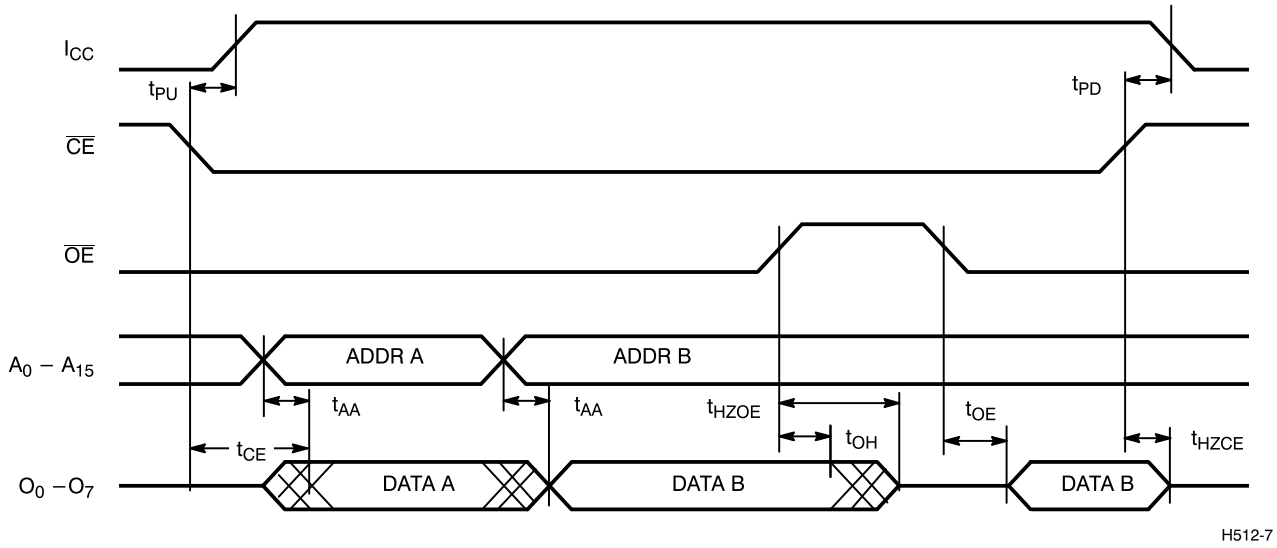




Switching Characteristics Over the Operating Range

Parameter	Description	27H512−25		27H512−30		27H512−35		27H512−45		27H512−55		27H512−70		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
t_{AA}	Address to Output Valid		25		30		35		45		55		70	ns
t_{OE}	$\overline{OE}$ Active to Output Valid		12		15		15		15		20		25	ns
t_{HZOE}	$\overline{OE}$ Inactive to High Z		12		15		15		15		20		25	ns
t_{CE}	$\overline{CE}$ Active to Output Valid		30		35		35		45		55		70	ns
t_{HZCE}	$\overline{CE}$ Inactive to High Z		12		15		15		15		20		25	ns
t_{PU}	$\overline{CE}$ Active to Power-Up	0		0		0		0		0		0		ns
t_{PD}	$\overline{CE}$ Inactive to Power-Down		30		35		40		40		50		60	ns
t_{OH}	Output Data Hold	0		0		0		0		0		0		ns

Switching Waveform



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Erasure Characteristics

Wavelengths of light less than 4000 Angstroms begin to erase the CY27H512 in the windowed package. For this reason, an opaque label should be placed over the window if the EPROM is exposed to sunlight or fluorescent lighting for extended periods of time.

The recommended dose of ultraviolet light for erasure is a wavelength of 2537 Angstroms for a minimum dose (UV intensity multiplied by exposure time) of 25 Wsec/cm^2. For an ultraviolet lamp with a 12 mW/cm^2 power rating, the exposure time would be approximately 35 minutes. The CY27H512 needs to be within 1 inch of the lamp during erasure. Permanent damage may result if the EPROM is exposed to high-intensity UV light for an extended period of time. 7258 Wsec/cm^2 is the recommended maximum dosage.

Programming Modes

Programming support is available from Cypress as well as from a number of third-party software vendors. For detailed programming information, including a listing of software packages, please see the PROM Programming Information located at the end of this section. Programming algorithms can be obtained from any Cypress representative.

Table 1. Programming Electrical Characteristics

Parameter	Description	Min.	Max.	Unit
V_{PP}	Programming Power Supply	12.5	13	V
I_{PP}	Programming Supply Current		50	mA
V_{IHP}	Programming Input Voltage HIGH	3.0	V_{CC}	V
V_{ILP}	Programming Input Voltage LOW	−0.5	0.4	V
V_{CCP}	Programming VCC	6.0	6.5	V

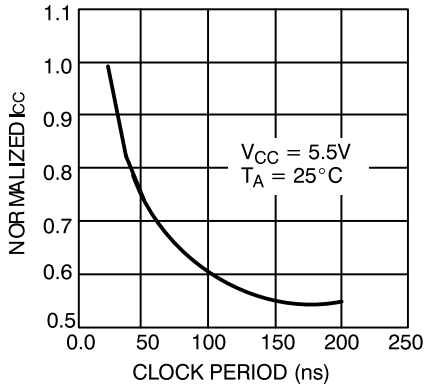
Table 2. Mode Selection

Mode	Pin Function[8]				
	$\overline{CE}$	$\overline{OE}/V_{PP}$	A_0	A_9	Data
Read	V_{IL}	V_{IL}	A_0	A_9	$O_7 - O_0$
Output Disable	X	V_{IH}	A_0	A_9	High Z
Stand-by	V_{IH}	X	X	X	High Z
Program	V_{ILP}	V_{PP}	A_0	A_9	$D_7 - D_0$
Program Verify	V_{ILP}	V_{ILP}	A_0	A_9	$O_7 - O_0$
Program Inhibit	V_{IHP}	V_{PP}	A_0	A_9	High Z
Signature Read (MFG)	V_{IL}	V_{IL}	V_{IL}	V_{HV}[9]	34H
Signature Read (DEV)	V_{IL}	V_{IL}	V_{IH}	V_{HV}[9]	1FH

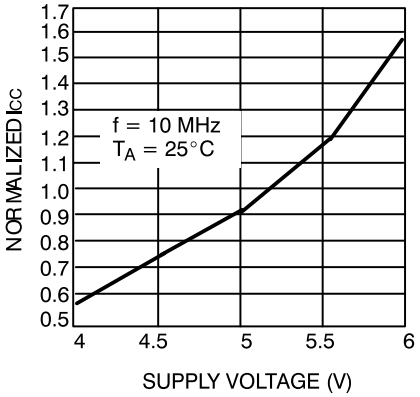
Note:
8. X can be V_{IL} or V_{IH}.
9. V_{HV}=12±0.5V

Typical DC and AC Characteristics

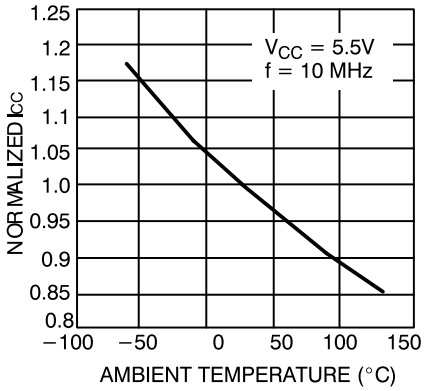
NORMALIZED SUPPLY CURRENT vs. CYCLE PERIOD



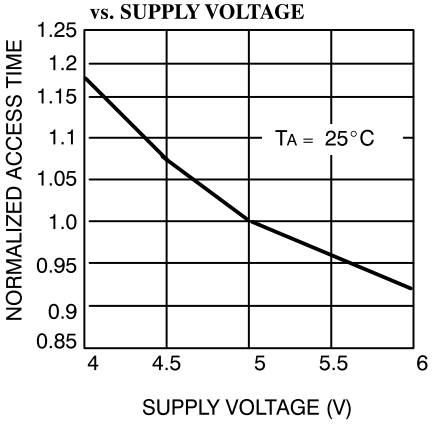
NORMALIZED SUPPLY CURRENT vs. SUPPLY VOLTAGE



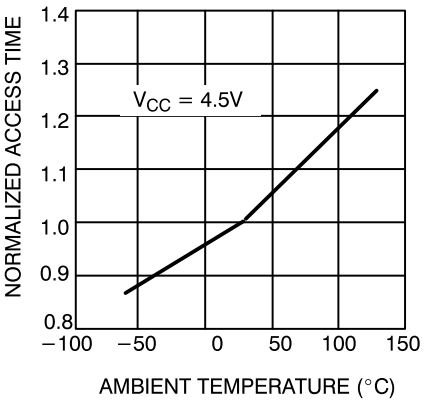
OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE



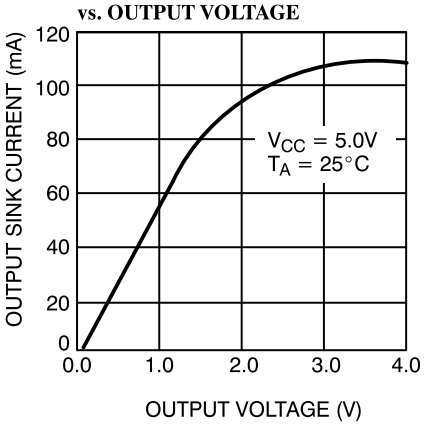
NORMALIZED ACCESS TIME vs. SUPPLY VOLTAGE



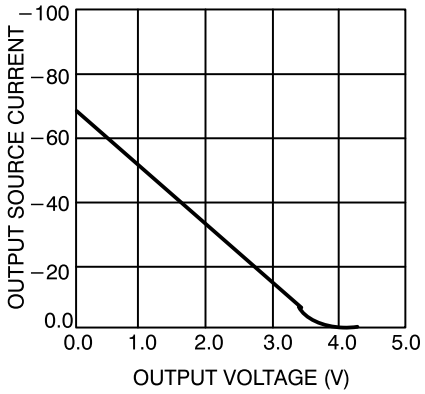
NORMALIZED ACCESS TIME vs. AMBIENT TEMPERATURE



OUTPUT SINK CURRENT vs. OUTPUT VOLTAGE



OUTPUT SOURCE CURRENT vs. OUTPUT VOLTAGE



Ordering Information[10]

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
25	CY27H512−25HC	H65	32-Pin Windowed Leaded Chip Carrier	Commercial
	CY27H512−25JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY27H512−25ZC	Z28	28-Lead Thin Small Outline Package	
30	CY27H512−30HC	H65	32-Pin Windowed Leaded Chip Carrier	Commercial
	CY27H512−30JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY27H512−30PC	P15	28-Lead (600-Mil) Molded DIP	
	CY27H512−30WC	W16	28-Lead (600-Mil) Windowed CerDIP	
	CY27H512−30ZC	Z28	28-Lead Thin Small Outline Package	
35	CY27H512−35HC	H65	32-Pin Windowed Leaded Chip Carrier	Commercial
	CY27H512−35JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY27H512−35PC	P15	28-Lead (600-Mil) Molded DIP	
	CY27H512−35WC	W16	28-Lead (600-Mil) Windowed CerDIP	
	CY27H512−35ZC	Z28	28-Lead Thin Small Outline Package	
	CY27H512−35HMB	H65	32-Pin Windowed Leaded Chip Carrier	Military
	CY27H512−35LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
	CY27H512−35QMB	Q55	32-Pin Windowed Rectangular Leadless Chip Carrier	
45	CY27H512−45HC	H65	32-Pin Windowed Leaded Chip Carrier	Commercial
	CY27H512−45JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY27H512−45PC	P15	28-Lead (600-Mil) Molded DIP	
	CY27H512−45WC	W16	28-Lead (600-Mil) Windowed CerDIP	
	CY27H512−45ZC	Z28	28-Lead Thin Small Outline Package	
	CY27H512−45DMB	D16	28-Lead (600-Mil) CerDIP	Military
	CY27H512−45HMB	H65	32-Pin Windowed Leaded Chip Carrier	
	CY27H512−45LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
	CY27H512−45QMB	Q55	32-Pin Windowed Rectangular Leadless Chip Carrier	
	CY27H512−45WMB	W16	28-Lead (600-Mil) Windowed CerDIP	
55	CY27H512−55HC	H65	32-Pin Windowed Leaded Chip Carrier	Commercial
	CY27H512−55JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY27H512−55PC	P15	28-Lead (600-Mil) Molded DIP	
	CY27H512−55WC	W16	28-Lead (600-Mil) Windowed CerDIP	
	CY27H512−55ZC	Z28	28-Lead Thin Small Outline Package	
	CY27H512−55DMB	D16	28-Lead (600-Mil) CerDIP	Military
	CY27H512−55HMB	H65	32-Pin Windowed Leaded Chip Carrier	
	CY27H512−55LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
	CY27H512−55QMB	Q55	32-Pin Windowed Rectangular Leadless Chip Carrier	
	CY27H512−55WMB	W16	28-Lead (600-Mil) Windowed CerDIP	

Notes:
10. Most of the above products are available in industrial temperature range. Contact a Cypress representative for specifications and product availability.

Ordering Information[10] (continued)

Speed (ns)	Ordering Code	Package Name	Package Type	Operating Range
70	CY27H512−70HC	H65	32-Pin Windowed Leaded Chip Carrier	Commercial
	CY27H512−70JC	J65	32-Lead Plastic Leaded Chip Carrier	
	CY27H512−70PC	P15	28-Lead (600-Mil) Molded DIP	
	CY27H512−70WC	W16	28-Lead (600-Mil) Windowed CerDIP	
	CY27H512−70ZC	Z28	28-Lead Thin Small Outline Package	
	CY27H512−70DMB	D16	28-Lead (600-Mil) CerDIP	Military
	CY27H512−70HMB	H65	32-Pin Windowed Leaded Chip Carrier	
	CY27H512−70LMB	L55	32-Pin Rectangular Leadless Chip Carrier	
	CY27H512−70QMB	Q55	32-Pin Windowed Rectangular Leadless Chip Carrier	
	CY27H512−70WMB	W16	28-Lead (600-Mil) Windowed CerDIP	

MILITARY SPECIFICATIONS
Group A Subgroup Testing

DC Characteristics

Parameter	Subgroups
V_{OH}	1, 2, 3
V_{OL}	1, 2, 3
V_{IH}	1, 2, 3
V_{IL}	1, 2, 3
I_{IX}	1, 2, 3
I_{OZ}	1, 2, 3
I_{CC}	1, 2, 3
I_{SB}	1, 2, 3

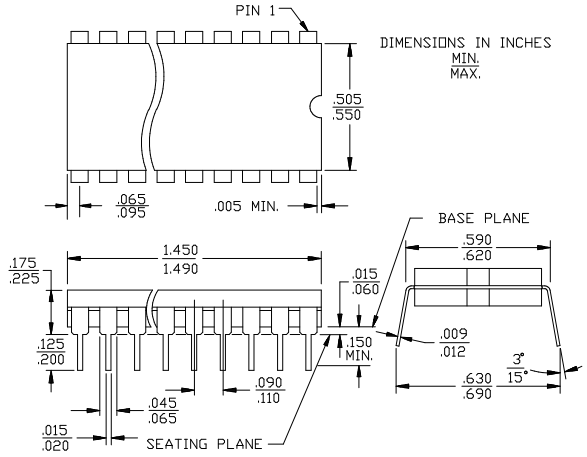
Switching Characteristics

Parameter	Subgroups
t_{AA}	7, 8, 9, 10, 11
t_{OE}	7, 8, 9, 10, 11
t_{CE}	7, 8, 9, 10, 11

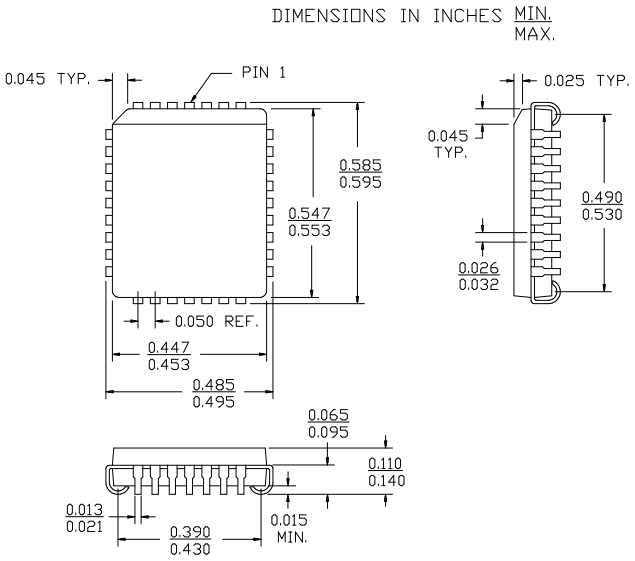
Document #: 38−00422

Package Diagrams (continued)

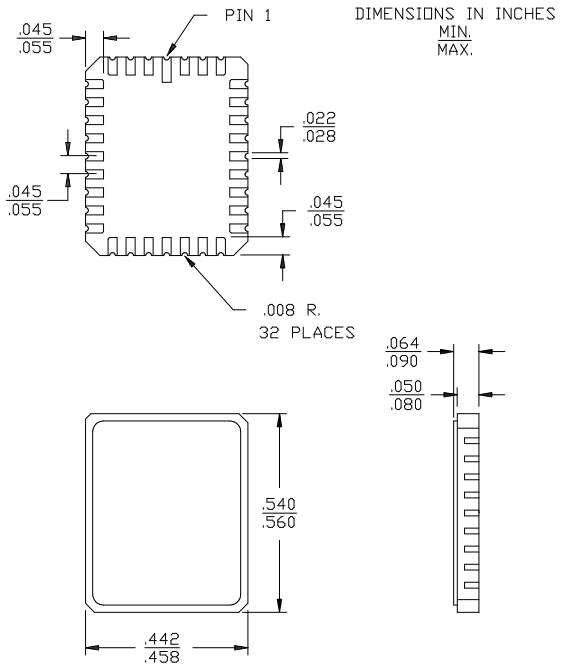
28-Lead (600-Mil) CerDIP D16
MIL−STD−1835 D−10 Config. A



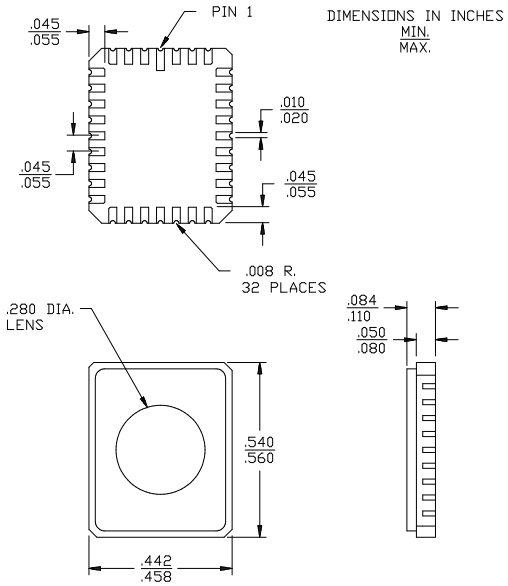
32-Lead Plastic Leaded Chip Carrier J65



32-Pin Rectangular Leadless Chip Carrier L55
MIL−STD−1835 C−12

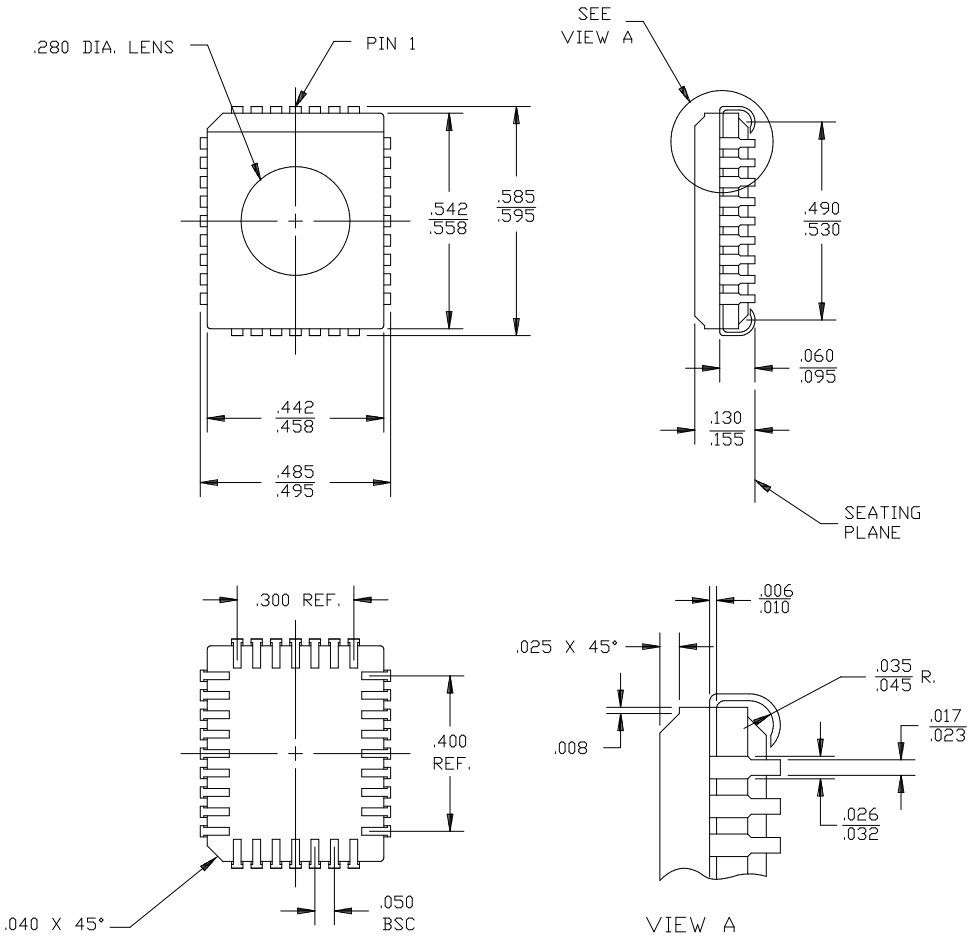


32-Pin Windowed Rectangular Leadless Chip Carrier Q55
MIL−STD−1835 C−12

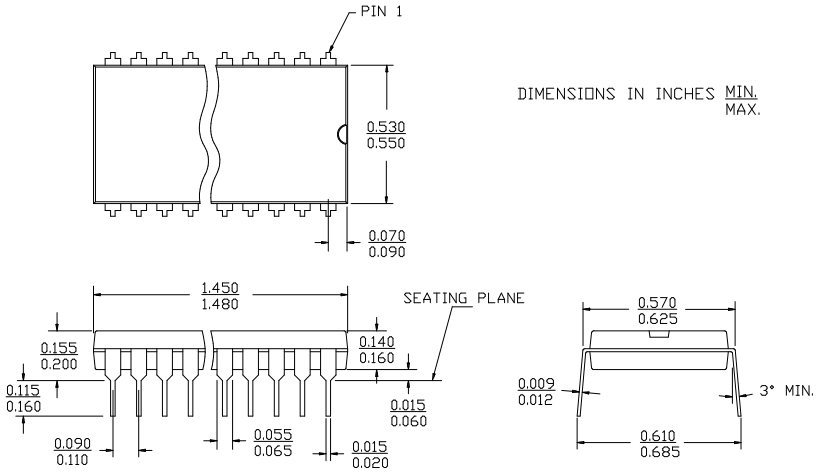


Package Diagrams

32-Pin Windowed Leaded Chip Carrier H65

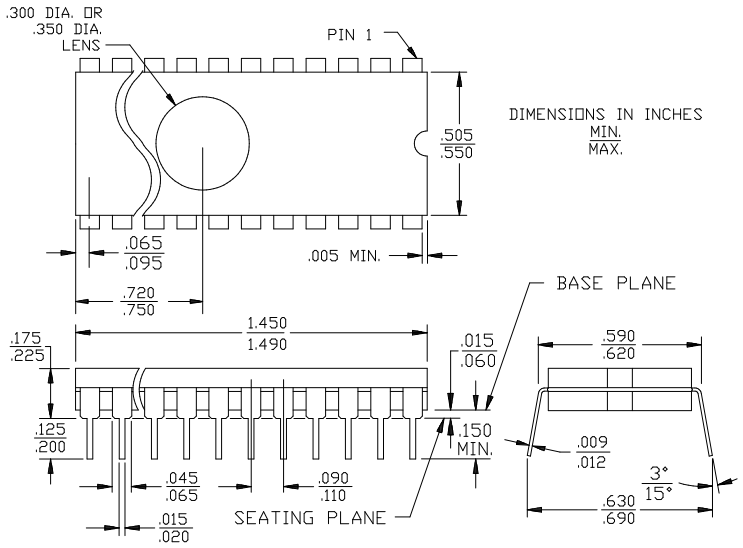


28-Lead (600-Mil) Molded DIP P15



Package Diagrams

28-Lead (600-Mil) Windowed CerDIP W16
MIL−STD−1835 D−10 Config. A



28-Lead Thin Small Outline Package Z28