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FEATURES

- 50ps output-to-output skew
- Synchronous enable/disable
- Multiplexed clock input
- 75KΩ internal input pull-down resistors
- Available in 16-pin SOIC package

Precision Edge™

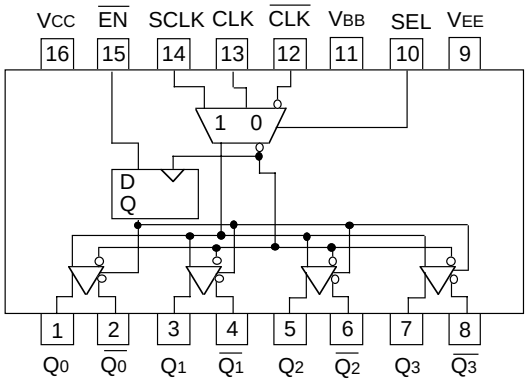
DESCRIPTION

The SY10/100EL15 are low skew 1:4 clock distribution chips designed explicitly for low skew clock distribution applications. The device can be driven by either a differential or single-ended ECL or, if positive power supplies are used, PECL input signal. If a single-ended input is to be used the V_{BB} output should be connected to the $\overline{CLK}$ input and bypassed to V_{CC} via a 0.01µF capacitor. The V_{BB} output is designed to act as the switching reference for the input of the EL15 under single-ended input conditions, as a result this pin can only source/sink up to 0.5mA of current.

The EL15 features a multiplexed clock input to allow for the distribution of a lower speed scan or test clock along with the high speed system clock. When LOW (or left open and pulled LOW by the input pull-down resistor) the SEL pin will select the differential clock input.

The common enable ($\overline{EN}$) is synchronous so that the outputs will only be enabled/disabled when they are already in the LOW state. This avoids any chance of generating a runt clock pulse when the device is enabled/disabled as can happen with an asynchronous control. The internal flip flop is clocked on the falling edge of the input clock, therefore all associated specification limits are referenced to the negative edge of the clock input.

PIN CONFIGURATION/BLOCK DIAGRAM



SOIC
TOP VIEW

PIN NAMES

Pin	Function
CLK	Differential Clock Inputs
SCLK	Synchronous Clock Input
$\overline{EN}$	Synchronous Enable
SEL	Clock Select Input
V_{BB}	Reference Output
Q_{0-3}	Differential Clock Outputs

TRUTH TABLE

CLK	SCLK	SEL	$\overline{EN}$	Q
L	X	L	L	L
H	X	L	L	H
X	L	H	L	L
X	H	H	L	H
X	X	X	H	L*

* On next negative transition of CLK or SCLK

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ABSOLUTE MAXIMUM RATINGS[1]

Symbol	Rating	Value	Unit
V_{EE}	Power Supply (V_{CC} = 0V)	–8.0 to 0	VDC
V_I	Input Voltage (V_{CC} = 0V)	0 to –6.0	VDC
I_{OUT}	Output Current –Continuous –Surge	 50 100	mA
T_A	Operating Temperature Range	–40 to +85	°C
V_{EE}	Operating Range[1],[2]	–5.7 to –4.2	V

NOTES:

1. Absolute maximum rating, beyond which, device life may be impaired, unless otherwise specified on an individual data sheet.
2. Parametric values specified at: 100EL15 Series: –4.2V to –5.5V.
   10EL15 Series –4.75V to –5.5V.

10EL DC ELECTRICAL CHARACTERISTICS

V_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = GND[1]

		T_A = –40°C		T_A = 0°C		T_A = +25°C			T_A = +85°C		
Symbol	Parameter	Min.	Max.	Min.	Max.	Min.	Typ.	Max.	Min.	Max.	Unit
V_{OH}	Output HIGH Voltage	–1080	–890	–1020	–840	–980	—	–810	–910	–720	mV
V_{OL}	Output LOW Voltage	–1950	–1650	–1950	–1630	–1950	—	–1630	–1950	–1595	mV
V_{IH}	Input HIGH Voltage	–1230	–890	–1170	–840	–1130	—	–810	–1060	–720	mV
V_{IL}	Input LOW Voltage	–1950	–1500	–1950	–1480	–1950	—	–1480	–1950	–1445	mV
I_{IH}	Input High Current	—	150	—	150	—	—	150	—	150	µA
I_{IL}	Input LOW Current	0.5	—	0.5	—	0.5	—	—	0.5	—	µA
I_{EE}	Power Supply Current	—	35	—	35	—	25	35	—	38	mA
V_{BB}	Output Reference Voltage	–1.38	–1.26	–1.38	–1.26	–1.38	—	–1.26	–1.38	–1.26	V

NOTE:

1. 10EL circuits are designed to meet the DC specifications shown in the table after thermal equilibrium has been established. The circuit is in a test socket or mounted on a printed circuit board and transverse airflow greater than 500lfpm is maintained. Outputs are terminated through a 50Ω resistor to –2.0V except where otherwise specified on the individual data sheets.

PRODUCT ORDERING CODE

Ordering Code	Package Type	Operating Range	Marking Code
SY10EL15ZC	Z16-2	Commercial	HEL15
SY10EL15ZCTR*	Z16-2	Commercial	HEL15
SY100EL15ZC	Z16-2	Commercial	XEL15
SY100EL15ZCTR*	Z16-2	Commercial	XEL15

*Tape and Reel

Ordering Code	Package Type	Operating Range	Marking Code
SY10EL15ZI[1]	Z16-2	Industrial	HEL15
SY10EL15ZITR*[1]	Z16-2	Industrial	HEL15
SY100EL15ZI[1]	Z16-2	Industrial	XEL15
SY100EL15ZITR*[1]	Z16-2	Industrial	XEL15

*Tape and Reel

Note 1. Recommended for new designs.

100EL DC ELECTRICAL CHARACTERISTICS

V_{EE} = V_{EE} (Min.) to V_{EE} (Max.); V_{CC} = GND[1]

Symbol	Parameter	T_A = –40°C		T_A = 0°C		T_A = +25°C			T_A = +85°C		Unit
		Min.	Max.	Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
V_{OH}	Output HIGH Voltage[2]	–1085	–880	–1025	–880	–1025	–955	–880	–1025	–880	mV
V_{OL}	Output LOW Voltage[2]	–1830	–1555	–1810	–1620	–1810	–1705	–1620	–1810	–1620	mV
V_{OHA}	Output HIGH Voltage[3]	–1095	—	–1035	—	–1035	—	—	–1035	—	mV
V_{OLA}	Output LOW Voltage[3]	—	–1555	—	–1610	—	—	–1610	—	–1610	mV
V_{IH}	Input HIGH Voltage	–1165	–880	–1165	–880	–1165	—	–880	–1165	–880	mV
V_{IL}	Input LOW Voltage	–1810	–1475	–1810	–1475	–1810	—	–1475	–1810	–1475	mV
I_{IH}	Input High Current	—	150	—	150	—	—	150	—	150	µA
I_{IL}	Input LOW Current[4]	0.5	—	0.5	—	0.5	—	—	0.5	—	µA
I_{EE}	Power Supply Current	—	35	—	35	—	25	35	—	38	mA
V_{BB}	Output Reference Voltage	–1.38	–1.26	–1.38	–1.26	–1.38	—	–1.26	–1.38	–1.26	V

NOTES:

1. This table replaces the three traditionally seen in ECL 100K data books. The same DC parameter values at V_{EE} = –4.5V now apply across the full V_{EE} range of –4.2V to –5.5V. Outputs are terminated through a 50Ω resistor to –2.0V except where otherwise specified on the individual data sheets.
2. V_{IN} = V_{IH}(Max) or V_{IL}(Min).
3. V_{IN} = V_{IH}(Min) or V_{IL}(Max).
4. V_{IN} = V_{IL}(Max).

AC ELECTRICAL CHARACTERISTICS

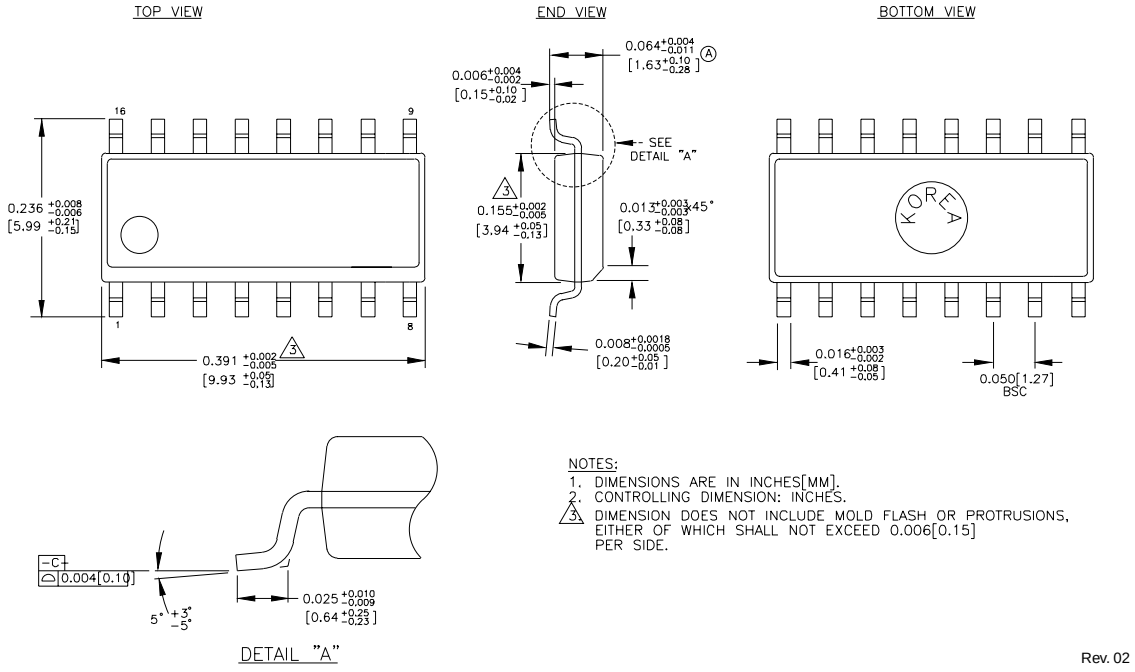
V_{EE} = V_{EE} (Min) to V_{EE} (Max); V_{CC} = GND

Symbol	Parameter	T_A = –40°C		T_A = 0°C		T_A = +25°C			T_A = +85°C		Unit
		Min.	Max.	Min.	Max.	Min.	Typ.	Max.	Min.	Max.	
t_{PLH} t_{PHL}	Propagation Delay CLK to Q (Diff) CLK to Q (SE) SCLK to Q	 460 410 410	 660 710 710	 470 420 420	 670 720 720	 470 420 420	 — — —	 670 720 720	 500 450 470	 700 750 750	ps
t_{skew}	Part-to-Part Skew[1] Within-Device Skew	— —	200 50	— —	200 50	— —	— —	200 50	— —	200 50	ps
t_S	Setup Time $\overline{EN}$	150	—	150	—	150	—	—	150	—	ps
t_H	Hold Time $\overline{EN}$	400	—	400	—	400	—	—	400	—	ps
V_{PP}	Minimum Input CLK Swing	250	—	250	—	250	—	—	250	—	mV
V_{CMR}	Common Mode CLK Range	–2.0	–0.4	–2.0	–0.4	–2.0	—	–0.4	–2.0	–0.4	V
t_r t_f	Output Rise/Fall Times Q (20% – 80%)	—	—	325	575	325	—	575	325	575	ps

NOTE:

1. Skews are specified for identical LOW-to-HIGH or HIGH-to-LOW transitions.

16 LEAD SOIC .150" WIDE (Z16-2)



Rev. 02

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