

- Control Inputs V_{IH}/V_{IL} Levels are Referenced to V_{CCA} Voltage
- V_{CC} Isolation Feature – If Either V_{CC} Input Is at GND, Both Ports Are in the High-Impedance State
- Overvoltage-Tolerant Inputs/Outputs Allow Mixed-Voltage-Mode Data Communications
- Fully Configurable Dual-Rail Design Allows Each Port to Operate Over the Full 1.2-V to 3.6-V Power-Supply Range
- I_{off} Supports Partial-Power-Down Mode Operation
- I/Os Are 4.6-V Tolerant
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Max Data Rates
 - 380 Mbps (1.8-V to 3.3-V Translation)
 - 260 Mbps (<1.8-V to 3.3-V Translation)
 - 260 Mbps (Translate to 2.5 V)
 - 210 Mbps (Translate to 1.8 V)
 - 120 Mbps (Translate to 1.5 V)
 - 100 Mbps (Translate to 1.2 V)
- Latch-Up Performance Exceeds 100 mA Per JESD 78, Class II
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)
 - 1000-V Charged-Device Model (C101)

DGG OR DGV PACKAGE
(TOP VIEW)

1DIR	1	56	1OE
1B1	2	55	1A1
1B2	3	54	1A2
GND	4	53	GND
1B3	5	52	1A3
1B4	6	51	1A4
V_{CCB}	7	50	V_{CCA}
1B5	8	49	1A5
1B6	9	48	1A6
1B7	10	47	1A7
GND	11	46	GND
1B8	12	45	1A8
1B9	13	44	1A9
1B10	14	43	1A10
2B1	15	42	2A1
2B2	16	41	2A2
2B3	17	40	2A3
GND	18	39	GND
2B4	19	38	2A4
2B5	20	37	2A5
2B6	21	36	2A6
V_{CCB}	22	35	V_{CCA}
2B7	23	34	2A7
2B8	24	33	2A8
GND	25	32	GND
2B9	26	31	2A9
2B10	27	30	2A10
2DIR	28	29	2OE

description/ordering information

This 20-bit noninverting bus transceiver uses two separate configurable power-supply rails. The SN74AVCH20T245 is optimized to operate with V_{CCA}/V_{CCB} set at 1.4 V to 3.6 V. It is operational with V_{CCA}/V_{CCB} as low as 1.2 V. The A port is designed to track V_{CCA} . V_{CCA} accepts any supply voltage from 1.2 V to 3.6 V. The B port is designed to track V_{CCB} . V_{CCB} accepts any supply voltage from 1.2 V to 3.6 V. This allows for universal low-voltage bidirectional translation between any of the 1.2-V, 1.5-V, 1.8-V, 2.5-V, and 3.3-V voltage nodes.

ORDERING INFORMATION

T_A	PACKAGE†		ORDERABLE PART NUMBER	TOP-SIDE MARKING
–40°C to 85°C	TSSOP – DGG	Tape and reel	SN74AVCH20T245GR	AVCH20T245
	TVSOP – DGV	Tape and reel	SN74AVCH20T245VR	WK245
	VFBGA – GQL	Tape and reel	SN74AVCH20T245KR	WK245
	VFBGA – ZQL (Pb-free)		74AVCH20T245ZQLR	

† Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



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SN74AVCH20T245

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description/ordering information (continued)

The SN74AVCH20T245 is designed for asynchronous communication between data buses. The device transmits data from the A bus to the B bus or from the B bus to the A bus, depending on the logic level at the direction-control (DIR) input. The output-enable ($\overline{OE}$) input can be used to disable the outputs so that the buses are effectively isolated.

The SN74AVCH20T245 is designed so that the control (1DIR, 2DIR, $1\overline{OE}$, and $2\overline{OE}$) inputs are supplied by V_{CCA} .

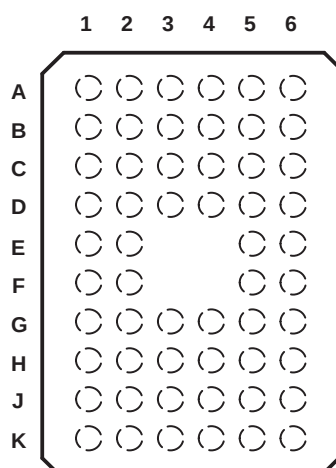
This device is fully specified for partial-power-down applications using I_{off} . The I_{off} circuitry disables the outputs, preventing damaging current backflow through the device when it is powered down.

The V_{CC} isolation feature ensures that if either V_{CC} input is at GND, both outputs are in the high-impedance state. The bus-hold circuitry on the powered-up side always stays active.

Active bus-hold circuitry holds unused or undriven inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

To ensure the high-impedance state during power up or power down, $\overline{OE}$ should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

GQL OR ZQL PACKAGE (TOP VIEW)



terminal assignments

	1	2	3	4	5	6
A	1B1	1B2	1DIR	$1\overline{OE}$	1A2	1A1
B	1B3	1B4	GND	GND	1A4	1A3
C	1B5	1B6	V_{CCB}	V_{CCA}	1A6	1A5
D	1B7	1B8	GND	GND	1A8	1A7
E	1B9	1B10			1A10	1A9
F	2B1	2B2			2A2	2A1
G	2B3	2B4	GND	GND	2A4	2A3
H	2B5	2B6	V_{CCB}	V_{CCA}	2A6	2A5
J	2B7	2B8	GND	GND	2A8	2A7
K	2B9	2B10	2DIR	$2\overline{OE}$	2A10	2A9

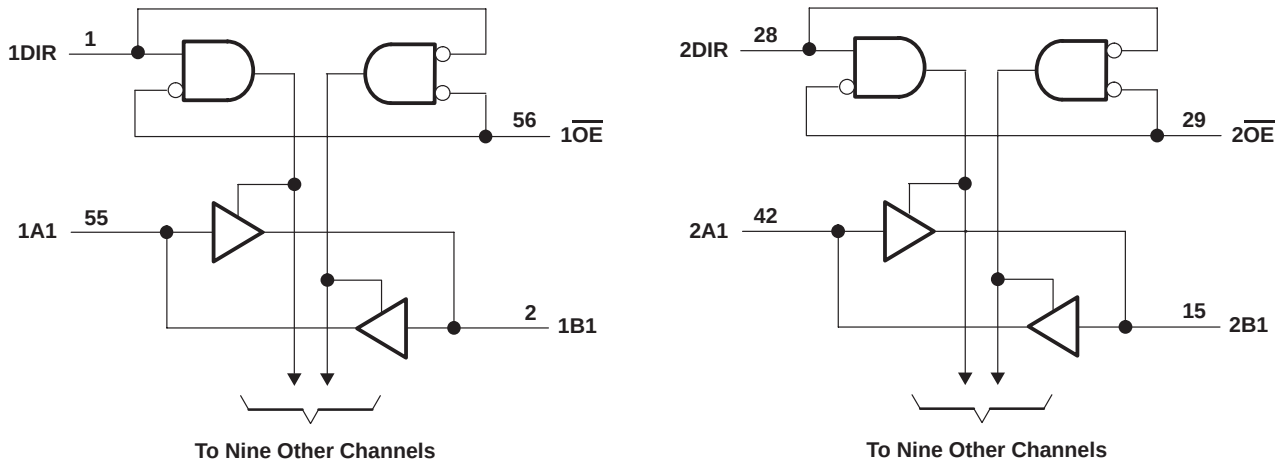
FUNCTION TABLE (each 10-bit section)

INPUTS		OPERATION
$\overline{OE}$	DIR	
L	L	B data to A bus
L	H	A data to B bus
H	X	Isolation

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logic diagram (positive logic)



Pin numbers shown are for the DGG and DGV packages.

absolute maximum ratings over operating free-air temperature range (unless otherwise noted)[†]

Supply voltage range, V_{CCA} and V_{CCB}	–0.5 V to 4.6 V
Input voltage range, V_I (see Note 1): I/O ports (A port)	–0.5 V to 4.6 V
I/O ports (B port)	–0.5 V to 4.6 V
Control inputs	–0.5 V to 4.6 V
Voltage range applied to any output in the high-impedance or power-off state, V_O	
(see Note 1): (A port)	–0.5 V to 4.6 V
(B port)	–0.5 V to 4.6 V
Voltage range applied to any output in the high or low state, V_O	
(see Notes 1 and 2): (A port)	–0.5 V to $V_{CCA} + 0.5$ V
(B port)	–0.5 V to $V_{CCB} + 0.5$ V
Input clamp current, I_{IK} ($V_I < 0$)	–50 mA
Output clamp current, I_{OK} ($V_O < 0$)	–50 mA
Continuous output current, I_O	±50 mA
Continuous current through each V_{CCA} , V_{CCB} , and GND	±100 mA
Package thermal impedance, θ_{JA} (see Note 3): DGG package	64°C/W
DGV package	48°C/W
GQL/ZQL package	42°C/W
Storage temperature range, T_{stg}	–65°C to 150°C

[†] Stresses beyond those listed under “absolute maximum ratings” may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “recommended operating conditions” is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

- NOTES: 1. The input voltage and output negative-voltage ratings may be exceeded if the input and output current ratings are observed.
2. The output positive-voltage rating may be exceeded up to 4.6 V maximum if the output current rating is observed.
3. The package thermal impedance is calculated in accordance with JESD 51-7.

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recommended operating conditions (see Notes 4 through 8)

			V _{CCI}	V _{CCO}	MIN	MAX	UNIT
V _{CCA}	Supply voltage				1.2	3.6	V
V _{CCB}	Supply voltage				1.2	3.6	V
V _{IH}	High-level input voltage	Data inputs (see Note 7)	1.2 V to 1.95 V		V _{CCI} ×0.65		V
			1.95 V to 2.7 V		1.6		
			2.7 V to 3.6 V		2		
V _{IL}	Low-level input voltage	Data inputs (see Note 7)	1.2 V to 1.95 V		V _{CCI} × 0.35		V
			1.95 V to 2.7 V		0.7		
			2.7 V to 3.6 V		0.8		
V _{IH}	High-level input voltage	DIR (Referenced to V _{CCA}) (see Note 8)	1.2 V to 1.95 V		V _{CCA} ×0.65		V
			1.95 V to 2.7 V		1.6		
			2.7 V to 3.6 V		2		
V _{IL}	Low-level input voltage	DIR (Referenced to V _{CCA}) (see Note 8)	1.2 V to 1.95 V		V _{CCA} ×0.35		V
			1.95 V to 2.7 V		0.7		
			2.7 V to 3.6 V		0.8		
V _I	Input voltage				0	3.6	V
V _O	Output voltage	Active state			0	V _{CCO}	V
		3-state			0	3.6	
I _{OH}	High-level output current			1.2 V	−3		mA
				1.4 V to 1.6 V	−6		
				1.65 V to 1.95 V	−8		
				2.3 V to 2.7 V	−9		
				3 V to 3.6 V	−12		
I _{OL}	Low-level output current			1.2 V	3		mA
				1.4 V to 1.6 V	6		
				1.65 V to 1.95 V	8		
				2.3 V to 2.7 V	9		
				3 V to 3.6 V	12		
Δt/Δv	Input transition rise or fall rate				5		ns/V
T _A	Operating free-air temperature				−40	85	°C

NOTES: 4. V_{CCI} is the V_{CC} associated with the data input port.5. V_{CCO} is the V_{CC} associated with the output port.6. All unused data inputs of the device must be held at V_{CCI} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.7. For V_{CCI} values not specified in the data sheet, V_{IH(min)} = V_{CCI} × 0.7 V, V_{IL(max)} = V_{CCI} × 0.3 V.8. For V_{CCI} values not specified in the data sheet, V_{IH(min)} = V_{CCA} × 0.7 V, V_{IL(max)} = V_{CCA} × 0.3 V.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Note 9)

PARAMETER		TEST CONDITIONS		V _{CCA}	V _{CCB}	T _A = 25°C			–40°C to 85°C		UNIT
						MIN	TYP	MAX	MIN	MAX	
V _{OH}	I _{OH} = –100 μA	V _I = V _{IH}	1.2 V to 3.6 V	1.2 V to 3.6 V				V _{CCO} – 0.2 V		V	
	I _{OH} = –3 mA		1.2 V	1.2 V	0.95						
	I _{OH} = –6 mA		1.4 V	1.4 V				1.05			
	I _{OH} = –8 mA		1.65 V	1.65 V				1.2			
	I _{OH} = –9 mA		2.3 V	2.3 V				1.75			
	I _{OH} = –12 mA		3 V	3 V				2.3			
V _{OL}	I _{OL} = 100 μA	V _I = V _{IL}	1.2 V to 3.6 V	1.2 V to 3.6 V				0.2		V	
	I _{OL} = 3 mA		1.2 V	1.2 V	0.15						
	I _{OL} = 6 mA		1.4 V	1.4 V				0.35			
	I _{OL} = 8 mA		1.65 V	1.65 V				0.45			
	I _{OL} = 9 mA		2.3 V	2.3 V				0.55			
	I _{OL} = 12 mA		3 V	3 V				0.7			
I _I	Contr ol inputs	V _I = V _{CCA} or GND	1.2 V to 3.6 V	1.2 V to 3.6 V	±0.025	±0.25		±1	μA		
I _{BHL} [†]	V _I = 0.42 V		1.2 V	1.2 V	25					μA	
	V _I = 0.49 V		1.4 V	1.4 V				15			
	V _I = 0.58 V		1.65 V	1.65 V				25			
	V _I = 0.7 V		2.3 V	2.3 V				45			
	V _I = 0.8 V		3.3 V	3.3 V				100			
I _{BHH} [‡]	V _I = 0.78 V		1.2 V	1.2 V	–25					μA	
	V _I = 0.91 V		1.4 V	1.4 V				–15			
	V _I = 1.07 V		1.65 V	1.65 V				–25			
	V _I = 1.6 V		2.3 V	2.3 V				–45			
	V _I = 2 V		3.3 V	3.3 V				–100			
I _{BHLO} [§]	V _I = 0 to V _{CC}		1.2 V	1.2 V	50					μA	
			1.6 V	1.6 V				125			
			1.95 V	1.95 V				200			
			2.7 V	2.7 V				300			
			3.6 V	3.6 V				500			
I _{BHHO} [¶]	V _I = 0 to V _{CC}		1.2 V	1.2 V	–50					μA	
			1.6 V	1.6 V				–125			
			1.95 V	1.95 V				–200			
			2.7 V	2.7 V				–300			
			3.6 V	3.6 V				–500			

[†] The bus-hold circuit can sink at least the minimum low sustaining current at V_{IL} max. I_{BHL} should be measured after lowering V_{IN} to GND and then raising it to V_{IL} max.

[‡] The bus-hold circuit can source at least the minimum high sustaining current at V_{IH} min. I_{BHH} should be measured after raising V_{IN} to V_{CC} and then lowering it to V_{IH} min.

[§] An external driver must source at least I_{BHLO} to switch this node from low to high.

[¶] An external driver must sink at least I_{BHHO} to switch this node from high to low.

NOTE 9: V_{CCO} is the V_{CC} associated with the output port.

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electrical characteristics over recommended operating free-air temperature range (unless otherwise noted) (see Notes 10 and 11) (continued)

PARAMETER		TEST CONDITIONS		V _{CCA}	V _{CCB}	T _A = 25°C		–40°C to 85°C		UNIT
						MIN	TYP	MAX	MIN	
I _{off}	A port	V _I or V _O = 0 to 3.6 V		0 V	0 to 3.6 V	±0.1	±1	±5		μA
	B port			0 to 3.6 V	0 V	±0.1	±1	±5		
I _{OZ} [†]	A or B ports	V _O = V _{CCO} or GND, V _I = V _{CCI} or GND	$\overline{\text{OE}} = V_{IH}$	3.6 V	3.6 V	±0.5	±2.5	±5		μA
	B port		$\overline{\text{OE}} =$	0 V	3.6 V			±5		
	A port		don't care	3.6 V	0 V			±5		
I _{CCA}		V _I = V _{CCI} or GND, I _O = 0		1.2 V to 3.6 V	1.2 V to 3.6 V			35		μA
				0 V	3.6 V			–5		
				3.6 V	0 V			35		
I _{CCB}		V _I = V _{CCI} or GND, I _O = 0		1.2 V to 3.6 V	1.2 V to 3.6 V			35		μA
				0 V	3.6 V			35		
				3.6 V	0 V			–5		
I _{CCA} + I _{CCB}		V _I = V _{CCI} or GND, I _O = 0		1.2 V to 3.6 V	1.2 V to 3.6 V			65		μA
C _i	Control inputs	V _I = 3.3 V or GND		3.3 V	3.3 V	3.5				pF
C _{io}	A or B ports	V _O = 3.3 V or GND		3.3 V	3.3 V	7				pF

[†] For I/O ports, the parameter I_{OZ} includes the input leakage current.

NOTES: 10. V_{CCO} is the V_{CC} associated with the output port.

11. V_{CCI} is the V_{CC} associated with the input port.

switching characteristics over recommended operating free-air temperature range,
V_{CCA} = 1.2 V (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	V _{CCB} = 1.2 V	V _{CCB} = 1.5 V	V _{CCB} = 1.8 V	V _{CCB} = 2.5 V	V _{CCB} = 3.3 V	UNIT
			TYP	TYP	TYP	TYP	TYP	
t _{PLH}	A	B	3.8	3.1	2.8	2.7	3.3	ns
t _{PHL}			3.8	3.1	2.8	2.7	3.3	
t _{PLH}	B	A	4.1	3.8	3.6	3.5	3.4	ns
t _{PHL}			4.1	3.8	3.6	3.5	3.4	
t _{PZH}	$\overline{\text{OE}}$	A	6.5	6.5	6.5	6.5	6.5	ns
t _{PZL}			6.5	6.5	6.5	6.5	6.5	
t _{PZH}	$\overline{\text{OE}}$	B	5.6	4.4	3.8	3.3	3.2	ns
t _{PZL}			5.6	4.4	3.8	3.3	3.2	
t _{PHZ}	$\overline{\text{OE}}$	A	6.4	6.4	6.4	6.4	6.4	ns
t _{PLZ}			6.4	6.4	6.4	6.4	6.4	
t _{PHZ}	$\overline{\text{OE}}$	B	5.7	4.6	4.7	4.1	5.4	ns
t _{PLZ}			5.7	4.6	4.7	4.1	5.4	



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switching characteristics over recommended operating free-air temperature range,
 $V_{CCA} = 1.5 \text{ V} \pm 0.1 \text{ V}$ (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CCB} = 1.2 \text{ V}$	$V_{CCB} = 1.5 \text{ V} \pm 0.1 \text{ V}$		$V_{CCB} = 1.8 \text{ V} \pm 0.15 \text{ V}$		$V_{CCB} = 2.5 \text{ V} \pm 0.2 \text{ V}$		$V_{CCB} = 3.3 \text{ V} \pm 0.3 \text{ V}$		UNIT
			TYP	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	B	3.8	0.5	6.4	0.5	5.4	0.5	4.3	0.5	3.9	ns
t_{PHL}			3.8	0.5	6.4	0.5	5.4	0.5	4.3	0.5	3.9	
t_{PLH}	B	A	3.1	0.5	6.4	0.5	6.1	0.5	5.8	0.5	5.7	ns
t_{PHL}			3.1	0.5	6.4	0.5	6.1	0.5	5.8	0.5	5.7	
t_{PZH}	$\overline{OE}$	A	4.3	1.5	10.3	1.5	10.3	1.5	10.2	1.5	10.2	ns
t_{PZL}			4.3	1.5	10.3	1.5	10.3	1.5	10.2	1.5	10.2	
t_{PZH}	$\overline{OE}$	B	5.2	1	10.3	1	8.4	0.5	6.1	0.5	5.3	ns
t_{PZL}			5.2	1	10.3	1	8.4	0.5	6.1	0.5	5.3	
t_{PHZ}	$\overline{OE}$	A	4.5	2	9	2	9	2	9	2	9	ns
t_{PLZ}			4.5	2	9	2	9	2	9	2	9	
t_{PHZ}	$\overline{OE}$	B	5.1	1.5	9	1.5	7.8	1	6.4	1	5.9	ns
t_{PLZ}			5.1	1.5	9	1.5	7.8	1	6.4	1	5.9	

switching characteristics over recommended operating free-air temperature range,
 $V_{CCA} = 1.8 \text{ V} \pm 0.15 \text{ V}$ (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CCB} = 1.2 \text{ V}$	$V_{CCB} = 1.5 \text{ V} \pm 0.1 \text{ V}$		$V_{CCB} = 1.8 \text{ V} \pm 0.15 \text{ V}$		$V_{CCB} = 2.5 \text{ V} \pm 0.2 \text{ V}$		$V_{CCB} = 3.3 \text{ V} \pm 0.3 \text{ V}$		UNIT
			TYP	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	B	3.6	0.5	6.1	0.5	5	0.5	3.9	0.5	3.5	ns
t_{PHL}			3.6	0.5	6.1	0.5	5	0.5	3.9	0.5	3.5	
t_{PLH}	B	A	2.8	0.5	5.4	0.5	5	0.5	4.7	0.5	4.6	ns
t_{PHL}			2.8	0.5	5.4	0.5	5	0.5	4.7	0.5	4.6	
t_{PZH}	$\overline{OE}$	A	3.4	1	8.1	1	7.9	1	7.9	1	7.9	ns
t_{PZL}			3.4	1	8.1	1	7.9	1	7.9	1	7.9	
t_{PZH}	$\overline{OE}$	B	5	0.5	10	0.5	7.9	0.5	5.7	0.5	4.8	ns
t_{PZL}			5	0.5	10	0.5	7.9	0.5	5.7	0.5	4.8	
t_{PHZ}	$\overline{OE}$	A	4.1	2	7.4	2	7.4	2	7.4	2	7.4	ns
t_{PLZ}			4.1	2	7.4	2	7.4	2	7.4	2	7.4	
t_{PHZ}	$\overline{OE}$	B	4.9	1.5	8.7	1.5	7.4	1	5.8	1	5.1	ns
t_{PLZ}			4.9	1.5	8.7	1.5	7.4	1	5.8	1	5.1	

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switching characteristics over recommended operating free-air temperature range,
 $V_{CCA} = 2.5\text{ V} \pm 0.2\text{ V}$ (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CCB} = 1.2\text{ V}$	$V_{CCB} = 1.5\text{ V} \pm 0.1\text{ V}$		$V_{CCB} = 1.8\text{ V} \pm 0.15\text{ V}$		$V_{CCB} = 2.5\text{ V} \pm 0.2\text{ V}$		$V_{CCB} = 3.3\text{ V} \pm 0.3\text{ V}$		UNIT
			TYP	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	B	3.5	0.5	5.8	0.5	4.7	0.5	3.5	0.5	3	ns
t_{PHL}			3.5	0.5	5.8	0.5	4.7	0.5	3.5	0.5	3	
t_{PLH}	B	A	2.7	0.5	4.3	0.5	3.9	0.5	3.5	0.5	3.4	ns
t_{PHL}			2.7	0.5	4.3	0.5	3.9	0.5	3.5	0.5	3.4	
t_{PZH}	$\overline{OE}$	A	2.5	0.5	5.4	0.5	5.3	0.5	5.2	0.5	5.2	ns
t_{PZL}			2.5	0.5	5.4	0.5	5.3	0.5	5.2	0.5	5.2	
t_{PZH}	$\overline{OE}$	B	4.8	0.5	9.6	0.5	7.6	0.5	5.3	0.5	4.3	ns
t_{PZL}			4.8	0.5	9.6	0.5	7.6	0.5	5.3	0.5	4.3	
t_{PHZ}	$\overline{OE}$	A	3	1.1	5.2	1.1	5.2	1.1	5.2	1.1	5.2	ns
t_{PLZ}			3	1.1	5.2	1.1	5.2	1.1	5.2	1.1	5.2	
t_{PHZ}	$\overline{OE}$	B	4.7	1.2	8.2	1.2	6.9	1	5.3	1	5	ns
t_{PLZ}			4.7	1.2	8.2	1.2	6.9	1	5.3	1	5	

switching characteristics over recommended operating free-air temperature range,
 $V_{CCA} = 3.3\text{ V} \pm 0.3\text{ V}$ (see Figure 1)

PARAMETER	FROM (INPUT)	TO (OUTPUT)	$V_{CCB} = 1.2\text{ V}$	$V_{CCB} = 1.5\text{ V} \pm 0.1\text{ V}$		$V_{CCB} = 1.8\text{ V} \pm 0.15\text{ V}$		$V_{CCB} = 2.5\text{ V} \pm 0.2\text{ V}$		$V_{CCB} = 3.3\text{ V} \pm 0.3\text{ V}$		UNIT
			TYP	MIN	MAX	MIN	MAX	MIN	MAX	MIN	MAX	
t_{PLH}	A	B	3.4	0.5	5.7	0.5	4.6	0.5	3.4	0.5	2.9	ns
t_{PHL}			3.4	0.5	5.7	0.5	4.6	0.5	3.4	0.5	2.9	
t_{PLH}	B	A	3.3	0.5	3.9	0.5	3.5	0.5	3	0.5	2.9	ns
t_{PHL}			3.3	0.5	3.9	0.5	3.5	0.5	3	0.5	2.9	
t_{PZH}	$\overline{OE}$	A	2.2	0.5	4.4	0.5	4.3	0.5	4.2	0.5	4.1	ns
t_{PZL}			2.2	0.5	4.4	0.5	4.3	0.5	4.2	0.5	4.1	
t_{PZH}	$\overline{OE}$	B	4.7	1	9.6	0.5	7.5	0.5	5.1	0.5	4.1	ns
t_{PZL}			4.7	1	9.6	0.5	7.5	0.5	5.1	0.5	4.1	
t_{PHZ}	$\overline{OE}$	A	3.4	0.8	5	0.8	5	0.8	5	0.8	5	ns
t_{PLZ}			3.4	0.8	5	0.8	5	0.8	5	0.8	5	
t_{PHZ}	$\overline{OE}$	B	4.6	1.2	8.1	1.2	6.7	1	5.1	0.8	5	ns
t_{PLZ}			4.6	1.2	8.1	1.2	6.7	1	5.1	0.8	5	

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operating characteristics, $T_A = 25^\circ\text{C}$

PARAMETER			TEST CONDITIONS	$V_{CCA} = V_{CCB} = 1.2\text{ V}$	$V_{CCA} = V_{CCB} = 1.5\text{ V}$	$V_{CCA} = V_{CCB} = 1.8\text{ V}$	$V_{CCA} = V_{CCB} = 2.5\text{ V}$	$V_{CCA} = V_{CCB} = 3.3\text{ V}$	UNIT
				TYP	TYP	TYP	TYP	TYP	
$C_{pdA}^\dagger$	A to B	Outputs Enabled	$C_L = 0$, $f = 10\text{ MHz}$, $t_r = t_f = 1\text{ ns}$	1	1	1	1	2	pF
		Outputs Disabled		1	1	1	1	1	
	B to A	Outputs Enabled		12	13	14	15	16	
		Outputs Disabled		1	1	1	1	1	
$C_{pdB}^\dagger$	A to B	Outputs Enabled	$C_L = 0$, $f = 10\text{ MHz}$, $t_r = t_f = 1\text{ ns}$	13	13	14	15	16	pF
		Outputs Disabled		1	1	1	1	1	
	B to A	Outputs Enabled		1	1	1	2	2	
		Outputs Disabled		1	1	1	1	1	

† Power-dissipation capacitance per transceiver

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power-up considerations

A proper power-up sequence always should be followed to avoid excessive supply current, bus contention, oscillations, or other anomalies. To guard against power-up problems, take the following precautions:

1. Connect ground before any supply voltage is applied.
2. Power up V_{CCA} .
3. V_{CCB} can be ramped up along with or after V_{CCA} .

typical total static power consumption ($I_{CCA} + I_{CCB}$)

TABLE 1

V_{CCB}	V_{CCA}						UNIT
	0 V	1.2 V	1.5 V	1.8 V	2.5 V	3.3 V	
0 V	0	<0.5	<0.5	<0.5	<0.5	<0.5	μA
1.2 V	<0.5	<1	<1	<1	<1	1	
1.5 V	<0.5	<1	<1	<1	<1	1	
1.8 V	<0.5	<1	<1	<1	<1	<1	
2.5 V	<0.5	1	<1	<1	<1	<1	
3.3 V	<0.5	1	<1	<1	<1	<1	

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TYPICAL CHARACTERISTICS

TYPICAL PROPAGATION DELAY (A to B) vs LOAD CAPACITANCE

$T_A = 25^\circ\text{C}$, $V_{CCA} = 1.2\text{ V}$

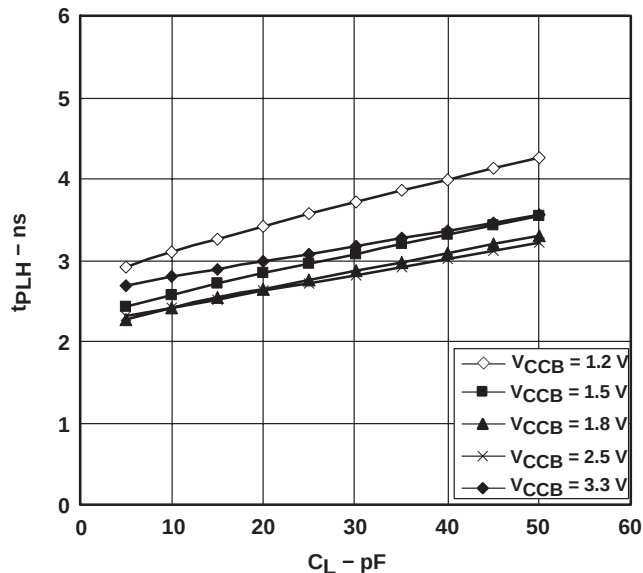


Figure 1

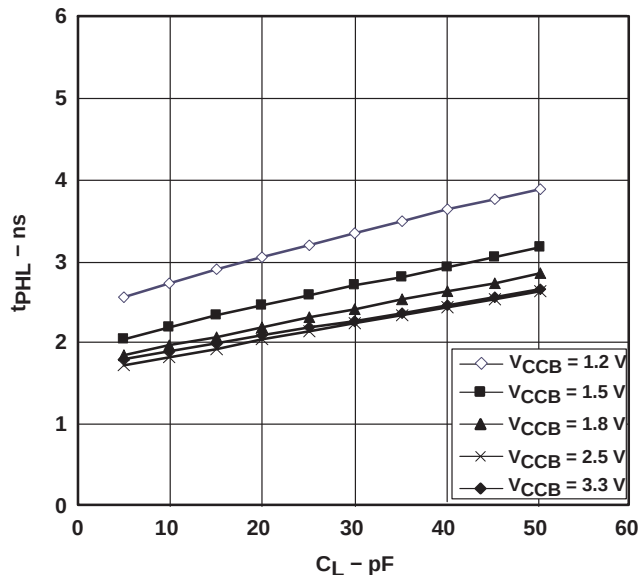


Figure 2

TYPICAL PROPAGATION DELAY (A to B) vs LOAD CAPACITANCE

$T_A = 25^\circ\text{C}$, $V_{CCA} = 1.5\text{ V}$

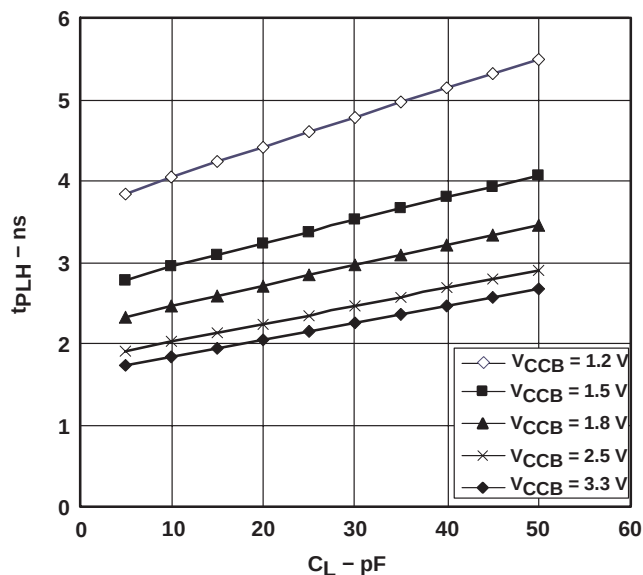


Figure 3

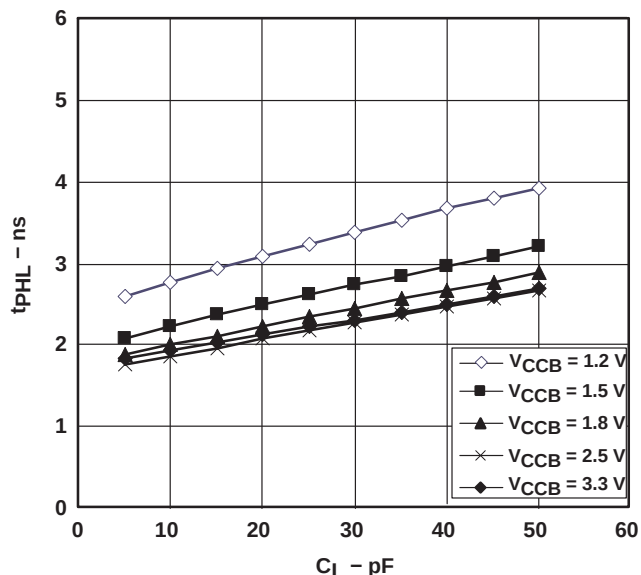


Figure 4

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TYPICAL PROPAGATION DELAY (A to B) vs LOAD CAPACITANCE
 $T_A = 25^\circ\text{C}$, $V_{CCA} = 1.8\text{ V}$

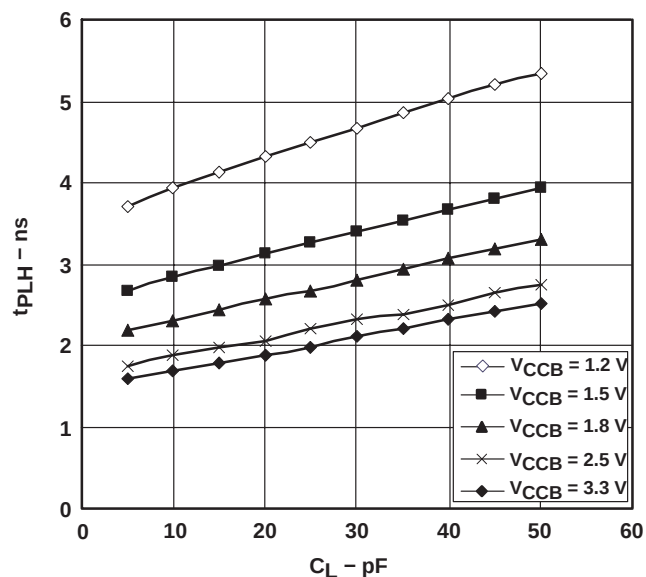


Figure 5

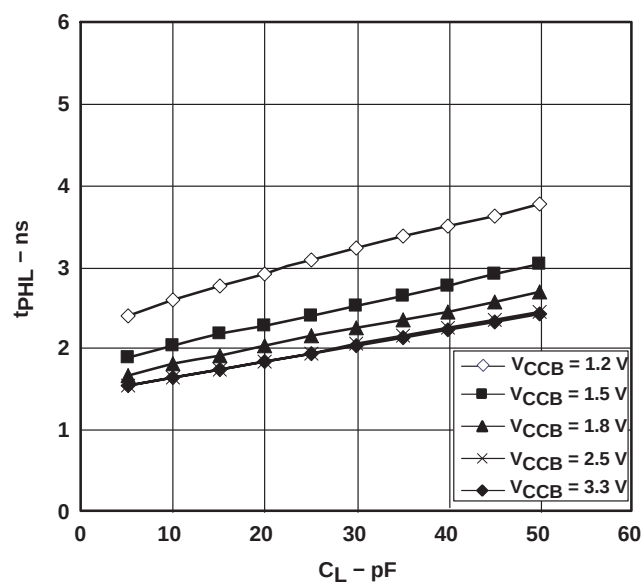


Figure 6

TYPICAL PROPAGATION DELAY (A to B) vs LOAD CAPACITANCE
 $T_A = 25^\circ\text{C}$, $V_{CCA} = 2.5\text{ V}$

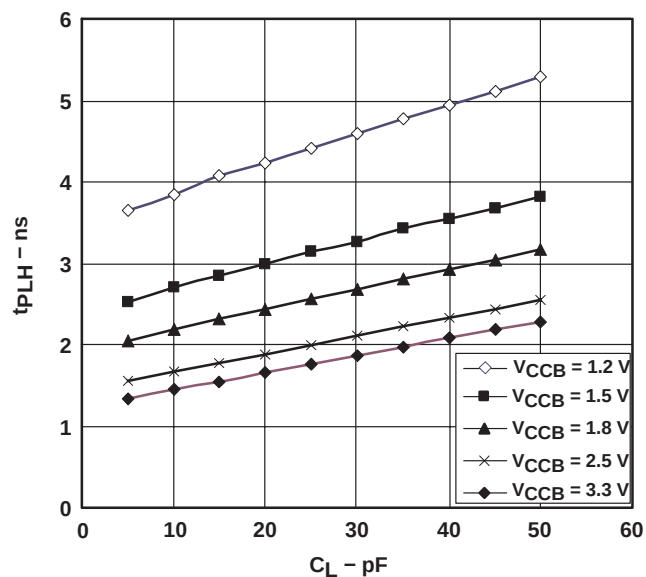


Figure 7

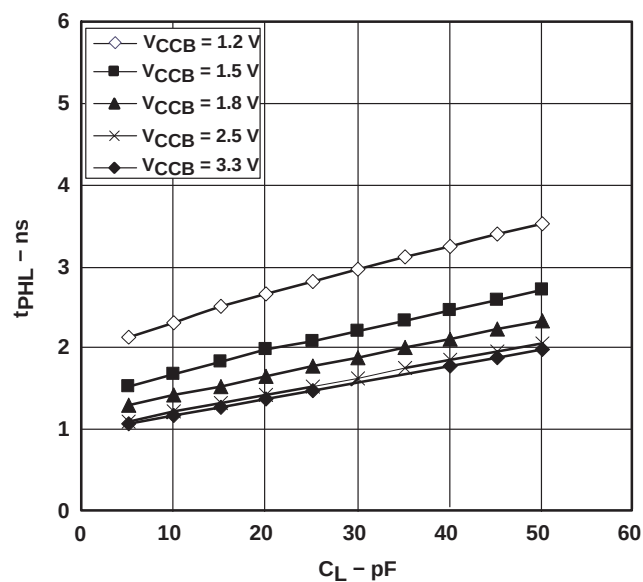


Figure 8

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TYPICAL PROPAGATION DELAY (A to B) vs LOAD CAPACITANCE
 $T_A = 25^\circ\text{C}$, $V_{CCA} = 3.3\text{ V}$

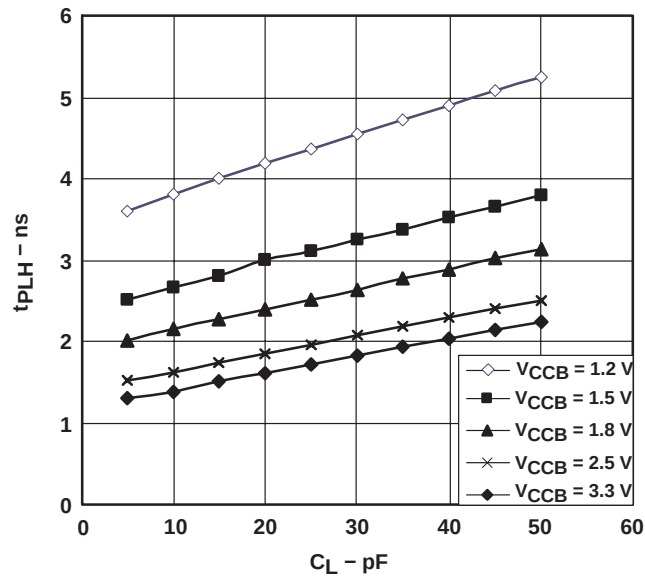


Figure 9

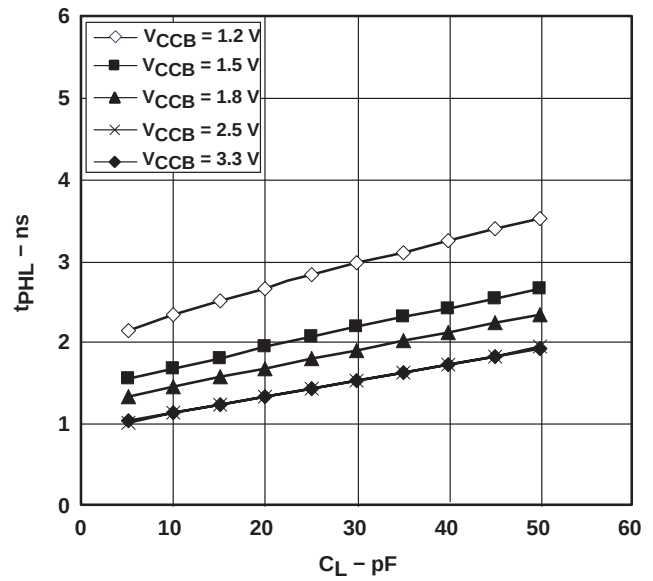


Figure 10

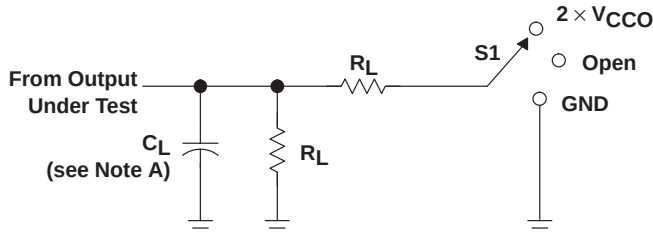
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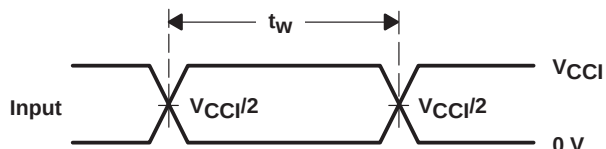
PARAMETER MEASUREMENT INFORMATION



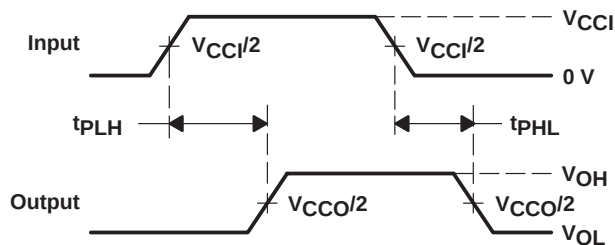
LOAD CIRCUIT

V_{CCO}	C_L	R_L	V_{TP}
1.2 V	15 pF	2 k Ω	0.1 V
1.5 V $\pm$ 0.1 V	15 pF	2 k Ω	0.1 V
1.8 V $\pm$ 0.15 V	15 pF	2 k Ω	0.15 V
2.5 V $\pm$ 0.2 V	15 pF	2 k Ω	0.15 V
3.3 V $\pm$ 0.3 V	15 pF	2 k Ω	0.3 V

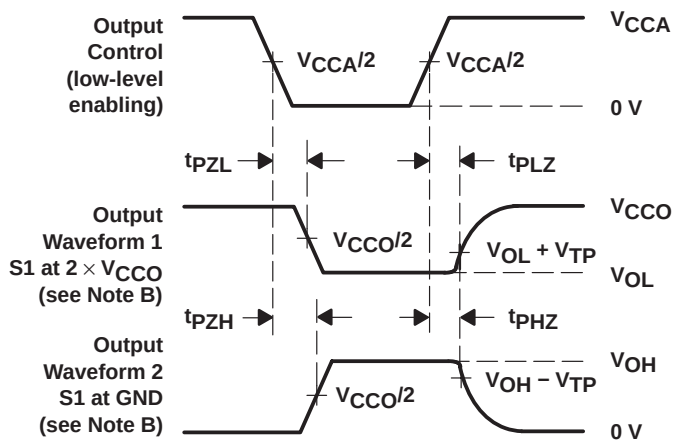
TEST	S1
t_{pd}	Open
t_{PLZ}/t_{PZL}	$2 \times V_{CCO}$
t_{PHZ}/t_{PZH}	GND



VOLTAGE WAVEFORMS
PULSE DURATION



VOLTAGE WAVEFORMS
PROPAGATION DELAY TIMES



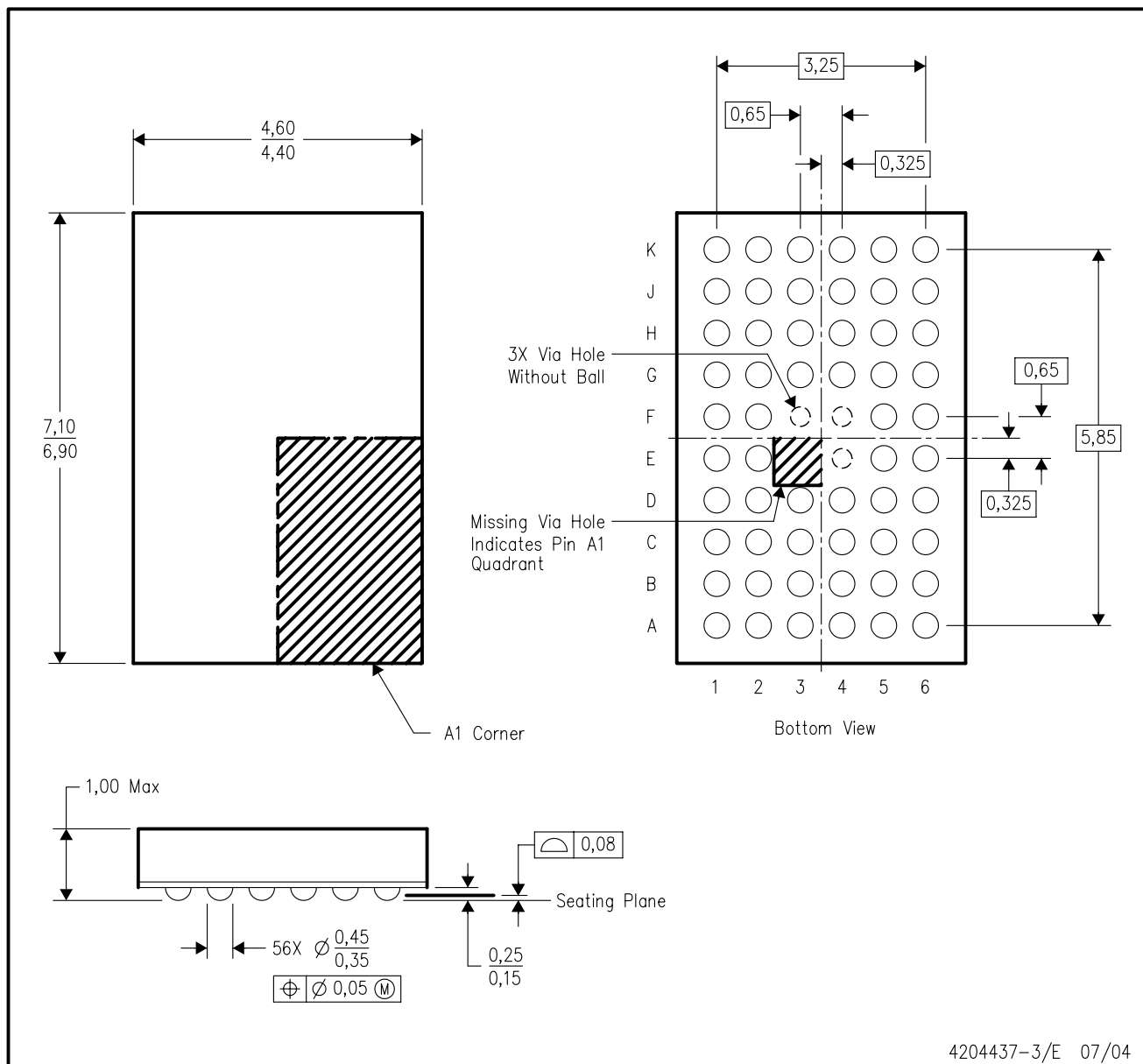
VOLTAGE WAVEFORMS
ENABLE AND DISABLE TIMES

- NOTES:
- C_L includes probe and jig capacitance.
 - Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 - All input pulses are supplied by generators having the following characteristics: $PRR \leq 10$ MHz, $Z_O = 50 \Omega$, $dv/dt \geq 1$ V/ns.
 - The outputs are measured one at a time, with one transition per measurement.
 - t_{PLZ} and t_{PHZ} are the same as t_{dis} .
 - t_{PZL} and t_{PZH} are the same as t_{en} .
 - t_{PLH} and t_{PHL} are the same as t_{pd} .
 - V_{CCI} is the V_{CC} associated with the input port.
 - V_{CCO} is the V_{CC} associated with the output port.

Figure 11. Load Circuit and Voltage Waveforms

ZQL (R-PBGA-N56)

PLASTIC BALL GRID ARRAY



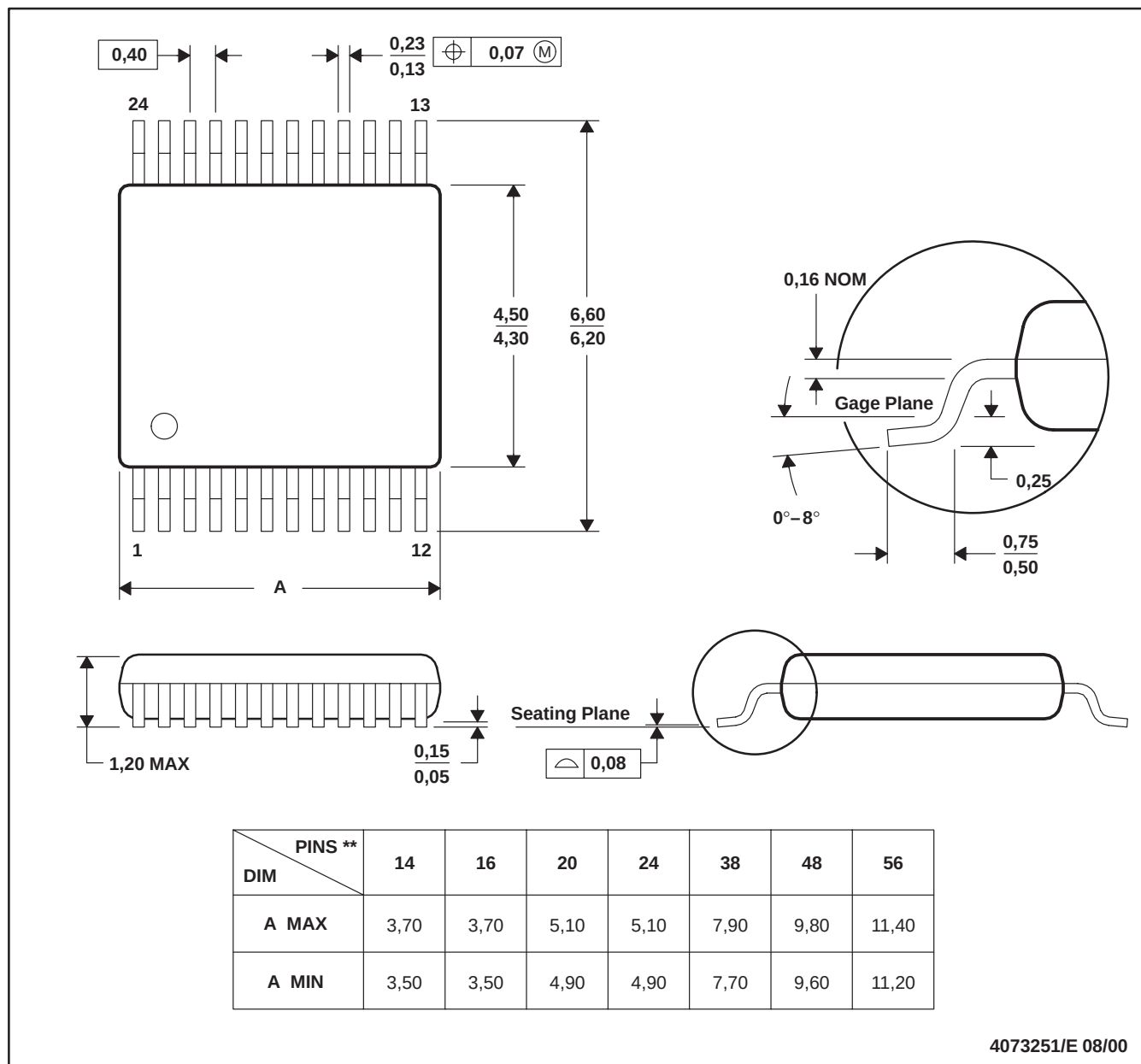
4204437-3/E 07/04

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Falls within JEDEC MO-225 variation BA.
 - D. This package is lead-free. Refer to the 56 GQL package (drawing 4200583) for tin-lead (SnPb).

DGV (R-PDSO-G**)

PLASTIC SMALL-OUTLINE

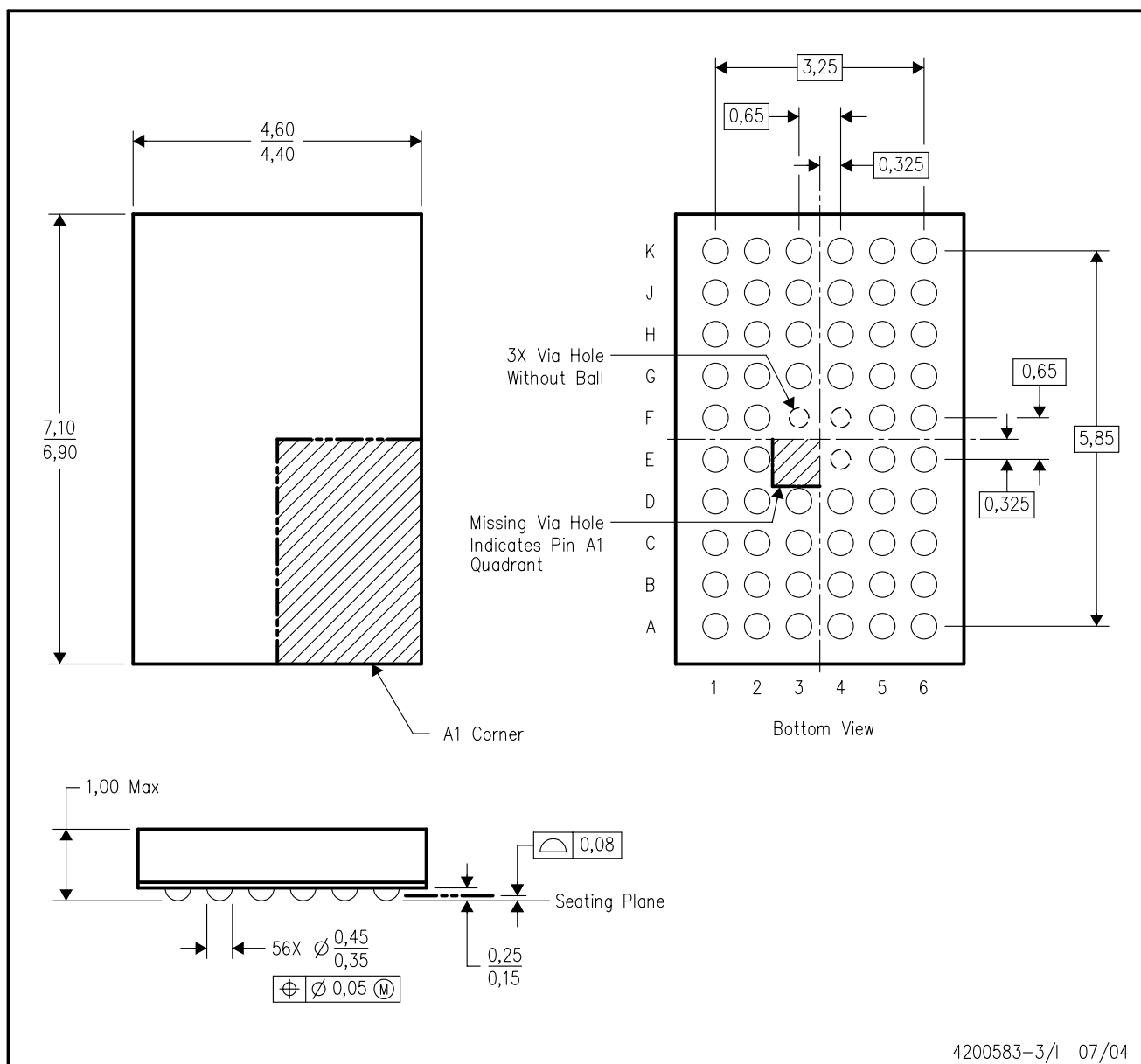
24 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion, not to exceed 0,15 per side.
 D. Falls within JEDEC: 24/48 Pins – MO-153
 14/16/20/56 Pins – MO-194

GQL (R-PBGA-N56)

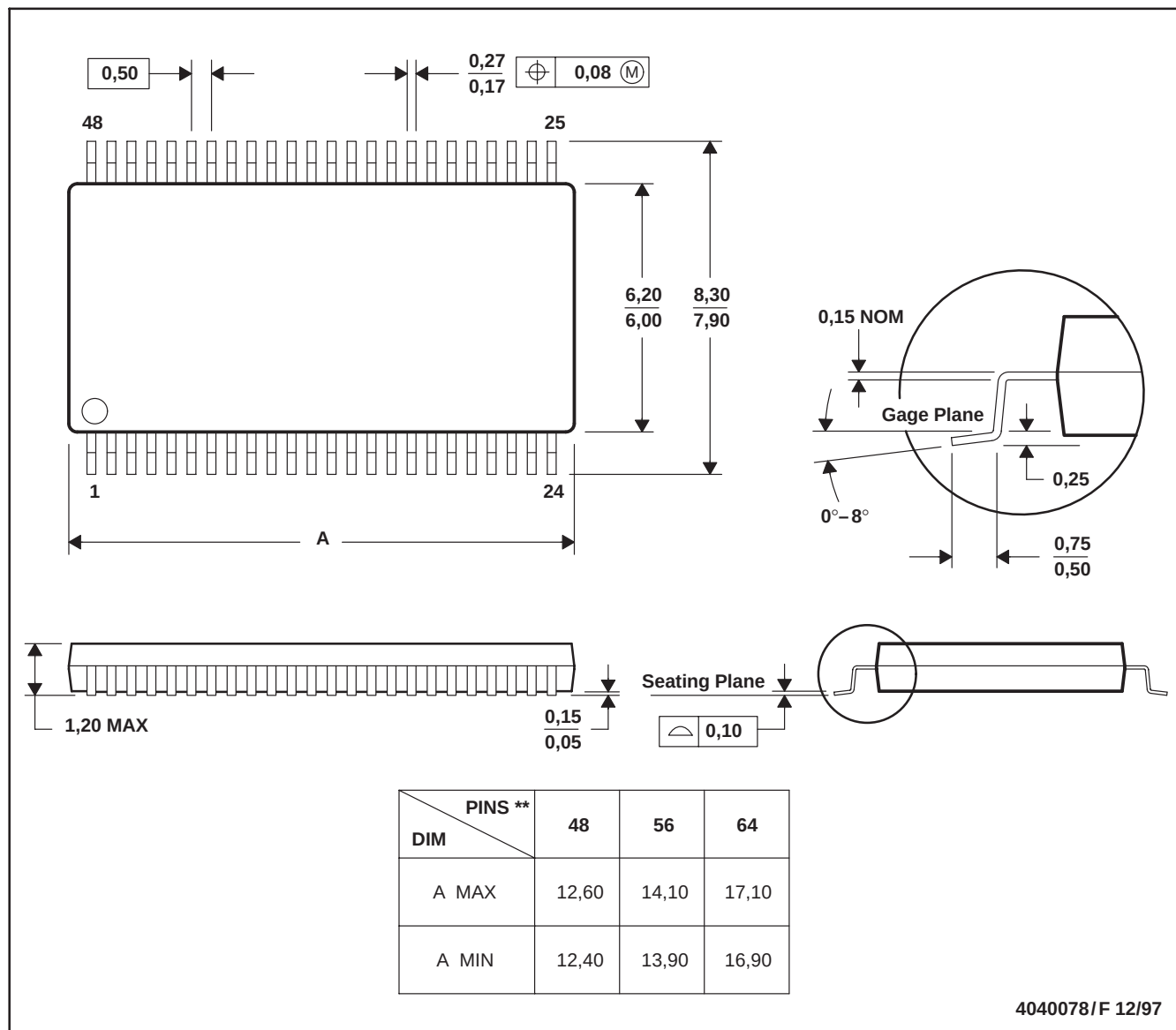
PLASTIC BALL GRID ARRAY



DGG (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

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