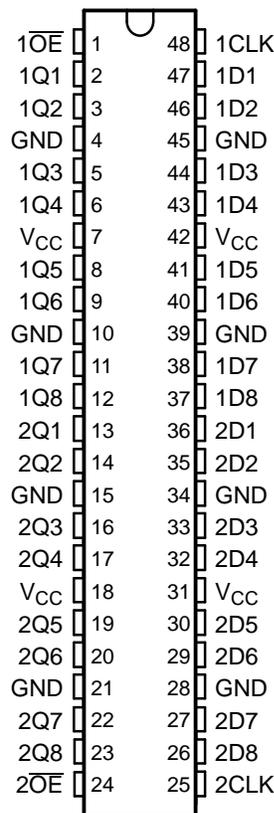


FEATURES

- Members of the Texas Instruments Widebus™ Family
- Output Ports Have Equivalent 22-Ω Series Resistors, So No External Resistors Are Required
- Support Mixed-Mode Signal Operation (5-V Input and Output Voltages With 3.3-V V_{CC})
- Support Unregulated Battery Operation Down to 2.7 V
- Typical V_{OLP} (Output Ground Bounce) <0.8 V at V_{CC} = 3.3 V, T_A = 25°C
- I_{off} and Power-Up 3-State Support Hot Insertion
- Bus Hold on Data Inputs Eliminates the Need for External Pullup/Pulldown Resistors
- Distributed V_{CC} and GND Pins Minimize High-Speed Switching Noise
- Flow-Through Architecture Optimizes PCB Layout
- Latch-Up Performance Exceeds 500 mA Per JESD 17
- ESD Protection Exceeds JESD 22
 - 2000-V Human-Body Model (A114-A)
 - 200-V Machine Model (A115-A)

SN54LVTH162374...WD PACKAGE
 SN74LVTH162374...DGG OR DL PACKAGE
 (TOP VIEW)



DESCRIPTION/ORDERING INFORMATION

ORDERING INFORMATION

| T _A | PACKAGE ⁽¹⁾ | | ORDERABLE PART NUMBER | TOP-SIDE MARKING |
|----------------|------------------------|------------------|--|-------------------|
| –40°C to 85°C | FBGA – GRD | Tape and reel | 74LVTH162374GRDR | LL2374 |
| | FBGA – ZRD (Pb-free) | | 74LVTH162374ZRDR | |
| | SSOP – DL | Tube | SN74LVTH162374DL | LVTH162374 |
| | | Tape and reel | SN74LVTH162374DLR | |
| | | Tube | 74LVTH162374DLG4 | |
| | | Tape and reel | 74LVTH162374DLRG4 | |
| | TSSOP – DGG | Tape and reel | SN74LVTH162374DGGR 74LVTH162374DGGRG4 | LVTH162374 |
| VFBGA – GQL | Tape and reel | SN74LVTH162374KR | LL2374 | |
| | | 74LVTH162374ZQLR | | |
| –55°C to 125°C | CFP – WD | Tube | SNJ54LVTH162374WD | SNJ54LVTH162374WD |

(1) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.



Please be aware that an important notice concerning availability, standard warranty, and use in critical applications of Texas Instruments semiconductor products and disclaimers thereto appears at the end of this data sheet.

Widebus is a trademark of Texas Instruments.

SN54LVTH162374, SN74LVTH162374

3.3-V ABT 16-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

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DESCRIPTION/ORDERING INFORMATION (CONTINUED)

The 'LVTH162374 devices are 16-bit edge-triggered D-type flip-flops with 3-state outputs designed for low-voltage (3.3-V) V_{CC} operation, but with the capability to provide a TTL interface to a 5-V system environment. They are particularly suitable for implementing buffer registers, I/O ports, bidirectional bus drivers, and working registers.

These devices can be used as two 8-bit flip-flops or one 16-bit flip-flop. On the positive transition of the clock (CLK), the Q outputs of the flip-flop take on the logic levels set up at the D inputs.

A buffered output-enable (\overline{OE}) input can be used to place the eight outputs in either a normal logic state (high or low logic levels) or a high-impedance state. In the high-impedance state, the outputs neither load nor drive the bus lines significantly. The high-impedance state and the increased drive provide the capability to drive bus lines without need for interface or pullup components.

\overline{OE} does not affect internal operations of the flip-flop. Old data can be retained or new data can be entered while the outputs are in the high-impedance state.

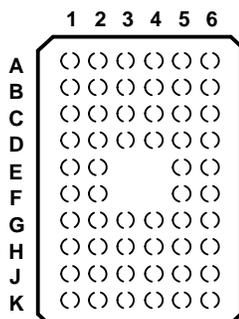
The outputs, which are designed to source or sink up to 12 mA, include equivalent 22- Ω series resistors to reduce overshoot and undershoot.

Active bus-hold circuitry holds unused or undriven inputs at a valid logic state. Use of pullup or pulldown resistors with the bus-hold circuitry is not recommended.

When V_{CC} is between 0 and 1.5 V, the devices are in the high-impedance state during power up or power down. However, to ensure the high-impedance state above 1.5 V, \overline{OE} should be tied to V_{CC} through a pullup resistor; the minimum value of the resistor is determined by the current-sinking capability of the driver.

These devices are fully specified for hot-insertion applications using I_{off} and power-up 3-state. The I_{off} circuitry disables the outputs, preventing damaging current backflow through the devices when they are powered down. The power-up 3-state circuitry places the outputs in the high-impedance state during power up and power down, which prevents driver conflict.

**GQL OR ZQL PACKAGE
(TOP VIEW)**

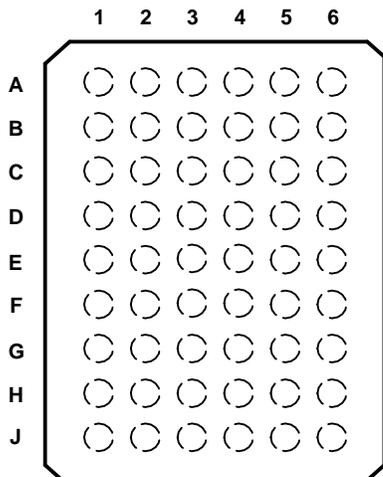


**TERMINAL ASSIGNMENTS⁽¹⁾
(56-Ball GQL/ZQL Package)**

| | 1 | 2 | 3 | 4 | 5 | 6 |
|----------|-------------------|-----|-----------------|-----------------|-----|------|
| A | 1 \overline{OE} | NC | NC | NC | NC | 1CLK |
| B | 1Q2 | 1Q1 | GND | GND | 1D1 | 1D2 |
| C | 1Q4 | 1Q3 | V _{CC} | V _{CC} | 1D3 | 1D4 |
| D | 1Q6 | 1Q5 | GND | GND | 1D5 | 1D6 |
| E | 1Q8 | 1Q7 | | | 1D7 | 1D8 |
| F | 2Q1 | 2Q2 | | | 2D2 | 2D1 |
| G | 2Q3 | 2Q4 | GND | GND | 2D4 | 2D3 |
| H | 2Q5 | 2Q6 | V _{CC} | V _{CC} | 2D6 | 2D5 |
| J | 2Q7 | 2Q8 | GND | GND | 2D8 | 2D7 |
| K | 2 \overline{OE} | NC | NC | NC | NC | 2CLK |

(1) NC – No internal connection

**GRD OR ZRD PACKAGE
(TOP VIEW)**



**TERMINAL ASSIGNMENTS⁽¹⁾
(54-Ball GRD/ZRD Package)**

| | 1 | 2 | 3 | 4 | 5 | 6 |
|----------|-----|-----|-------------------|-----------------|-----|-----|
| A | 1Q1 | NC | 1 \overline{OE} | 1CLK | NC | 1D1 |
| B | 1Q3 | 1Q2 | NC | NC | 1D2 | 1D3 |
| C | 1Q5 | 1Q4 | V _{CC} | V _{CC} | 1D4 | 1D5 |
| D | 1Q7 | 1Q6 | GND | GND | 1D6 | 1D7 |
| E | 2Q1 | 1Q8 | GND | GND | 1D8 | 2D1 |
| F | 2Q3 | 2Q2 | GND | GND | 2D2 | 2D3 |
| G | 2Q5 | 2Q4 | V _{CC} | V _{CC} | 2D4 | 2D5 |
| H | 2Q7 | 2Q6 | NC | NC | 2D6 | 2D7 |
| J | 2Q8 | NC | 2 \overline{OE} | 2CLK | NC | 2D8 |

(1) NC – No internal connection

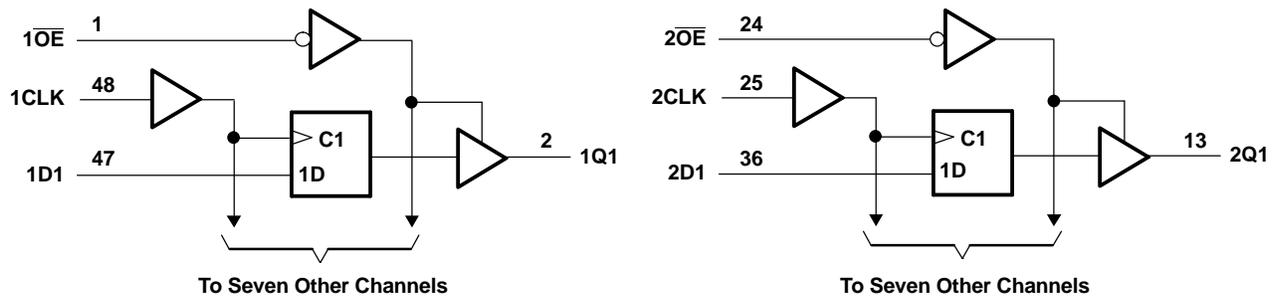
**FUNCTION TABLE
(EACH FLIP-FLOP)**

| INPUTS | | | OUTPUT Q |
|-----------------|--------|---|----------------|
| \overline{OE} | CLK | D | |
| L | ↑ | H | H |
| L | ↑ | L | L |
| L | H or L | X | Q ₀ |
| H | X | X | Z |

SN54LVTH162374, SN74LVTH162374 3.3-V ABT 16-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOPS WITH 3-STATE OUTPUTS

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LOGIC DIAGRAM (POSITIVE LOGIC)



Pin numbers shown are for the DGG, DL, and WD packages.

Absolute Maximum Ratings⁽¹⁾

over operating free-air temperature range (unless otherwise noted)

| | | MIN | MAX | UNIT |
|---------------|---|-----------------|----------------|------|
| V_{CC} | Supply voltage range | -0.5 | 4.6 | V |
| V_I | Input voltage range ⁽²⁾ | -0.5 | 7 | V |
| V_O | Voltage range applied to any output in the high-impedance or power-off state ⁽²⁾ | -0.5 | 7 | V |
| V_O | Voltage range applied to any output in the high state ⁽²⁾ | -0.5 | $V_{CC} + 0.5$ | V |
| I_O | Current into any output in the low state | | 30 | mA |
| I_O | Current into any output in the high state ⁽³⁾ | | 30 | mA |
| I_{IK} | Input clamp current | $V_I < 0$ | -50 | mA |
| I_{OK} | Output clamp current | $V_O < 0$ | -50 | mA |
| θ_{JA} | Package thermal impedance ⁽⁴⁾ | DGG package | 70 | °C/W |
| | | DL package | 63 | |
| | | GQL/ZQL package | 42 | |
| | | GRD/ZRD package | 36 | |
| T_{stg} | Storage temperature range | -65 | 150 | °C |

- (1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- (2) The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
- (3) This current flows only when the output is in the high state and $V_O > V_{CC}$.
- (4) The package thermal impedance is calculated in accordance with JESD 51-7.

Recommended Operating Conditions⁽¹⁾

| | | SN54LVTH162374 | | SN74LVTH162374 | | UNIT |
|--------------------------|------------------------------------|----------------|-----|----------------|-----|-----------|
| | | MIN | MAX | MIN | MAX | |
| V_{CC} | Supply voltage | 2.7 | 3.6 | 2.7 | 3.6 | V |
| V_{IH} | High-level input voltage | 2 | | 2 | | V |
| V_{IL} | Low-level input voltage | | 0.8 | | 0.8 | V |
| V_I | Input voltage | | 5.5 | | 5.5 | V |
| I_{OH} | High-level output current | | -12 | | -12 | mA |
| I_{OL} | Low-level output current | | 12 | | 12 | mA |
| $\Delta t/\Delta v$ | Input transition rise or fall rate | | 10 | | 10 | ns/V |
| $\Delta t/\Delta V_{CC}$ | Power-up ramp rate | 200 | | 200 | | μ s/V |
| T_A | Operating free-air temperature | -55 | 125 | -40 | 85 | °C |

- (1) All unused control inputs of the device must be held at V_{CC} or GND to ensure proper device operation. Refer to the TI application report, *Implications of Slow or Floating CMOS Inputs*, literature number SCBA004.

Electrical Characteristics

over recommended operating free-air temperature range (unless otherwise noted)

| PARAMETER | TEST CONDITIONS | | SN54LVTH162374 | | | SN74LVTH162374 | | | UNIT |
|--------------------------------|--|--|----------------------------------|--------------------|-------------|----------------|--------------------|---------------|---------------|
| | | | MIN | TYP ⁽¹⁾ | MAX | MIN | TYP ⁽¹⁾ | MAX | |
| V_{IK} | $V_{CC} = 2.7\text{ V}$, $I_I = -18\text{ mA}$ | | -1.2 | | | -1.2 | | | V |
| V_{OH} | $V_{CC} = 3\text{ V}$, $I_{OH} = -12\text{ mA}$ | | 2 | | | 2 | | | V |
| V_{OL} | $V_{CC} = 3\text{ V}$, $I_{OL} = 12\text{ mA}$ | | 0.8 | | | 0.8 | | | V |
| I_I | Control inputs | $V_{CC} = 0\text{ or }3.6\text{ V}$, $V_I = 5.5\text{ V}$ | 10 | | | 10 | | | μA |
| | | $V_{CC} = 3.6\text{ V}$, $V_I = V_{CC}\text{ or GND}$ | ± 1 | | | ± 1 | | | |
| | Data inputs | $V_{CC} = 3.6\text{ V}$ | $V_I = V_{CC}$ | 1 | | 1 | | | |
| | | | $V_I = 0$ | -5 | | -5 | | | |
| I_{off} | $V_{CC} = 0$, $V_I\text{ or }V_O = 0\text{ to }4.5\text{ V}$ | | | | | ± 100 | | | μA |
| $I_{I(\text{hold})}$ | Data inputs | $V_{CC} = 3\text{ V}$ | $V_I = 0.8\text{ V}$ | 75 | | 75 | | μA | |
| | | | $V_I = 2\text{ V}$ | -75 | | -75 | | | |
| | | $V_{CC} = 3.6\text{ V}$, ⁽²⁾ | $V_I = 0\text{ to }3.6\text{ V}$ | | 500 -750 | | | | |
| I_{OZH} | $V_{CC} = 3.6\text{ V}$, $V_O = 3\text{ V}$ | | 5 | | | 5 | | | μA |
| I_{OZL} | $V_{CC} = 3.6\text{ V}$, $V_O = 0.5\text{ V}$ | | -5 | | | -5 | | | μA |
| I_{OZPU} | $V_{CC} = 0\text{ to }1.5\text{ V}$, $V_O = 0.5\text{ V to }3\text{ V}$, $OE = \text{don't care}$ | | ± 100 ⁽³⁾ | | | ± 100 | | | μA |
| I_{OZPD} | $V_{CC} = 1.5\text{ V to }0$, $V_O = 0.5\text{ V to }3\text{ V}$, $OE = \text{don't care}$ | | ± 100 ⁽³⁾ | | | ± 100 | | | μA |
| I_{CC} | $V_{CC} = 3.6\text{ V}$, $I_O = 0$, $V_I = V_{CC}\text{ or GND}$ | | Outputs high | | 0.19 | | 0.19 | | mA |
| | | | Outputs low | | 5 | | 5 | | |
| | | | Outputs disabled | | 0.19 | | 0.19 | | |
| ΔI_{CC} ⁽⁴⁾ | $V_{CC} = 3\text{ V to }3.6\text{ V}$, One input at $V_{CC} - 0.6\text{ V}$, Other inputs at $V_{CC}\text{ or GND}$ | | 0.2 | | | 0.2 | | | mA |
| C_i | $V_I = 3\text{ V or }0$ | | 3 | | | 3 | | | pF |
| C_o | $V_O = 3\text{ V or }0$ | | 9 | | | 9 | | | pF |

 (1) All typical values are at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$.

(2) This is the bus-hold maximum dynamic current. It is the minimum overdrive current required to switch the input from one state to another.

(3) On products compliant to MIL-PRF-38535, this parameter is not production tested.

 (4) This is the increase in supply current for each input that is at the specified TTL voltage level, rather than V_{CC} or GND.

Timing Requirements

over recommended operating free-air temperature range (unless otherwise noted) (see Figure 1)

| | | SN54LVTH162374 | | | | SN74LVTH162374 | | | | UNIT |
|--------------------|--|--|-----|-------------------------|-----|--|-----|-------------------------|-----|------|
| | | $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ | | $V_{CC} = 2.7\text{ V}$ | | $V_{CC} = 3.3\text{ V} \pm 0.3\text{ V}$ | | $V_{CC} = 2.7\text{ V}$ | | |
| | | MIN | MAX | MIN | MAX | MIN | MAX | MIN | MAX | |
| f_{clock} | Clock frequency | 160 | | 160 | | 160 | | 160 | | MHz |
| t_w | Pulse duration, CLK high or low | 3 | | 3.3 | | 3 | | 3 | | ns |
| t_{su} | Setup time, data before CLK \uparrow | High or low | 2.8 | 3.2 | 1.8 | 2 | ns | | | |
| t_h | Hold time, data after CLK \uparrow | High or low | 1.2 | 0.5 | 0.8 | 0.1 | ns | | | |

SN54LVTH162374, SN74LVTH162374
3.3-V ABT 16-BIT EDGE-TRIGGERED D-TYPE FLIP-FLOPS
WITH 3-STATE OUTPUTS

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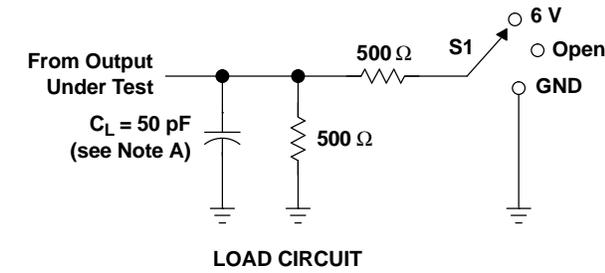
Switching Characteristics

over recommended operating free-air temperature range, $C_L = 50$ pF (unless otherwise noted) (see [Figure 1](#))

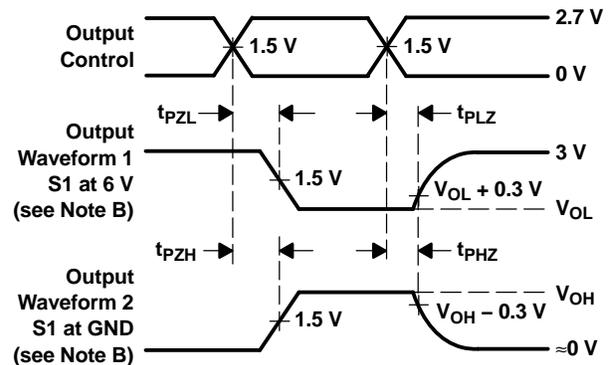
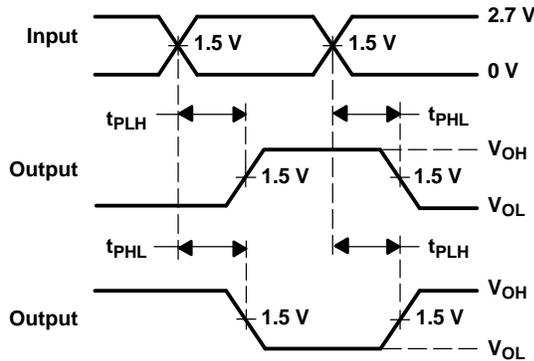
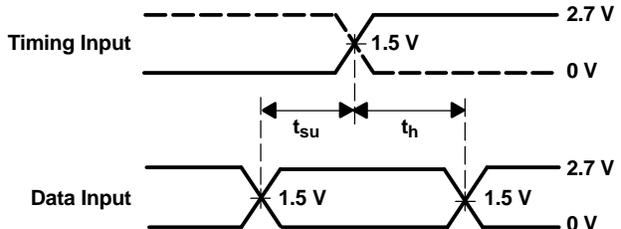
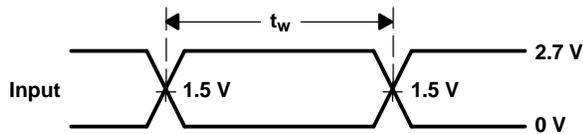
| PARAMETER | FROM (INPUT) | TO (OUTPUT) | SN54LVTH162374 | | | | SN74LVTH162374 | | | | UNIT | |
|-------------|-----------------|----------------|---|-----|-------------------------|-----|---|--------------------|-----|-------------------------|------|-----|
| | | | $V_{CC} = 3.3\text{ V}$ $\pm 0.3\text{ V}$ | | $V_{CC} = 2.7\text{ V}$ | | $V_{CC} = 3.3\text{ V}$ $\pm 0.3\text{ V}$ | | | $V_{CC} = 2.7\text{ V}$ | | |
| | | | MIN | MAX | MIN | MAX | MIN | TYP ⁽¹⁾ | MAX | MIN | | MAX |
| f_{max} | | | 160 | | 160 | | 160 | | | 160 | | MHz |
| t_{PLH} | CLK | Q | 1.4 | 6.6 | 7.4 | | 2 | 3.4 | 5.3 | 6.2 | | ns |
| t_{PHL} | | | 1.4 | 5.8 | 6 | | 2.2 | 3.3 | 4.9 | 5.1 | | |
| t_{PZH} | \overline{OE} | Q | 1 | 6.6 | 7.4 | | 1.8 | 3.5 | 5.6 | 6.9 | | ns |
| t_{PZL} | | | 1.4 | 6 | 6.8 | | 1.8 | 3.5 | 4.9 | 6 | | |
| t_{PHZ} | \overline{OE} | Q | 1 | 6.6 | 7.4 | | 2.4 | 4.2 | 5.4 | 5.7 | | ns |
| t_{PLZ} | | | 1.4 | 6 | 6 | | 2 | 3.8 | 5 | 5.1 | | |
| $t_{sk(o)}$ | | | | | | | | 0.5 | | | ns | |

(1) All typical values are at $V_{CC} = 3.3\text{ V}$, $T_A = 25^\circ\text{C}$.

PARAMETER MEASUREMENT INFORMATION



| TEST | S1 |
|-------------------|------|
| t_{PLH}/t_{PHL} | Open |
| t_{PLZ}/t_{PZL} | 6 V |
| t_{PHZ}/t_{PZH} | GND |



- NOTES: A. C_L includes probe and jig capacitance.
 B. Waveform 1 is for an output with internal conditions such that the output is low, except when disabled by the output control. Waveform 2 is for an output with internal conditions such that the output is high, except when disabled by the output control.
 C. All input pulses are supplied by generators having the following characteristics: $PRR \leq 10 \text{ MHz}$, $Z_O = 50 \Omega$, $t_r \leq 2.5 \text{ ns}$, $t_f \leq 2.5 \text{ ns}$.
 D. The outputs are measured one at a time, with one transition per measurement.

Figure 1. Load Circuit and Voltage Waveforms

PACKAGING INFORMATION

| Orderable Device | Status ⁽¹⁾ | Package Type | Package Drawing | Pins | Package Qty | Eco Plan ⁽²⁾ | Lead/Ball Finish | MSL Peak Temp ⁽³⁾ |
|--------------------|-----------------------|--------------|-----------------|------|-------------|-------------------------|------------------|------------------------------|
| 5962-9854201QXA | ACTIVE | CFP | WD | 48 | 1 | TBD | Call TI | Level-NC-NC-NC |
| 5962-9854201VXA | ACTIVE | CFP | WD | 48 | 1 | TBD | Call TI | Level-NC-NC-NC |
| 74LVTH162374DGGRG4 | ACTIVE | TSSOP | DGG | 48 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| 74LVTH162374DLG4 | ACTIVE | SSOP | DL | 48 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| 74LVTH162374DLRG4 | ACTIVE | SSOP | DL | 48 | 1000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| 74LVTH162374GRDR | ACTIVE | LFBGA | GRD | 54 | 1000 | TBD | SNPB | Level-1-240C-UNLIM |
| 74LVTH162374ZQLR | ACTIVE | VFBGA | ZQL | 56 | 1000 | Green (RoHS & no Sb/Br) | SNAGCU | Level-1-260C-UNLIM |
| 74LVTH162374ZRDR | ACTIVE | LFBGA | ZRD | 54 | 1000 | Green (RoHS & no Sb/Br) | SNAGCU | Level-1-260C-UNLIM |
| SN74LVTH162374DGGR | ACTIVE | TSSOP | DGG | 48 | 2000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LVTH162374DL | ACTIVE | SSOP | DL | 48 | 25 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LVTH162374DLR | ACTIVE | SSOP | DL | 48 | 1000 | Green (RoHS & no Sb/Br) | CU NIPDAU | Level-1-260C-UNLIM |
| SN74LVTH162374KR | ACTIVE | VFBGA | GQL | 56 | 1000 | TBD | SNPB | Level-1-240C-UNLIM |
| SNJ54LVTH162374WD | ACTIVE | CFP | WD | 48 | 1 | TBD | Call TI | Level-NC-NC-NC |

⁽¹⁾ The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

OBSOLETE: TI has discontinued the production of the device.

⁽²⁾ Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS) or Green (RoHS & no Sb/Br) - please check <http://www.ti.com/productcontent> for the latest availability information and additional product content details.

TBD: The Pb-Free/Green conversion plan has not been defined.

Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

⁽³⁾ MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

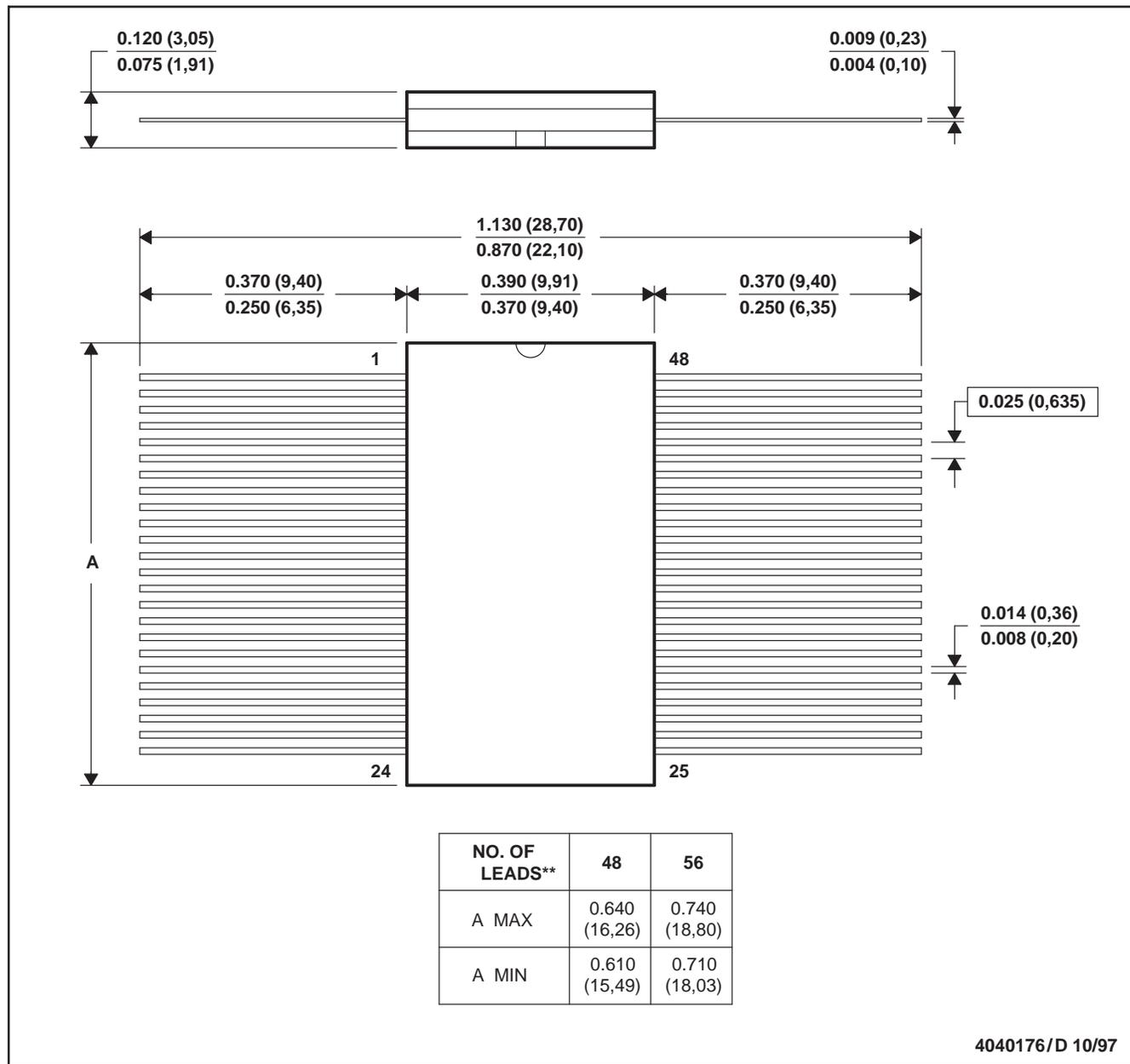
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WD (R-GDFP-F**)

CERAMIC DUAL FLATPACK

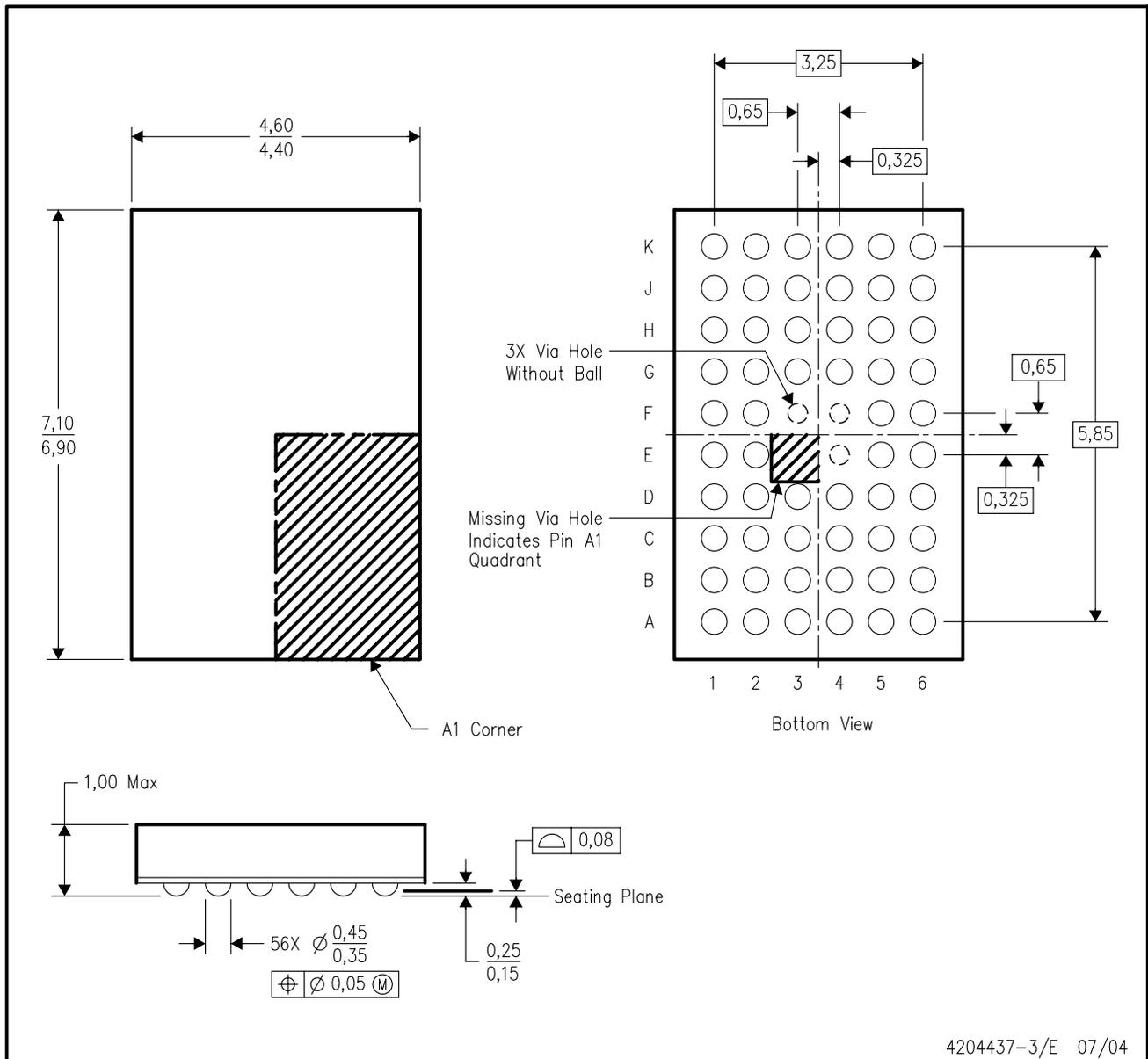
48 LEADS SHOWN



- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. This package can be hermetically sealed with a ceramic lid using glass frit.
 D. Index point is provided on cap for terminal identification only
 E. Falls within MIL STD 1835: GDFP1-F48 and JEDEC MO-146AA
 GDFP1-F56 and JEDEC MO-146AB

ZQL (R-PBGA-N56)

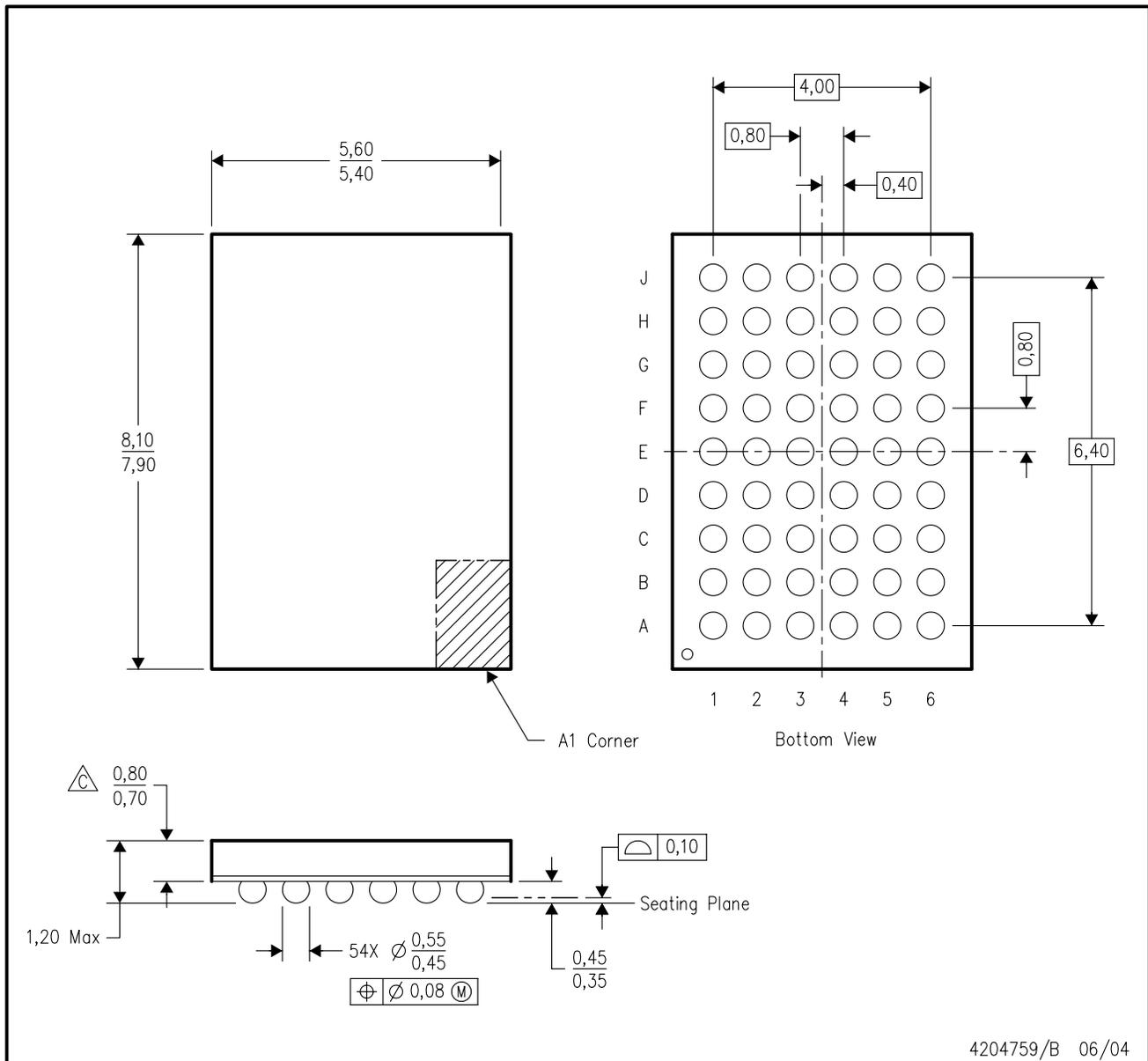
PLASTIC BALL GRID ARRAY



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Falls within JEDEC MO-225 variation BA.
 - D. This package is lead-free. Refer to the 56 GQL package (drawing 4200583) for tin-lead (SnPb).

GRD (R-PBGA-N54)

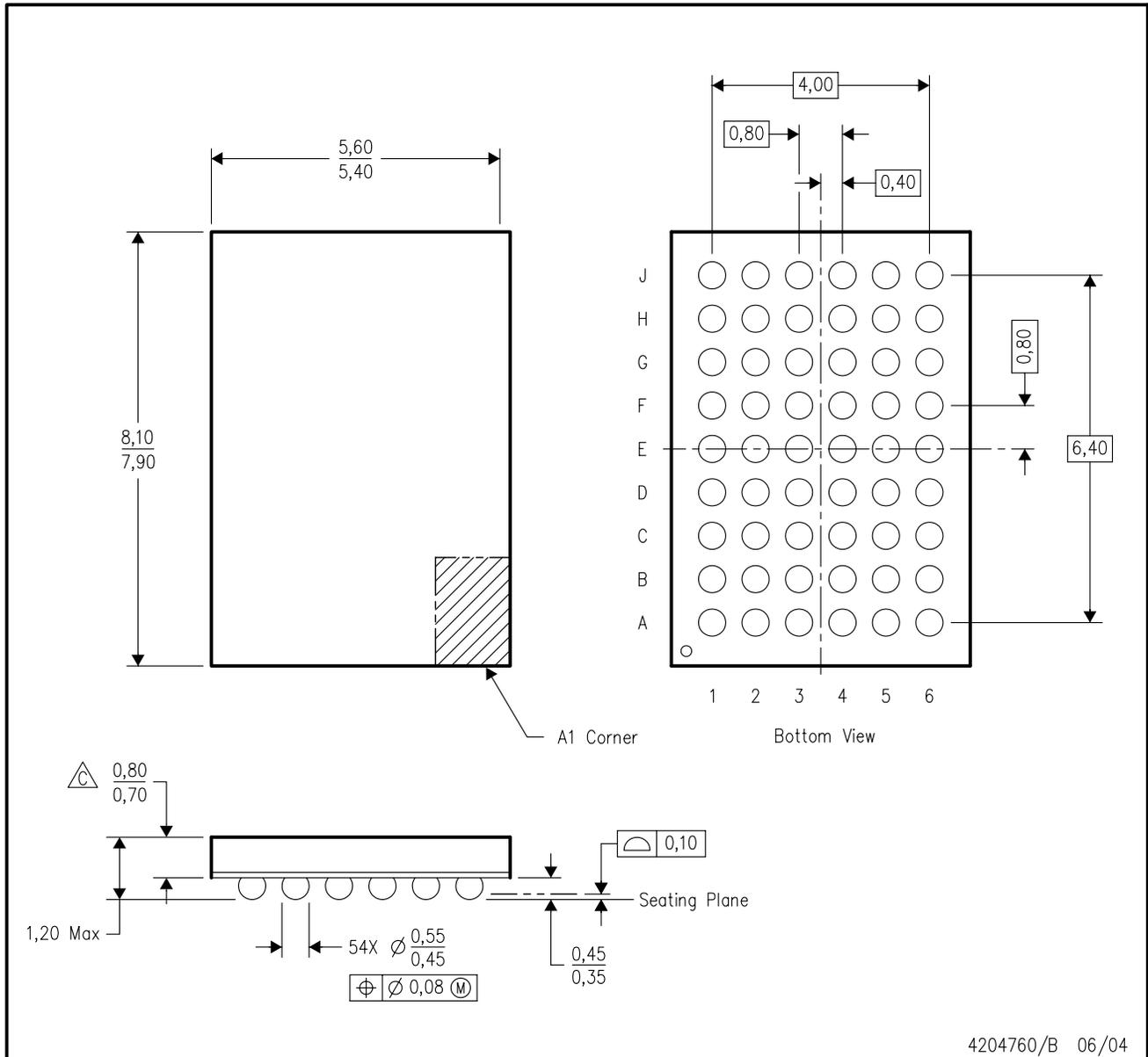
PLASTIC BALL GRID ARRAY



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - \triangle Falls within JEDEC MO-205 variation DD.
 - D. This package is tin-lead (SnPb). Refer to the 54 ZRD package (drawing 4204760) for lead-free.

ZRD (R-PBGA-N54)

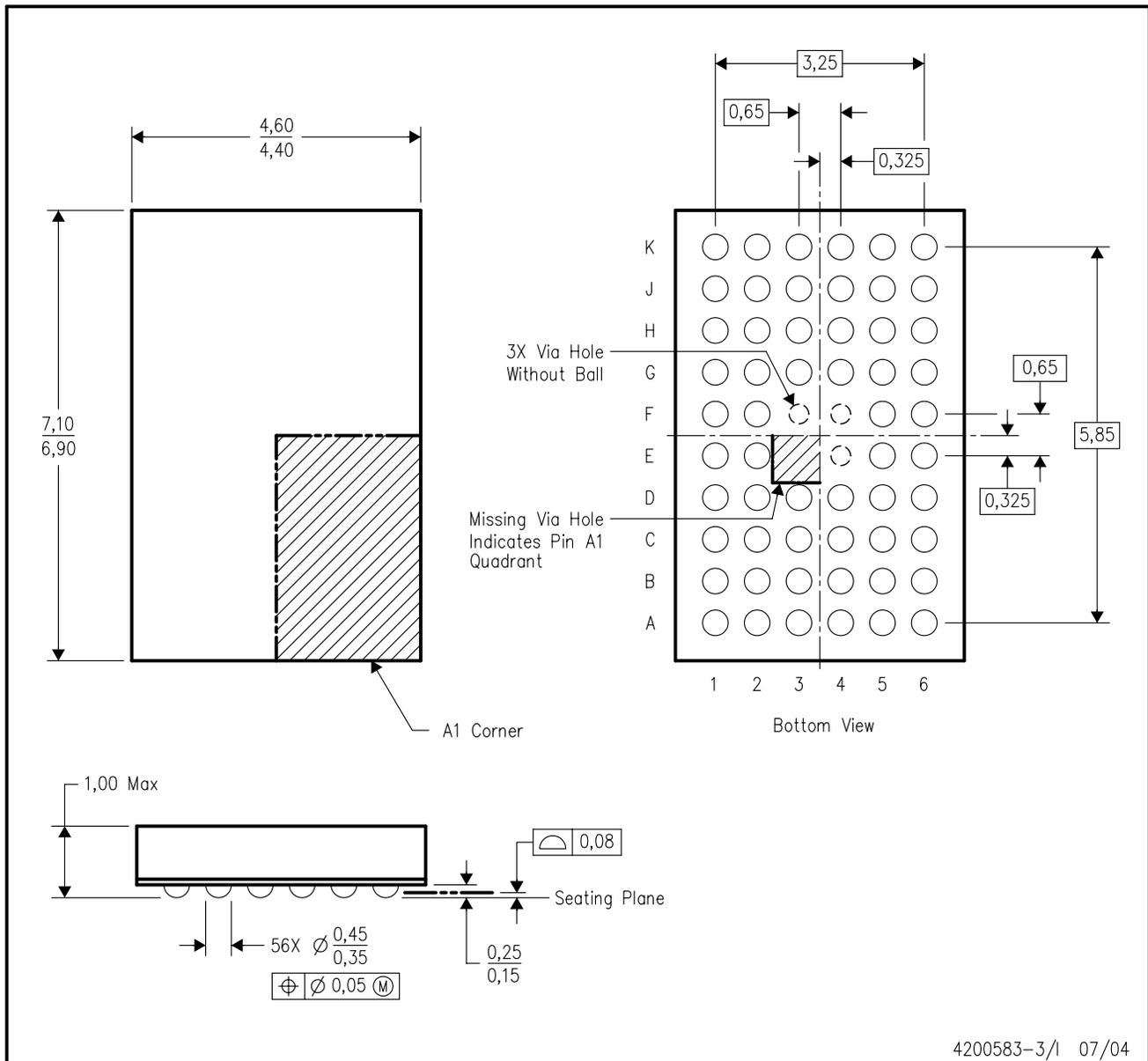
PLASTIC BALL GRID ARRAY



- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Falls within JEDEC MO-205 variation DD.
 - D. This package is lead-free. Refer to the 54 GRD package (drawing 4204759) for tin-lead (SnPb).

GQL (R-PBGA-N56)

PLASTIC BALL GRID ARRAY



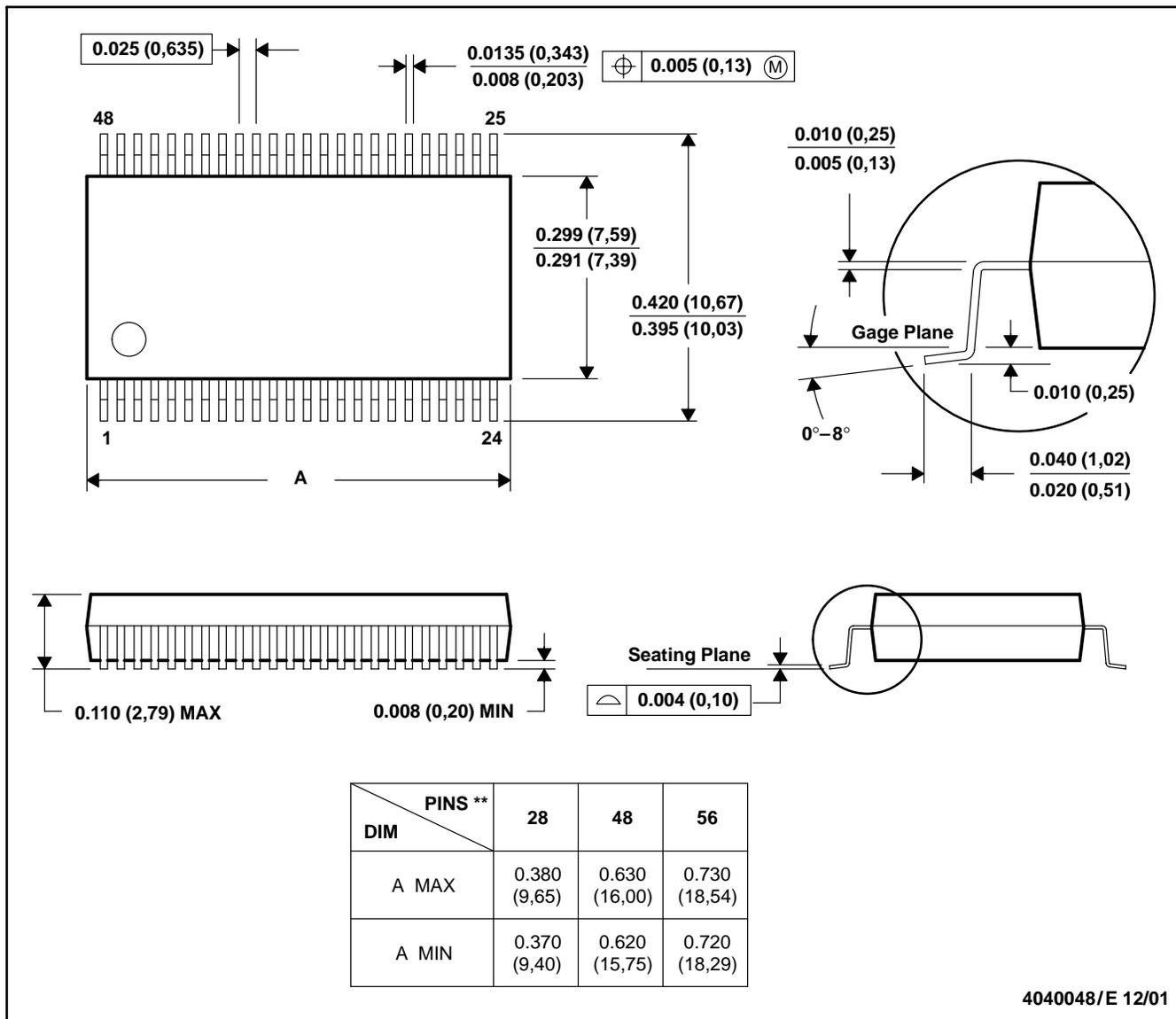
4200583-3/1 07/04

- NOTES:
- A. All linear dimensions are in millimeters.
 - B. This drawing is subject to change without notice.
 - C. Falls within JEDEC MO-225 variation BA.
 - D. This package is tin-lead (SnPb). Refer to the 56 ZQL package (drawing 4204437) for lead-free.

DL (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN

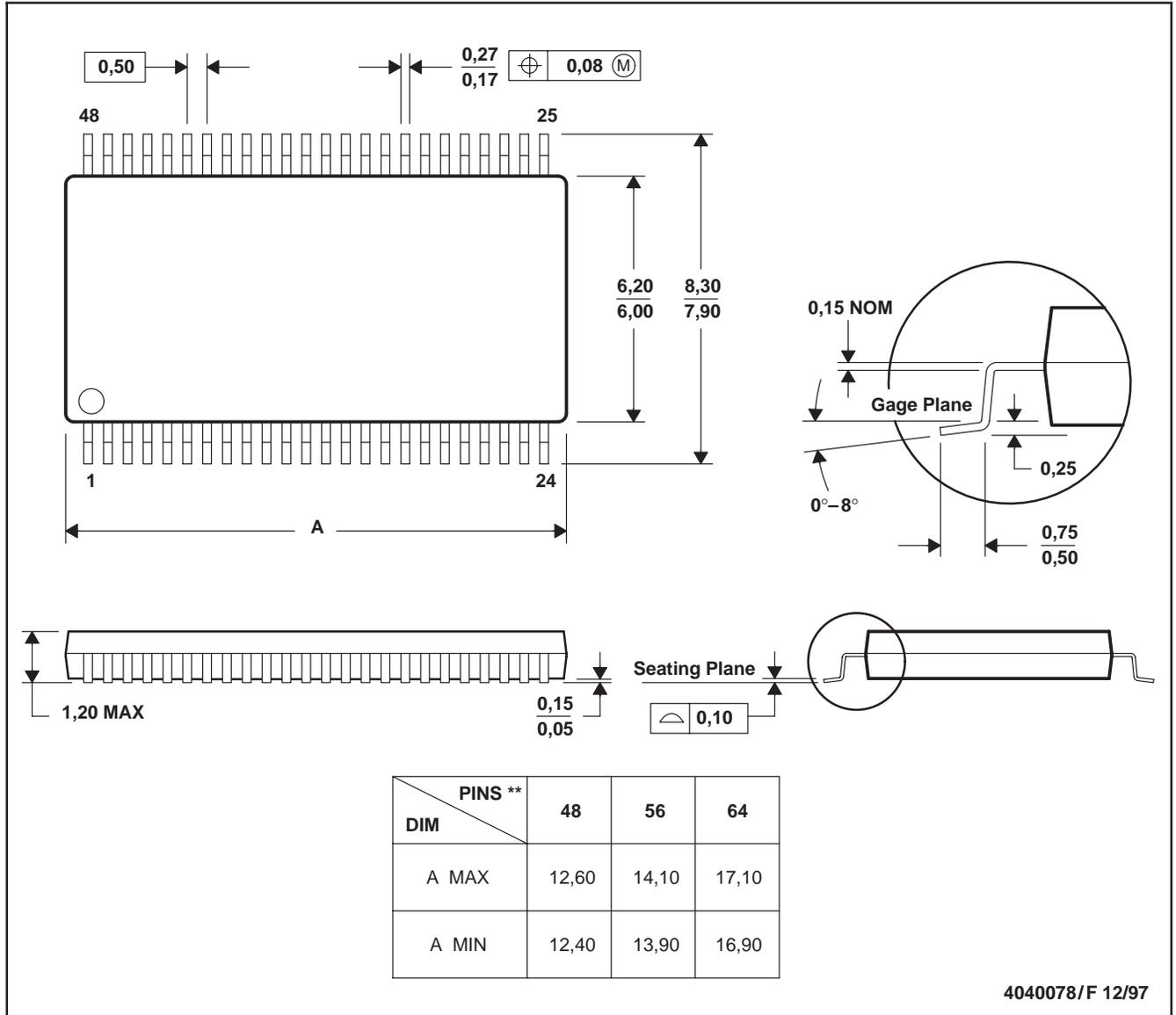


- NOTES: A. All linear dimensions are in inches (millimeters).
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold flash or protrusion not to exceed 0.006 (0,15).
 D. Falls within JEDEC MO-118

DGG (R-PDSO-G**)

PLASTIC SMALL-OUTLINE PACKAGE

48 PINS SHOWN



- NOTES: A. All linear dimensions are in millimeters.
 B. This drawing is subject to change without notice.
 C. Body dimensions do not include mold protrusion not to exceed 0,15.
 D. Falls within JEDEC MO-153

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