



ZXM64N02X

20V N-CHANNEL ENHANCEMENT MODE MOSFET

SUMMARY

$V_{(BR)DSS}=20V$; $R_{DS(ON)}=0.040\Omega$; $I_D=5.4A$

DESCRIPTION

This new generation of high density MOSFETs from Zetex utilises a unique structure that combines the benefits of low on-resistance with fast switching speed. This makes them ideal for high efficiency, low voltage, power management applications.

FEATURES

- Low on-resistance
- Fast switching speed
- Low threshold
- Low gate drive
- Low profile SOIC package

APPLICATIONS

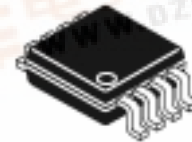
- DC - DC Converters
- Power Management Functions
- Disconnect switches
- Motor control

ORDERING INFORMATION

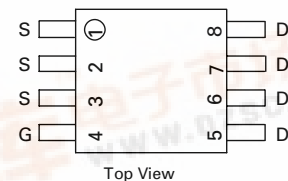
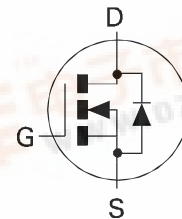
DEVICE	REEL SIZE (inches)	TAPE WIDTH (mm)	QUANTITY PER REEL
ZXM64N02XTA	7	12mm embossed	1000 units
ZXM64N02XTC	13	12mm embossed	4000 units

DEVICE MARKING

- ZXM4N02



MSOP8



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ABSOLUTE MAXIMUM RATINGS.

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	V_{DS}	20	V
Gate- Source Voltage	V_{GS}	± 12	V
Continuous Drain Current ($V_{GS}=4.5V$; $T_A=25^\circ C$)(b) ($V_{GS}=4.5V$; $T_A=70^\circ C$)(b)	I_D	5.4 4.3	A
Pulsed Drain Current (c)	I_{DM}	30	A
Continuous Source Current (Body Diode)(b)	I_S	2.4	A
Pulsed Source Current (Body Diode)(c)	I_{SM}	30	A
Power Dissipation at $T_A=25^\circ C$ (a) Linear Derating Factor	P_D	1.1 8.8	W mW/ $^\circ C$
Power Dissipation at $T_A=25^\circ C$ (b) Linear Derating Factor	P_D	1.8 14.4	W mW/ $^\circ C$
Operating and Storage Temperature Range	$T_j:T_{stg}$	-55 to +150	$^\circ C$

THERMAL RESISTANCE

PARAMETER	SYMBOL	VALUE	UNIT
Junction to Ambient (a)	$R_{\theta JA}$	113	$^\circ C/W$
Junction to Ambient (b)	$R_{\theta JA}$	70	$^\circ C/W$

NOTES

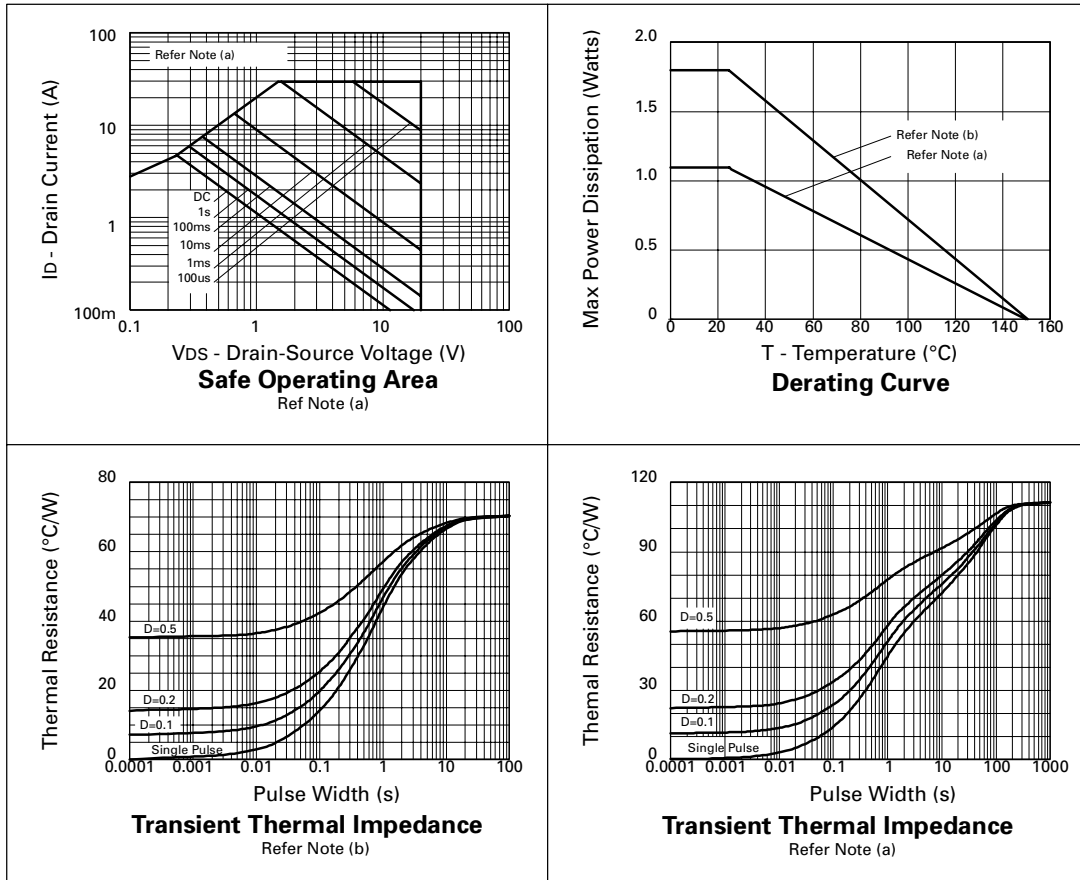
(a) For a device surface mounted on 25mm x 25mm FR4 PCB with high coverage of single sided 1oz copper, in still air conditions

(b) For a device surface mounted on FR4 PCB measured at $t \leq 10$ secs.

(c) Repetitive rating - pulse width limited by maximum junction temperature. Refer to Transient Thermal Impedance graph.

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TYPICAL CHARACTERISTICS



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ELECTRICAL CHARACTERISTICS (at $T_{amb} = 25^{\circ}\text{C}$ unless otherwise stated).

PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS.
STATIC						
Drain-Source Breakdown Voltage	$V_{(BR)DSS}$	20			V	$I_D=250\mu A, V_{GS}=0V$
Zero Gate Voltage Drain Current	I_{DSS}			1	μA	$V_{DS}=20V, V_{GS}=0V$
Gate-Body Leakage	I_{GSS}			100	nA	$V_{GS}=\pm 12V, V_{DS}=0V$
Gate-Source Threshold Voltage	$V_{GS(th)}$	0.7			V	$I_D=250\mu A, V_{DS}=V_{GS}$
Static Drain-Source On-State Resistance (1)	$R_{DS(on)}$			0.040 0.050	Ω Ω	$V_{GS}=4.5V, I_D=3.8A$ $V_{GS}=2.7V, I_D=1.9A$
Forward Transconductance (3)	g_{fs}	6.1			S	$V_{DS}=10V, I_D=1.9A$
DYNAMIC (3)						
Input Capacitance	C_{iss}		1100		pF	$V_{DS}=15V, V_{GS}=0V, f=1MHz$
Output Capacitance	C_{oss}		350		pF	
Reverse Transfer Capacitance	C_{rss}		100		pF	
SWITCHING(2) (3)						
Turn-On Delay Time	$t_{d(on)}$		5.7		ns	$V_{DD}=10V, I_D=3.8A$ $R_G=6.2\Omega, R_D=2.6\Omega$ (Refer to test circuit)
Rise Time	t_r		9.6		ns	
Turn-Off Delay Time	$t_{d(off)}$		28.3		ns	
Fall Time	t_f		11.6		ns	
Total Gate Charge	Q_g			16	nC	$V_{DS}=16V, V_{GS}=4.5V, I_D=3.8A$ (Refer to test circuit)
Gate-Source Charge	Q_{gs}			3.5	nC	
Gate Drain Charge	Q_{gd}			5.4	nC	
SOURCE-DRAIN DIODE						
Diode Forward Voltage (1)	V_{SD}			0.95	V	$T_J=25^{\circ}C, I_S=3.8A, V_{GS}=0V$
Reverse Recovery Time (3)	t_{rr}		23.7		ns	$T_J=25^{\circ}C, I_F=3.8A, di/dt=100A/\mu s$
Reverse Recovery Charge(3)	Q_{rr}		13.3		nC	

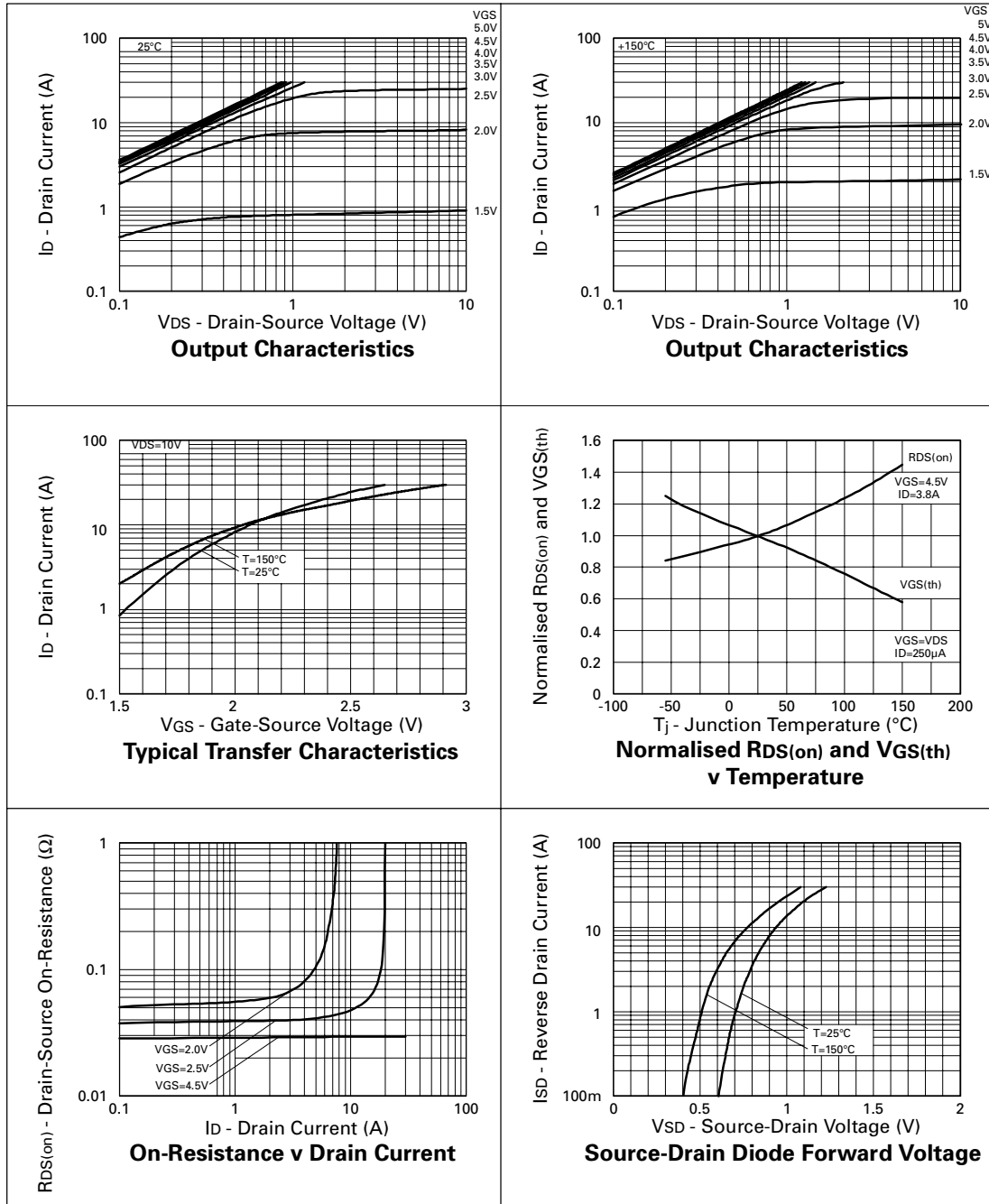
(1) Measured under pulsed conditions. Width=300 μs . Duty cycle $\leq 2\%$.

(2) Switching characteristics are independent of operating junction temperature.

(3) For design aid only, not subject to production testing.

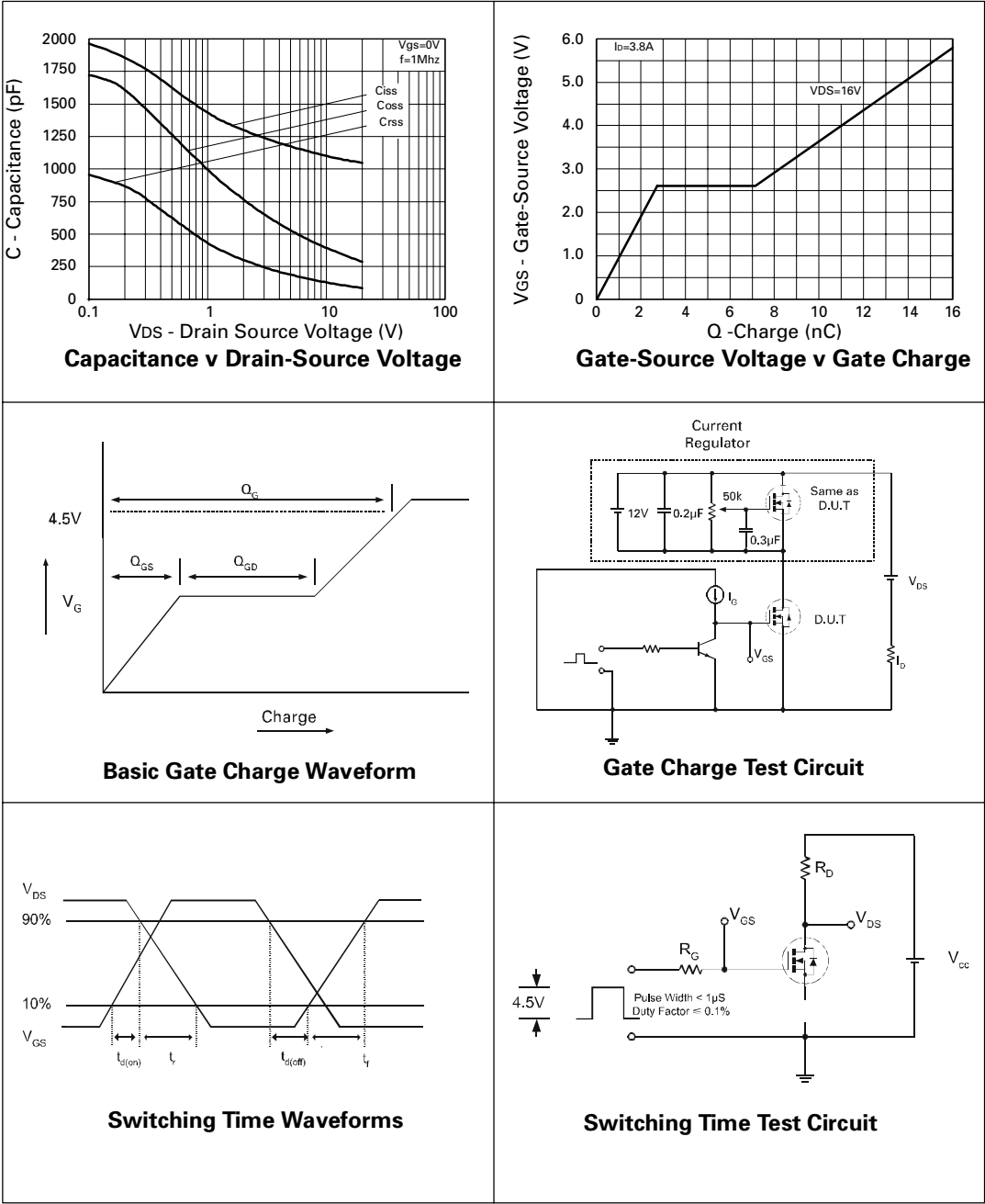
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TYPICAL CHARACTERISTICS



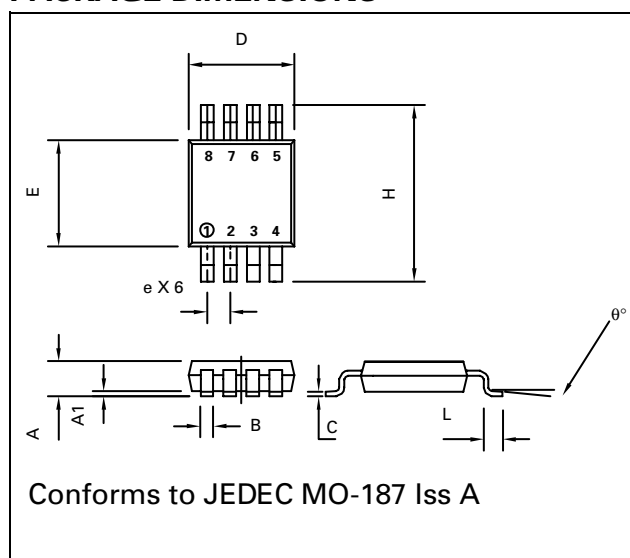
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TYPICAL CHARACTERISTICS



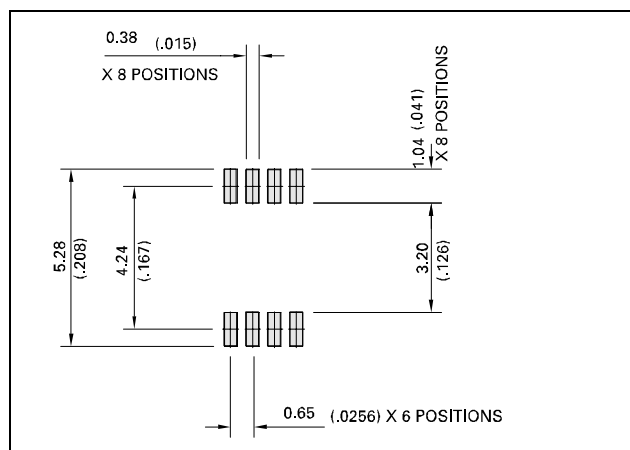
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PACKAGE DIMENSIONS



DIM	Millimetres		Inches	
	MIN	MAX	MIN	MAX
A		1.10		0.043
A1	0.05	0.15	0.002	0.006
B	0.25	0.40	0.010	0.016
C	0.13	0.23	0.005	0.009
D	2.90	3.10	0.114	0.122
e	0.65	BSC	0.0256	BSC
E	2.90	3.10	0.114	0.122
H	4.90	BSC	0.193	BSC
L	0.40	0.70	0.016	0.028
q°	0°	6°	0°	6°

PAD LAYOUT DETAILS



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PROVISIONAL ISSUE A - JULY 1999

ZETEX