35V N-CHANNEL ENHANCEMENT MODE MOSFET

SUMMARY

 $V(BR)DSS = 35V: RDS(on) = 0.050\Omega: ID = 6.7A$

DESCRIPTION

This new generation of high cell density planar MOSFETs from Zetex utilises a unique structure that combines the benefits of low on-resistance with fast switching speed. This makes them ideal for high efficiency, low voltage, power management applications.

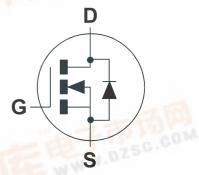


FEATURES

- · Low on-resistance
- Fast switching speed
- Low threshold
- Low gate drive
- SOT223 package

APPLICATIONS

- 50W Class D Audio Output Stage
- Motor Control

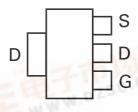


ORDERING INFORMATION

DEVICE	REEL SIZE	TAPE WIDTH	QUANTITY PER REEL
ZXM64N035GTA	7"	12mm	1000 units
ZXM64N035GTC	13"	12mm	4000 units

DEVICE MARKING

ZXM6 4N035



Top View







ABSOLUTE MAXIMUM RATING

PARAMETER	SYMBOL	LIMIT	UNIT
Drain-Source Voltage	V _{DSS}	35	V
Gate-Source Voltage	V _G S	±20	V
Continuous Drain Current ($V_{GS}=10V$; $T_{A}=25^{\circ}C$)(b) ($V_{GS}=10V$; $T_{A}=70^{\circ}C$)(b) ($V_{GS}=10V$; $T_{A}=25^{\circ}C$)(a)	ID	6.7 5.4 4.8	А
Pulsed Drain Current (c)	IDM	30	А
Continuous Source Current (Body Diode) (b)	IS	2.4	А
Pulsed Source Current (Body Diode)(c)	ISM	30	Α
Power Dissipation at T _A =25°C (a) Linear Derating Factor	PD	2.0 16	W mW/°C
Power Dissipation at T _A =25°C (b) Linear Derating Factor	PD	3.9 31	W mW/°C
Operating and Storage Temperature Range	T _j :T _{stg}	-55 to +150	°C

THERMAL RESISTANCE

PARAMETER	SYMBOL	VALUE	UNIT
Junction to Ambient (a)	R_{θ} JA	62.5	°C/W
Junction to Ambient (b)	$R_{\theta J A}$	32	°C/W

NOTES

- (a) For a device surface mounted on 25mm \times 25mm FR4 PCB with high coverage of single sided 1oz copper, in still air conditions
- (b) For a device surface mounted on FR4 PCB measured at $t \le 10$ secs.
- (c) Repetitive rating 25mm x 25mm FR4 PCB, D=0.05 pulse width limited by maximum junction temperature.



ELECTRICAL CHARACTERISTICS (at $T_A = 25$ °C unless otherwise stated).

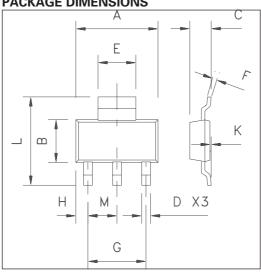
PARAMETER	SYMBOL	MIN.	TYP.	MAX.	UNIT	CONDITIONS.	
STATIC		•		•			
Drain-Source Breakdown Voltage	V(BR)DSS	35			V	I _D =250μA, V _{GS} =0V	
Zero Gate Voltage Drain Current	IDSS			1	μΑ	V _{DS} =35V, V _{GS} =0V	
Gate-Body Leakage	IGSS			100	nA	V _{GS} =±20V, V _{DS} =0V	
Gate-Source Threshold Voltage	VGS(th)	1.0			V	I _D =250μA, V _{DS} = V _{GS}	
Static Drain-Source On-State Resistance (1)	R _{DS(on)}			0.050 0.062	Ω	V _{GS} =10V, I _D =3.7A V _{GS} =4.5V, I _D =1.9A	
Forward Transconductance (1)(3)	9fs	4.3			S	V _{DS} =10V,I _D =1.9A	
DYNAMIC (3)					·		
Input Capacitance	C _{iss}		950		pF	V _{DS} =25V, V _{GS} =0V, f=1MHz	
Output Capacitance	Coss		200		pF		
Reverse Transfer Capacitance	C _{rss}		50		pF		
SWITCHING(2) (3)					•		
Turn-On Delay Time	t _{d(on)}		4.2		ns		
Rise Time	t _r		4.6		ns	V _{DD} =15V, I _D =3.7A	
Turn-Off Delay Time	td(off)		20.5		ns	RG=6.0Ω, VGS=10V	
Fall Time	tf		8		ns		
Total Gate Charge	Ωg			27	nC	V _{DS} =24V,V _{GS} =10V, I _D =3.7A	
Gate-Source Charge	αgs			5	nC		
Gate-Drain Charge	Qgd			4.5	nC		
SOURCE-DRAIN DIODE		•					
Diode Forward Voltage (1)	V _{SD}			0.95	V	TJ=25°C, IS=3.7A, VGS=0V	
Reverse Recovery Time (3)	t _{rr}		24.5		ns	T _J =25°C, I _F =3.7A, di/dt= 100A/μs	
Reverse Recovery Charge (3)	Q _{rr}		19.1		nC		

NOTES

- (1) Measured under pulsed conditions. Width=300 $\mu s.$ Duty cycle $\leq 2\%$.
- (2) Switching characteristics are independent of operating junction temperature.
- (3) For design aid only, not subject to production testing.

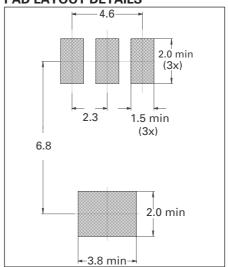


PACKAGE DIMENSIONS



DIM	Millimetres		Inches		
	Min	Max	Min	Max	
А	6.3	6.7	0.248	0.264	
В	3.3	3.7	0.130	0.146	
С	-	1.7	-	0.067	
D	0.6	0.8	0.024	0.031	
E	2.9	3.1	0.114	0.122	
F	0.24	0.32	0.009	0.13	
G	NOM 4.6		NOM 0.181		
Н	0.85	1.05	0.033	0.041	
K	0.02	0.10	0.0008	0.004	
L	6.7	7.3	0.264	0.287	
М	NOM 2.3		NOM 0.0905		

PAD LAYOUT DETAILS



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Zetex plc Fields New Road Chadderton Oldham, OL9 8NP United Kingdom Telephone (44) 161 622 4422 Fax: (44) 161 622 4420

Zetex GmbH Streitfeldstraße 19 D-81673 München

Germany Telefon: (49) 89 45 49 49 0 Fax: (49) 89 45 49 49 49

Zetex Inc 700 Veterans Memorial Hwy Hauppauge, NY11788

USA Telephone: (631) 360 2222 Fax: (631) 360 8222

Zetex (Asia) Ltd 3701-04 Metroplaza, Tower 1 Hing Fong Road Kwai Fong Hong Kong Telephone: (852) 26100 611 Fax: (852) 24250 494

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