

# Octal bus transceiver/register (3-State)

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74LVC646A

## FEATURES

- Wide supply voltage range of 1.2V to 3.6V
- Flow-through pin-out architecture
- In accordance with JEDEC standard no. 8-1A
- CMOS low power consumption
- Direct interface with TTL levels
- 5 Volt tolerant inputs/outputs, for interfacing with 5 Volt logic

## DESCRIPTION

The 74LVC646A is a high performance, low-power, low-voltage Si-gate CMOS device, superior to most advanced CMOS compatible TTL families.

Inputs can be driven from either 3.3V or 5.0V devices. In 3-State operation, outputs can handle 5V. This feature allows the use of these devices as translators in a mixed 3.3V/5V environment.

The 74LVC646A consist of non-inverting bus transceiver circuits with 3-State outputs, D-type flip-flops and control circuitry arranged

for multiplexed transmission of data directly from the internal registers. Data on the 'A' or 'B' bus will be clocked in the internal registers, as the appropriate clock (CPAB or CPBA) goes to a HIGH logic level. Output enable ( $\overline{OE}$ ) and direction (DIR) inputs are provided to control the transceiver function. In the transceiver mode, data present at the high-impedance port may be stored in either the 'A' or 'B' register, or in both. The select source inputs (SAB and SBA) can multiplex stored and real-time (transparent mode) data.

The direction (DIR) input determines which bus will receive data when  $\overline{OE}$  is active (LOW). In the isolation mode ( $OE = HIGH$ ), 'A' data may be stored in the 'B' register and/or 'B' data may be stored in the 'A' register.

When an output function is disabled, the input function is still enabled and may be used to store and transmit data. Only one of the two buses, 'A' or 'B' may be driven at a time.

The '646A' is functionally identical to the '648A' but has non-inverting data paths.

## QUICK REFERENCE DATA

GND = 0V;  $T_{amb} = 25^{\circ}C$ ;  $t_r = t_f \leq 2.5$  ns

SYMBOL	PARAMETER	CONDITIONS	TYPICAL	UNIT
$t_{PHL}/t_{PLH}$	Propagation delay An to Yn	$C_L = 50pF$ $V_{CC} = 3.3V$	3.9	ns
$f_{max}$	Maximum clock frequency		250	MHz
$C_I$	Input capacitance		5.0	pF
$C_{I/O}$	Input/output capacitance		10	pF
$C_{PD}$	Power dissipation capacitance per gate	Notes 1, 2	26	pF

### NOTES:

- $C_{PD}$  is used to determine the dynamic power dissipation ( $P_D$  in  $\mu W$ )  
 $P_D = C_{PD} \times V_{CC}^2 \times f_i + \Sigma (C_L \times V_{CC}^2 \times f_o)$  where:  
 $f_i$  = input frequency in MHz;  $C_L$  = output load capacitance in pF;  
 $f_o$  = output frequency in MHz;  $V_{CC}$  = supply voltage in V;  
 $\Sigma (C_L \times V_{CC}^2 \times f_o)$  = sum of the outputs.
- The condition is  $V_I = GND$  to  $V_{CC}$ .

## ORDERING AND PACKAGE INFORMATION

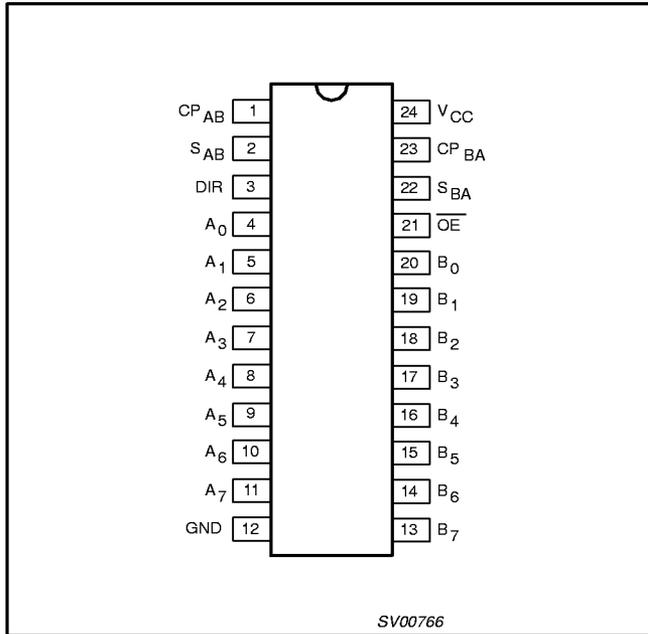
PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	PKG. DWG. #
24-Pin Plastic SO	-40°C to +85°C	74LVC646A D	74LVC646A D	SOT137-1
24-Pin Plastic SSOP Type II	-40°C to +85°C	74LVC646A DB	74LVC646A DB	SOT340-1
24-Pin Plastic TSSOP Type I	-40°C to +85°C	74LVC646A PW	7LVC646APW DH	SOT355-1

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# 74LVC646A

## PIN CONFIGURATION



## PIN DESCRIPTION

PIN NUMBER	SYMBOL	FUNCTION
1	CP <sub>AB</sub>	'A' to 'B' clock input (LOW-to-HIGH, edge-triggered)
2	S <sub>AB</sub>	Select 'A' to 'B' source input
3	DIR	Direction control input
4, 5, 6, 7, 8, 9, 10, 11	A <sub>0</sub> to A <sub>7</sub>	'A' data inputs/outputs
12	GND	Ground (0V)
20, 19, 18, 17, 16, 15, 14, 13	B <sub>0</sub> to B <sub>7</sub>	'B' data inputs/outputs
21	$\overline{OE}$	Output enable input (active LOW)
22	S <sub>BA</sub>	Select 'B' to 'A' source input
23	CP <sub>BA</sub>	'B' to 'A' clock input (LOW-to-HIGH, edge-triggered)
24	V <sub>CC</sub>	Positive supply voltage

## FUNCTION TABLE

INPUTS						DATA I/O *		FUNCTION
$\overline{OE}$	DIR	CP <sub>AB</sub>	CP <sub>BA</sub>	S <sub>AB</sub>	S <sub>BA</sub>	A <sub>0</sub> to A <sub>7</sub>	B <sub>0</sub> to B <sub>7</sub>	
X	X	↑	X	X	X	input	un *	store A, B unspecified *
X	X	X	↑	X	X	un *	input	store B, A unspecified *
H	X	↑	↑	X	X	input	input	store A and B data, isolation hold storage
H	X	H or L	H or L	X	X			
L	L	X	X	X	L	output	input	real-time B data to A bus
L	L	X	H or L	X	H			stored B data to A bus
L	H	X	X	L	X	input	output	real-time A data to B bus
L	H	H or L	X	H	X			stored A data to B bus

\* The data output functions may be enabled or disabled by various signals at the  $\overline{OE}$  and DIR inputs. Data input functions are always enabled, i.e., data at the bus inputs will be stored on every LOW-to-HIGH transition on the clock inputs.

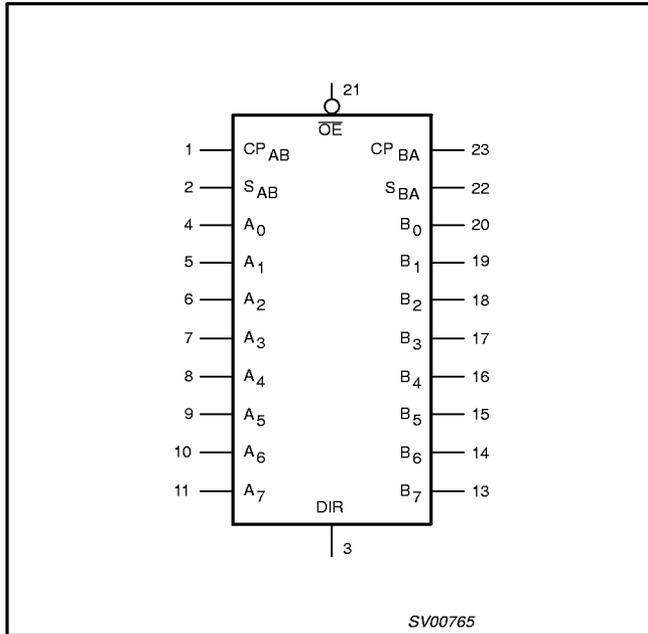
- un = unspecified
- H = HIGH voltage level
- L = LOW voltage level
- X = Don't care
- ↑ = LOW-to-HIGH level transition

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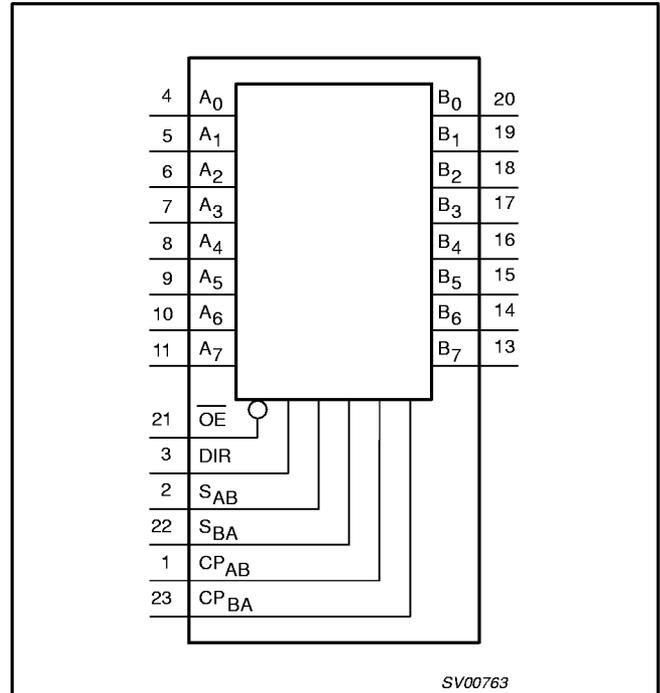
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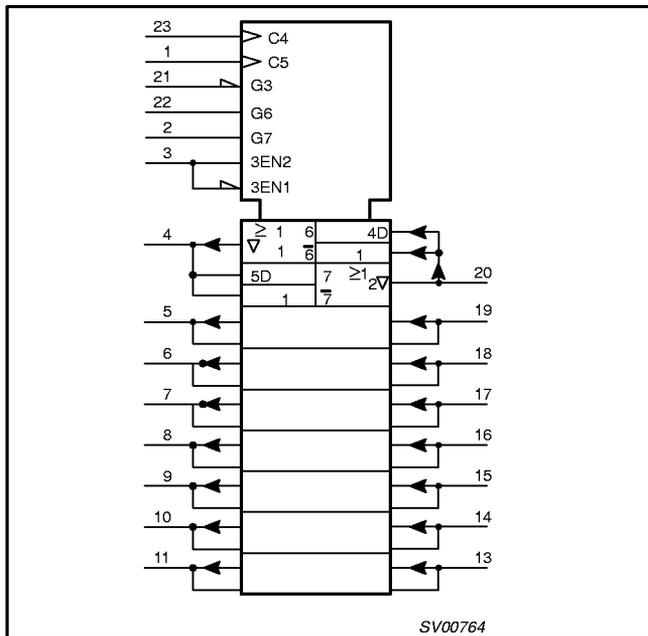
LOGIC SYMBOL



FUNCTIONAL DIAGRAM



LOGIC SYMBOL (IEEE/IEC)

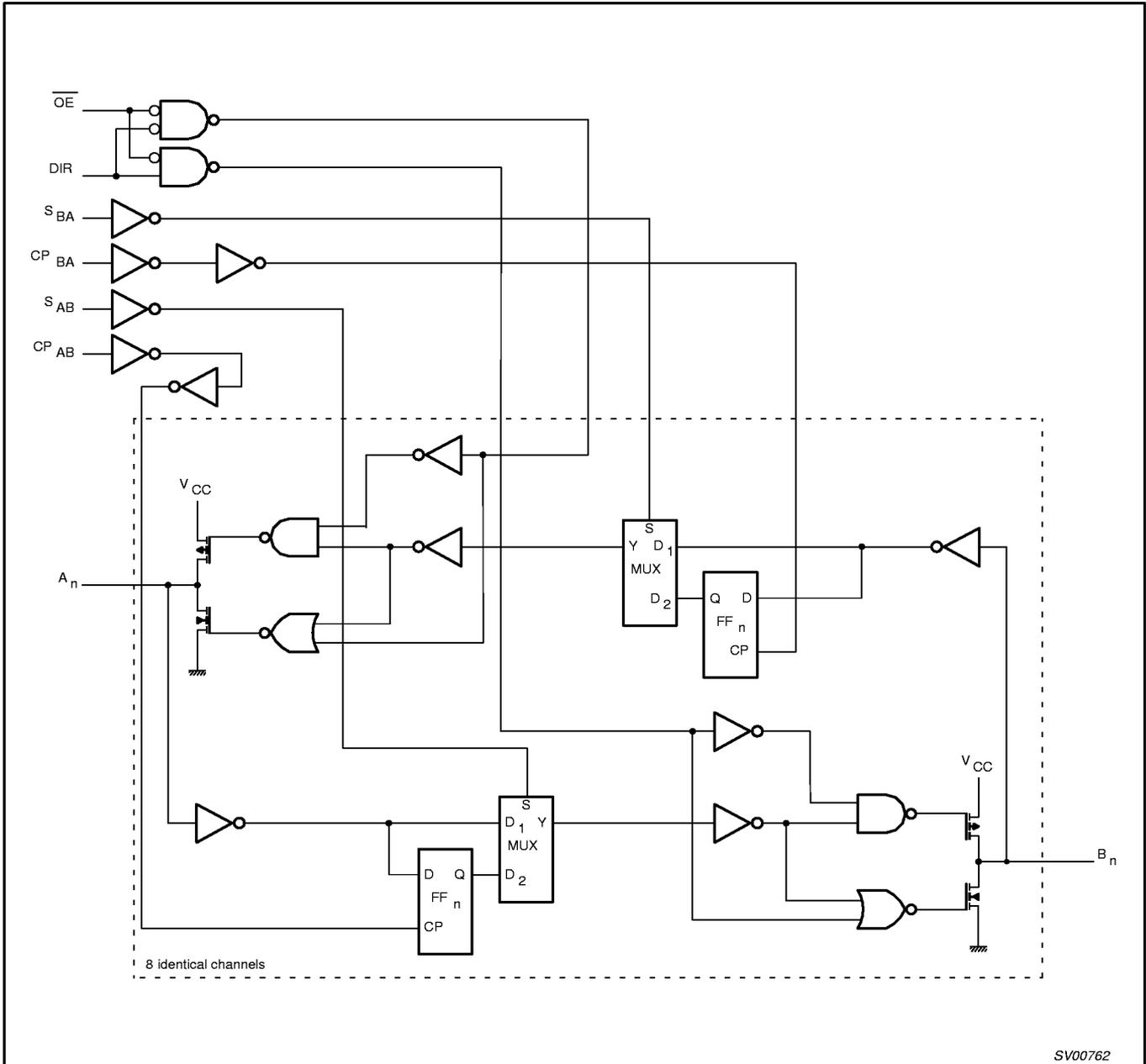


# Octal bus transceiver/register (3-State)

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### LOGIC DIAGRAM



SV00762

## Octal bus transceiver/register (3-State)

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## RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	CONDITIONS	LIMITS		UNIT
			MIN	MAX	
$V_{CC}$	DC supply voltage (for max. speed performance)		2.7	3.6	V
	DC supply voltage (for low-voltage applications)		1.2	3.6	
$V_I$	DC input voltage range		0	5.5	V
$V_O$	DC output voltage range; output HIGH or LOW state		0	$V_{CC}$	V
	DC output voltage range; output 3-State		0	5.5	
$T_{amb}$	Operating free-air temperature range		-40	+85	°C
$t_r, t_f$	Input rise and fall times	$V_{CC} = 1.2$ to $2.7V$ $V_{CC} = 2.7$ to $3.6V$	0	20 10	ns/V

ABSOLUTE MAXIMUM RATINGS<sup>1</sup>

In accordance with the Absolute Maximum Rating System (IEC 134)

Voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
$V_{CC}$	DC supply voltage		-0.5 to +6.5	V
$I_{IK}$	DC input diode current	$V_I < 0$	-50	mA
$V_I$	DC input voltage	Note 2	-0.5 to +6.5	V
$I_{OK}$	DC output diode current	$V_O > V_{CC}$ or $V_O < 0$	±50	mA
$V_O$	DC output voltage; output HIGH or LOW	Note 2	-0.5 to $V_{CC} + 0.5$	V
	DC output voltage; output 3-State	Note 2	-0.5 to 6.5	
$I_O$	DC output diode current	$V_O = 0$ to $V_{CC}$	±50	mA
$I_{GND}, I_{CC}$	DC $V_{CC}$ or GND current		±100	mA
$T_{stg}$	Storage temperature range		-65 to +150	°C
$P_{TOT}$	Power dissipation per package – plastic mini-pack (SO) – plastic shrink mini-pack (SSOP and TSSOP)	above +70°C derate linearly with 8 mW/K	500	mW
		above +60°C derate linearly with 5.5 mW/K	500	

## NOTES:

- Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

## Octal bus transceiver/register (3-State)

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Over recommended operating conditions voltages are referenced to GND (ground = 0V)

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Temp = -40°C to +85°C			
			MIN	TYP <sup>1</sup>	MAX	
V <sub>IH</sub>	HIGH level Input voltage	V <sub>CC</sub> = 1.2V	V <sub>CC</sub>			V
		V <sub>CC</sub> = 2.7 to 3.6V	2.0			
V <sub>IL</sub>	LOW level Input voltage	V <sub>CC</sub> = 1.2V			GND	V
		V <sub>CC</sub> = 2.7 to 3.6V			0.8	
V <sub>OH</sub>	HIGH level output voltage	V <sub>CC</sub> = 2.7V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = -12mA	V <sub>CC</sub> - 0.5			V
		V <sub>CC</sub> = 3.0V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = -100μA	V <sub>CC</sub> - 0.2	V <sub>CC</sub>		
		V <sub>CC</sub> = 3.0V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = -18mA	V <sub>CC</sub> - 0.6			
		V <sub>CC</sub> = 3.0V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = -24mA	V <sub>CC</sub> - 0.8			
V <sub>OL</sub>	LOW level output voltage	V <sub>CC</sub> = 2.7V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = 12mA			0.40	V
		V <sub>CC</sub> = 3.0V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = 100μA		GND	0.20	
		V <sub>CC</sub> = 3.0V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; I <sub>O</sub> = 24mA			0.55	
I <sub>I</sub>	Input leakage current	V <sub>CC</sub> = 3.6V; V <sub>I</sub> = 5.5V or GND   Not for I/O pins		±0.1	±5	μA
I <sub>IHZ</sub> /I <sub>ILZ</sub>	Input current for common I/O pins	V <sub>CC</sub> = 3.6V; V <sub>I</sub> = V <sub>CC</sub> or GND		±0.1	±15	μA
I <sub>OZ</sub>	3-State output OFF-state current	V <sub>CC</sub> = 3.6V; V <sub>I</sub> = V <sub>IH</sub> or V <sub>IL</sub> ; V <sub>O</sub> = 5.5V or GND		0.1	±10	μA
I <sub>OFF</sub>	Power off leakage current	V <sub>CC</sub> = 0.0V; V <sub>I</sub> or V <sub>O</sub> = 5.5V		0.1	±10	μA
I <sub>CC</sub>	Quiescent supply current	V <sub>CC</sub> = 3.6V; V <sub>I</sub> = V <sub>CC</sub> or GND; I <sub>O</sub> = 0		0.1	10	μA
ΔI <sub>CC</sub>	Additional quiescent supply current per input pin	V <sub>CC</sub> = 2.7V to 3.6V; V <sub>I</sub> = V <sub>CC</sub> - 0.6V; I <sub>O</sub> = 0		5	500	μA

**NOTES:**1. All typical values are at V<sub>CC</sub> = 3.3V and T<sub>amb</sub> = 25°C.

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**AC CHARACTERISTICS**

GND = 0 V;  $t_r = t_f \leq 2.5$  ns;  $C_L = 50$  pF

SYMBOL	PARAMETER	WAVEFORM	LIMITS						UNIT
			$V_{CC} = 3.3V \pm 0.3V$			$V_{CC} = 2.7V$		$V_{CC} = 1.2V$	
			MIN	TYP <sup>1</sup>	MAX	MIN	MAX	TYP	
$t_{PHL}/t_{PLH}$	Propagation delay An, Bn to Bn, An	Figures 1, 6	1.5	3.9	6.8	1.5	7.8	15	ns
$t_{PHL}/t_{PLH}$	Propagation delay CP <sub>AB</sub> , CP <sub>BA</sub> to B <sub>n</sub> , A <sub>n</sub>	Figures 2, 6	1.5	4.6	7.6	1.5	8.6	19	ns
$t_{PHL}/t_{PLH}$	Propagation delay S <sub>AB</sub> , S <sub>BA</sub> to B <sub>n</sub> , A <sub>n</sub>	Figures 3, 6	1.5	4.9	8.5	1.5	9.5	19	ns
$t_{PZH}/t_{PZL}$	3-State output enable time OEn to An, Bn	Figures 4, 6	1.5	4.5	7.8	1.5	8.8	20	ns
$t_{PHZ}/t_{PLZ}$	3-State output disable time OEn to An, Bn	Figures 4, 6	1.5	3.9	6.1	1.5	7.1	10	ns
$t_{PZH}/t_{PZL}$	3-State output enable time DIR to An, Bn	Figures 5, 6	1.5	4.6	7.9	1.5	8.9	20	ns
$t_{PHZ}/t_{PLZ}$	3-State output disable time DIR to An, Bn	Figures 5, 6	1.5	3.5	6.0	1.5	7.0	12	ns
$t_w$	Clock pulse width HIGH or LOW CP <sub>AB</sub> or CP <sub>BA</sub>	Figure 1, 3	3.3	1.9	–	3.3	–	–	ns
$t_{su}$	Set-up time An, Bn to CP <sub>AB</sub> , CP <sub>BA</sub>	Figure 2	1.6	0.35	–	1.6	–	–	ns
$t_h$	Hold time An, Bn to CP <sub>AB</sub> , CP <sub>BA</sub>	Figure 2	1.0	–0.3	–	1.0	–	–	ns
$f_{max}$	Maximum clock pulse frequency	Figure 2	150	250	–	125	–	–	ns

**NOTE:**

1. These typical values are at  $V_{CC} = 3.3V$  and  $T_{amb} = 25^\circ C$ .

# Octal bus transceiver/register (3-State)

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# 74LVC646A

## AC WAVEFORMS

$V_M = 1.5V$  at  $V_{CC} \geq 2.7V$   
 $V_M = 0.5V \cdot V_{CC}$  at  $V_{CC} < 2.7V$   
 $V_{OL}$  and  $V_{OH}$  are the typical output voltage drop that occur with the output load.  
 $V_X = V_{OL} + 0.3V$  at  $V_{CC} \geq 2.7V$   
 $V_X = V_{OL} + 0.1V_{CC}$  at  $V_{CC} < 2.7V$   
 $V_Y = V_{OH} - 0.3V$  at  $V_{CC} \geq 2.7V$   
 $V_Y = V_{OH} - 0.1V_{CC}$  at  $V_{CC} < 2.7V$

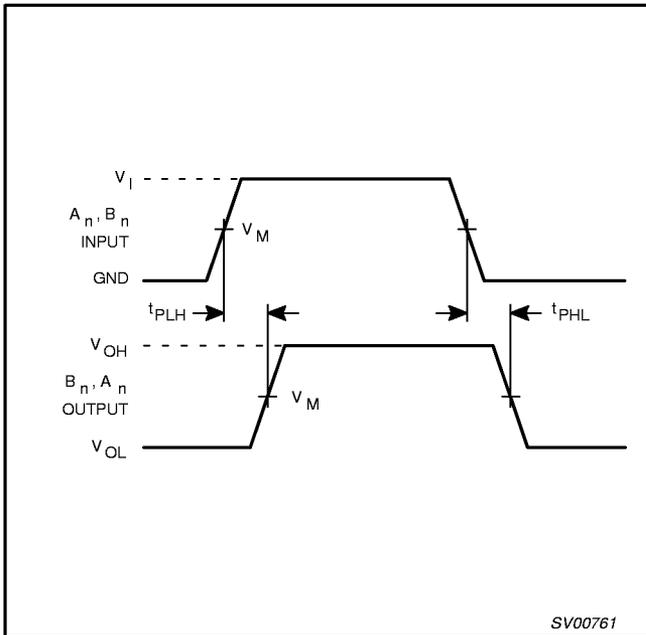


Figure 1. Input  $A_n, B_n$  to output  $B_n, A_n$  propagation delays.

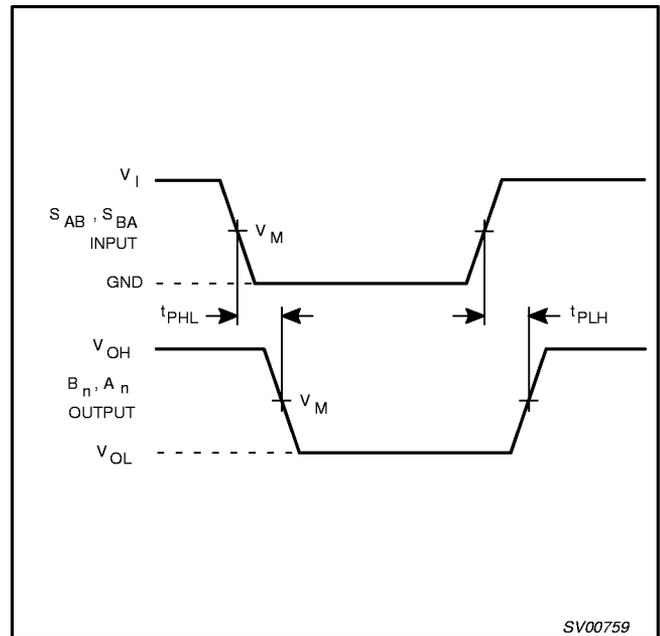


Figure 3. Input  $S_{AB}, S_{BA}$  to output  $B_n, A_n$  propagation delay times.

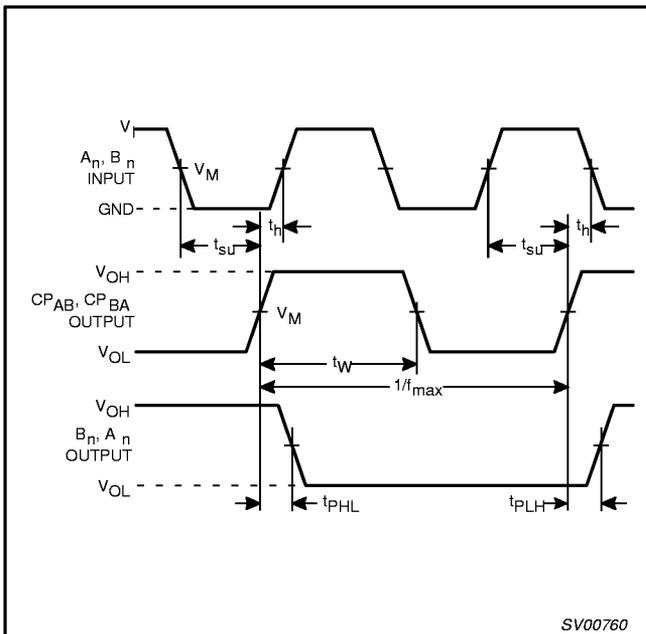


Figure 2.  $A_n, B_n$  to  $CP_{AB}, CP_{BA}$  set-up and hold times, clock  $CP_{AB}, CP_{BA}$  pulse width, maximum clock pulse frequency and the  $CP_{AB}, CP_{BA}$  to output  $B_n, A_n$  propagation delays.

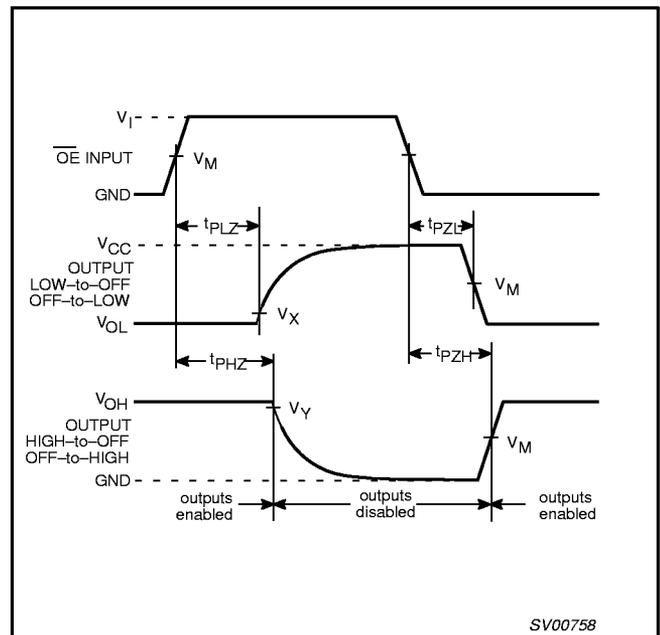


Figure 4. Input  $\overline{OE}$  to output  $A_n, B_n$  3-State enable and disable times.

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## AC WAVEFORMS (Continued)

- $V_M = 1.5V$  at  $V_{CC} \geq 2.7V$
- $V_M = 0.5V \cdot V_{CC}$  at  $V_{CC} < 2.7V$
- $V_{OL}$  and  $V_{OH}$  are the typical output voltage drop that occur with the output load.
- $V_X = V_{OL} + 0.3V$  at  $V_{CC} \geq 2.7V$
- $V_X = V_{OL} + 0.1V_{CC}$  at  $V_{CC} < 2.7V$
- $V_Y = V_{OH} - 0.3V$  at  $V_{CC} \geq 2.7V$
- $V_Y = V_{OH} - 0.1V_{CC}$  at  $V_{CC} < 2.7V$

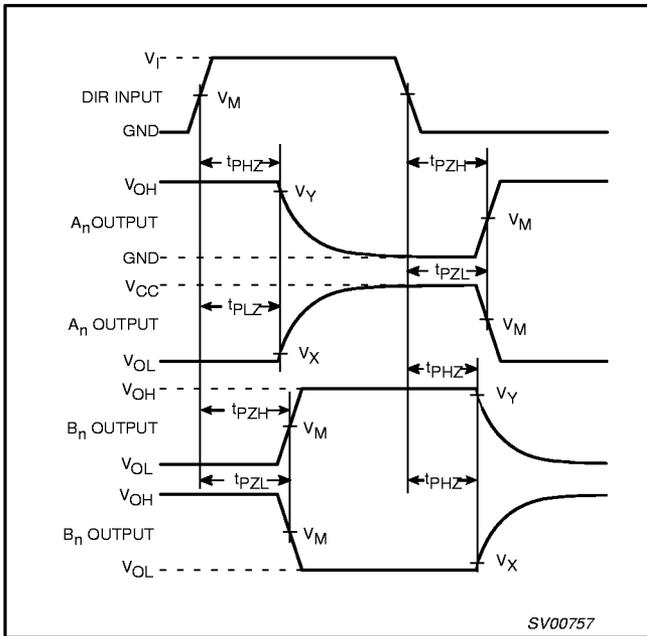


Figure 5. Input DIR to output A<sub>n</sub>, B<sub>n</sub> 3-State enable and disable times.

## TEST CIRCUIT

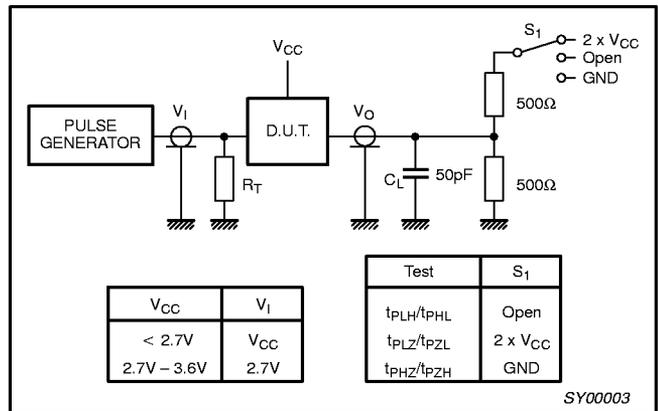


Figure 6. Load circuitry for switching times.

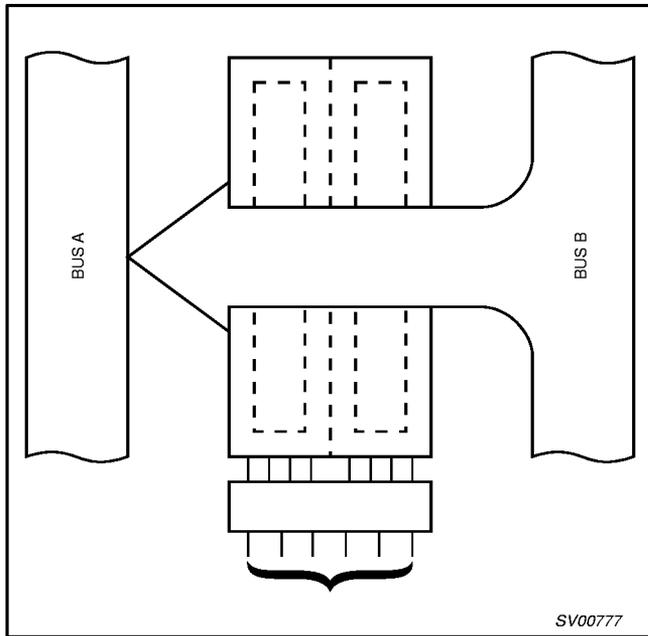
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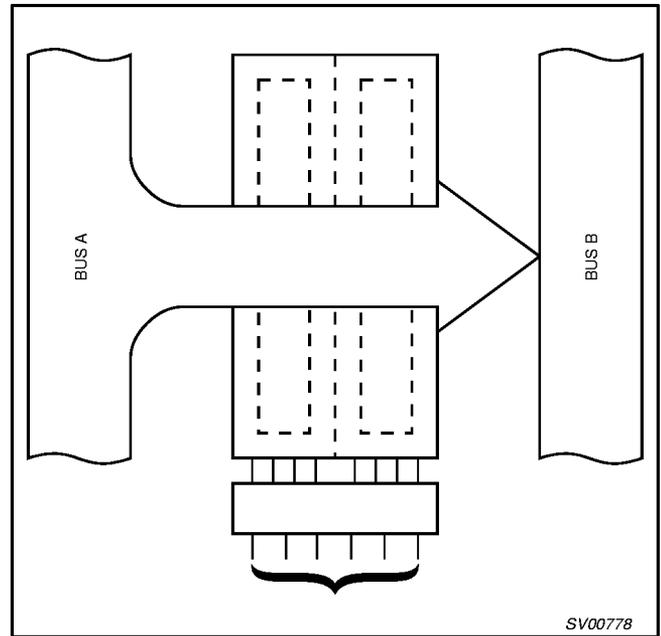
## APPLICATION INFORMATION

Real-time transfer; bus B to bus A



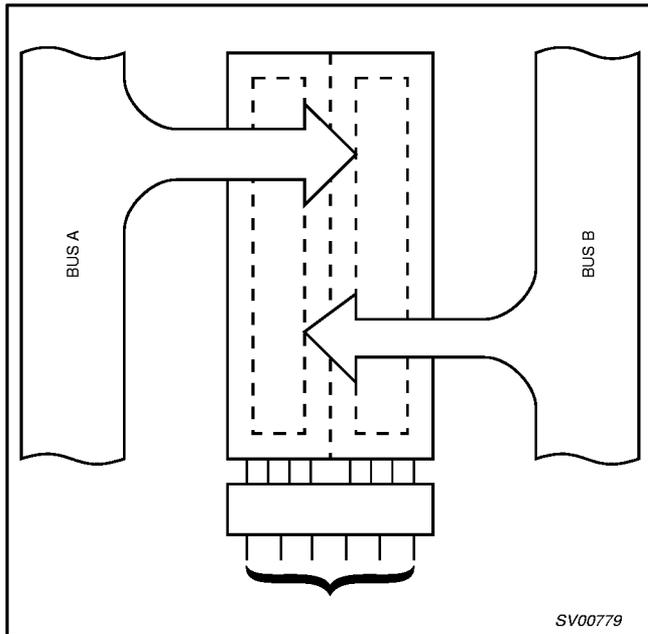
(1)	(14)	(28)	(16)	(27)	(15)
$\overline{OE}$	DIR	CP <sub>AB</sub>	CP <sub>BA</sub>	S <sub>AB</sub>	S <sub>BA</sub>
L	L	X	X	X	L

Real-time transfer; bus A to bus B



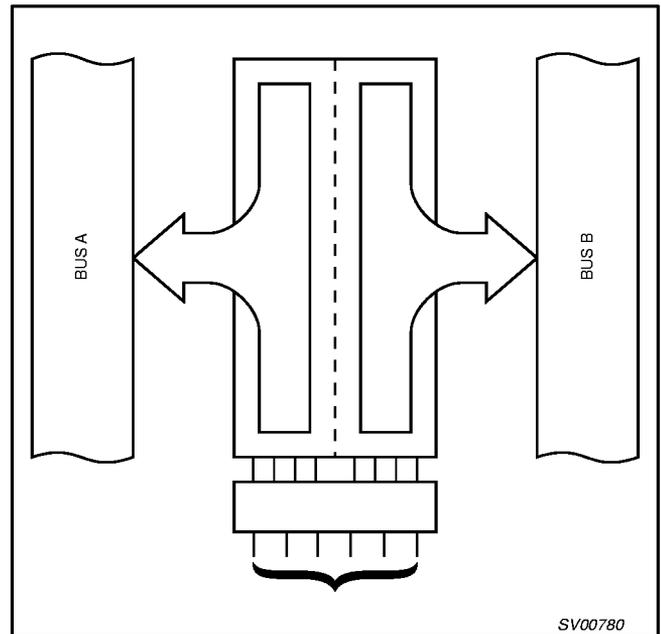
(1)	(14)	(28)	(16)	(27)	(15)
$\overline{OE}$	DIR	CP <sub>AB</sub>	CP <sub>BA</sub>	S <sub>AB</sub>	S <sub>BA</sub>
L	H	X	X	L	X

Storage from A, B or A and B



(1)	(14)	(28)	(16)	(27)	(15)
$\overline{OE}$	DIR	CP <sub>AB</sub>	CP <sub>BA</sub>	S <sub>AB</sub>	S <sub>BA</sub>
X	X	↑	X	X	X
X	X	X	↑	X	L
H	X	↑	↑	X	X

Transfer storage data to A or B



(1)	(14)	(28)	(16)	(27)	(15)
$\overline{OE}$	DIR	CP <sub>AB</sub>	CP <sub>BA</sub>	S <sub>AB</sub>	S <sub>BA</sub>
L	L	X	H or L	X	H
L	H	H or L	X	H	X

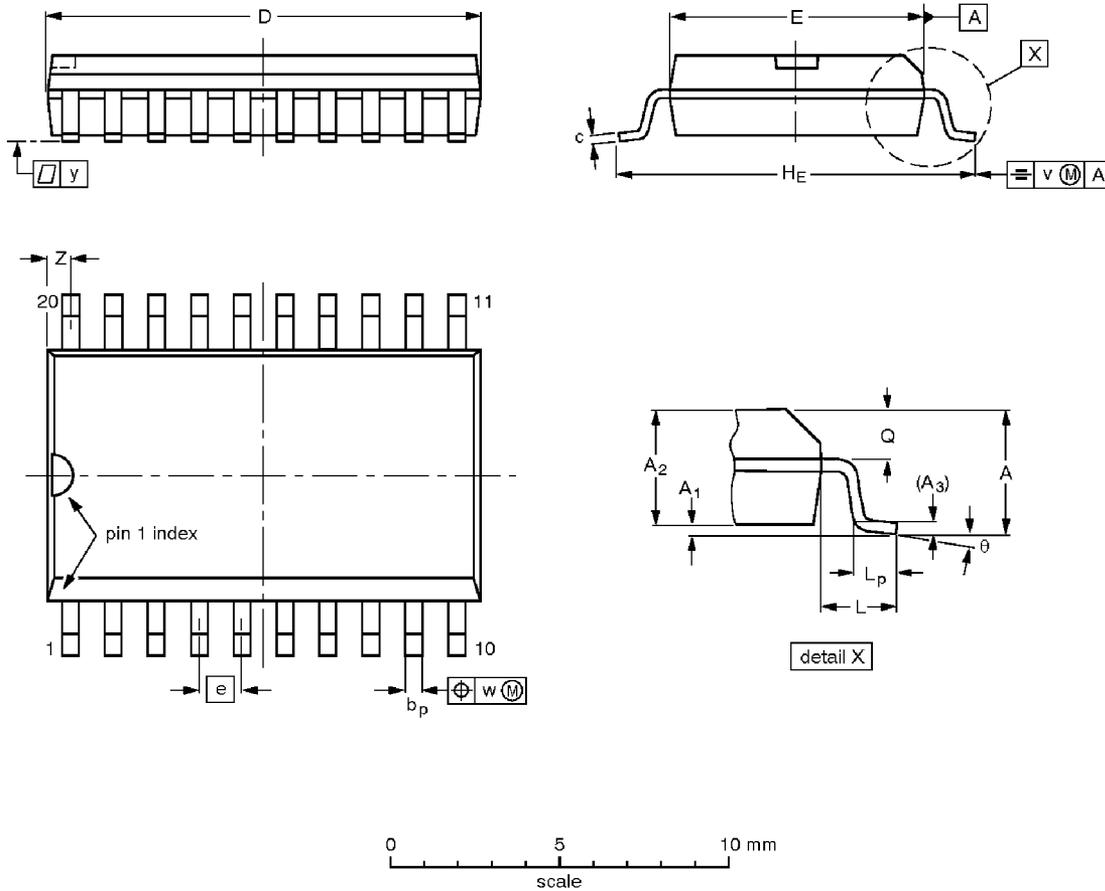
Octal bus transceiver/register (3-State)

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SO20: plastic small outline package; 20 leads; body width 7.5 mm

SOT163-1



**DIMENSIONS** (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	θ
mm	2.65	0.30 0.10	2.45 2.25	0.25	0.49 0.36	0.32 0.23	13.0 12.6	7.6 7.4	1.27	10.65 10.00	1.4	1.1 0.4	1.1 1.0	0.25	0.25	0.1	0.9 0.4	8° 0°
inches	0.10	0.012 0.004	0.096 0.089	0.01	0.019 0.014	0.013 0.009	0.51 0.49	0.30 0.29	0.050	0.42 0.39	0.055	0.043 0.016	0.043 0.039	0.01	0.01	0.004	0.035 0.016	

**Note**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT163-1	075E04	MS-013AC				92-11-17 95-01-24

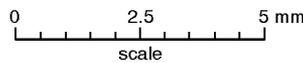
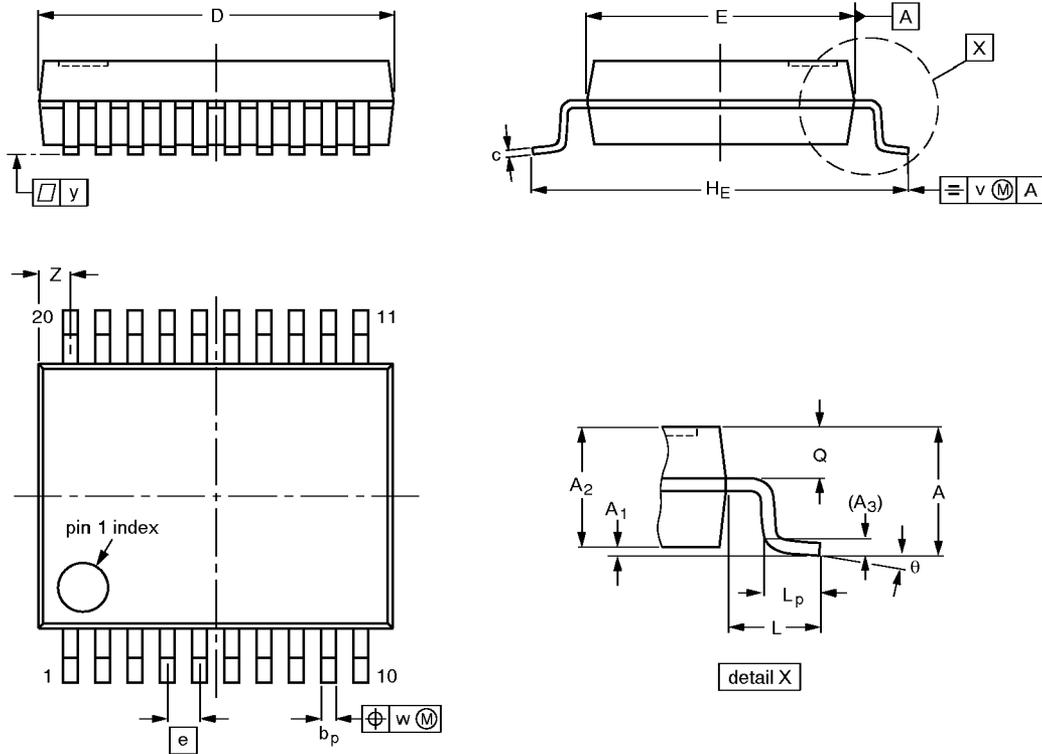
Octal bus transceiver/register (3-State)

74LVC646A

[查询74LVC646ADB-T 供应商](#)

SSOP20: plastic shrink small outline package; 20 leads; body width 5.3 mm

SOT339-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	θ
mm	2.0	0.21 0.05	1.80 1.65	0.25	0.38 0.25	0.20 0.09	7.4 7.0	5.4 5.2	0.65	7.9 7.6	1.25	1.03 0.63	0.9 0.7	0.2	0.13	0.1	0.9 0.5	8° 0°

Note

1. Plastic or metal protrusions of 0.20 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT339-1		MO-150AE				93-09-08 95-02-04

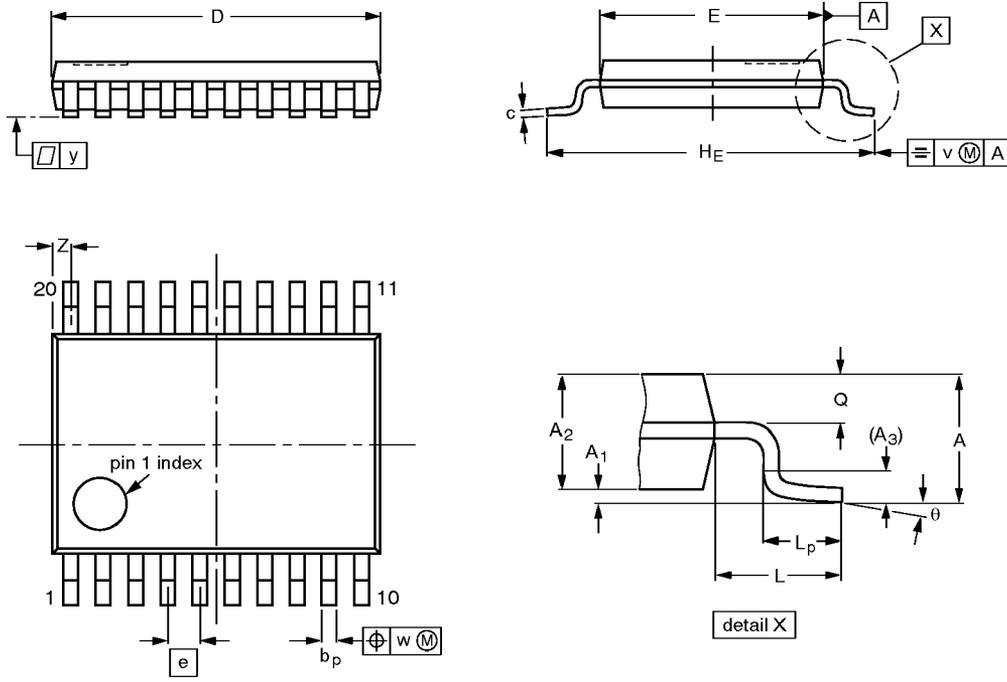
Octal bus transceiver/register (3-State)

74LVC646A

[查询74LVC646ADB-T 供应商](#)

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm

SOT360-1



**DIMENSIONS (mm are the original dimensions)**

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(2)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	θ
mm	1.10	0.15 0.05	0.95 0.80	0.25	0.30 0.19	0.2 0.1	6.6 6.4	4.5 4.3	0.65	6.6 6.2	1.0	0.75 0.50	0.4 0.3	0.2	0.13	0.1	0.5 0.2	8° 0°

**Notes**

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT360-1		MO-153AC				93-06-16 95-02-04