



May 1988
Revised August 1999

74F381

4-Bit Arithmetic Logic Unit

General Description

The 74F381 performs three arithmetic and three logic operations on two 4-bit words, A and B. Two additional select input codes force the function outputs LOW or HIGH. Carry propagate and generate outputs are provided for use with the 74F182 carry lookahead generator for high-speed expansion to longer word lengths. For ripple expansion, refer to the 74F382 ALU data sheet.

Features

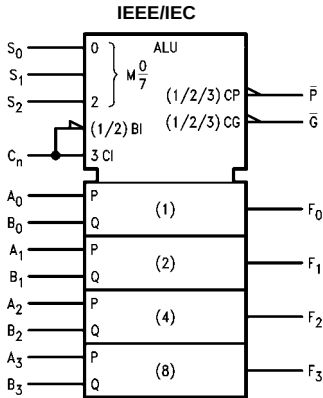
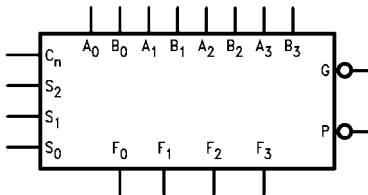
- Low input loading minimizes drive requirements
- Performs six arithmetic and logic functions
- Selectable LOW (clear) and HIGH (preset) functions
- Carry generate and propagate outputs for use with carry lookahead generator

Ordering Code:

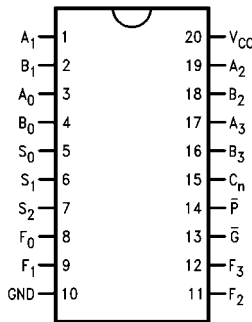
Order Number	Package Number	Package Description
74F381SC	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide
74F381SJ	M20D	20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74F381PC	N20A	20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Logic Symbols



Connection Diagram



74F381 4-Bit Arithmetic Logic Unit

Pin Names	Description	U.L. HIGH/LOW	Input I_{IH}/I_{IL} Output I_{OH}/I_{OL}
A ₀ –A ₃	A Operand Inputs	1.0/3.0	20 μ A/–1.8 mA
B ₀ –B ₃	B Operand Inputs	1.0/3.0	20 μ A/–1.8 mA
S ₀ –S ₂	Function Select Inputs	1.0/1.0	20 μ A/–0.6 mA
C _n	Carry Input	1.0/4.0	20 μ A/–2.4 mA
$\overline{G}$	Carry Generate Output (Active LOW)	50/33.3	–1 mA/20 mA
$\overline{P}$	Carry Propagate Output (Active LOW)	50/33.3	–1 mA/20 mA
F ₀ –F ₃	Function Outputs	50/33.3	–1 mA/20 mA

Select			Operation
S ₀	S ₁	S ₂	
L	L	L	Clear
H	L	L	B Minus A
L	H	L	A Minus B
H	H	L	A Plus B
L	L	H	$A \oplus B$
H	L	H	$A + B$
L	H	H	AB
H	H	H	Preset

Path Segment	Toward F	Output C _n + 4, OVR
A _i or B _i to $\overline{P}$	7.2 ns	7.2 ns
$\overline{P}_i$ to C _n + ('F182)	6.2 ns	6.2 ns
C _n to F	8.1 ns	—
C _n or C _n + 4, OVR	—	8.0 ns
Total Delay	21.5 ns	21.4 ns

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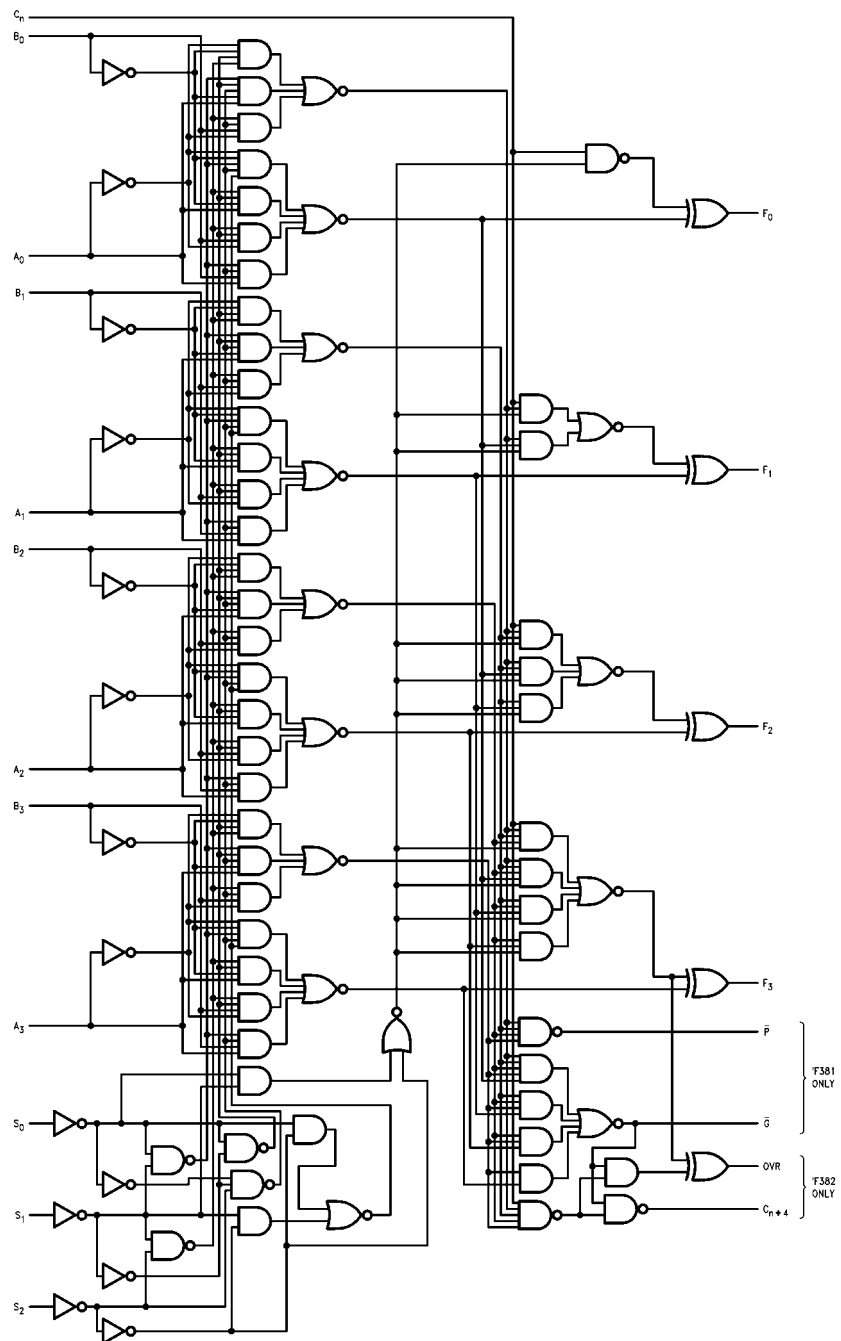
Truth Table

	Inputs						Outputs					
Function	S ₀	S ₁	S ₂	C _n	A _n	B _n	F ₀	F ₁	F ₂	F ₃	$\overline{G}$	$\overline{P}$
CLEAR	L	L	L	X	X	X	L	L	L	L	L	L
B Minus A	H	L	L	L	L	L	H	H	H	H	H	L
				L	L	H	L	H	H	H	L	L
				L	H	L	L	L	L	L	H	H
				L	H	H	H	H	H	H	H	L
				H	L	L	L	L	L	L	H	L
				H	L	H	H	H	H	H	L	L
				H	H	L	H	L	L	L	H	H
				H	H	H	L	L	L	L	H	L
A Minus B	L	H	L	L	L	L	H	H	H	H	H	L
				L	L	H	L	L	L	L	H	H
				L	H	L	L	H	H	H	L	L
				L	H	H	H	H	H	H	H	L
				H	L	L	L	L	L	L	H	L
				H	L	H	H	L	L	L	H	H
				H	H	L	L	H	H	H	L	L
				H	H	H	L	L	L	L	H	L
A Plus B	H	H	L	L	L	L	L	L	L	L	H	H
				L	L	H	H	H	H	H	H	L
				L	H	L	H	H	H	H	L	L
				L	H	H	L	H	H	H	H	H
				H	L	L	L	L	L	L	H	L
				H	L	H	L	L	L	L	H	L
				H	H	L	L	L	L	L	H	L
				H	H	H	H	H	H	H	L	L
A ⊕ B	L	L	H	X	L	L	L	L	L	L	H	H
				X	L	H	H	H	H	H	H	H
				X	H	L	H	H	H	H	H	L
				X	H	H	L	L	L	L	L	L
A + B	H	L	H	X	L	L	L	L	L	L	H	H
				X	L	H	H	H	H	H	H	H
				X	H	L	H	H	H	H	H	H
				X	H	H	H	H	H	H	H	L
AB	L	H	H	X	L	L	L	L	L	L	L	L
				X	L	H	L	L	L	L	H	H
				X	H	L	L	L	L	L	L	L
				X	H	H	H	H	H	H	H	L
PRESET	H	H	H	X	L	L	H	H	H	H	H	H
				X	L	H	H	H	H	H	H	H
				X	H	L	H	H	H	H	H	H
				X	H	H	H	H	H	H	H	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial

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Logic Diagram



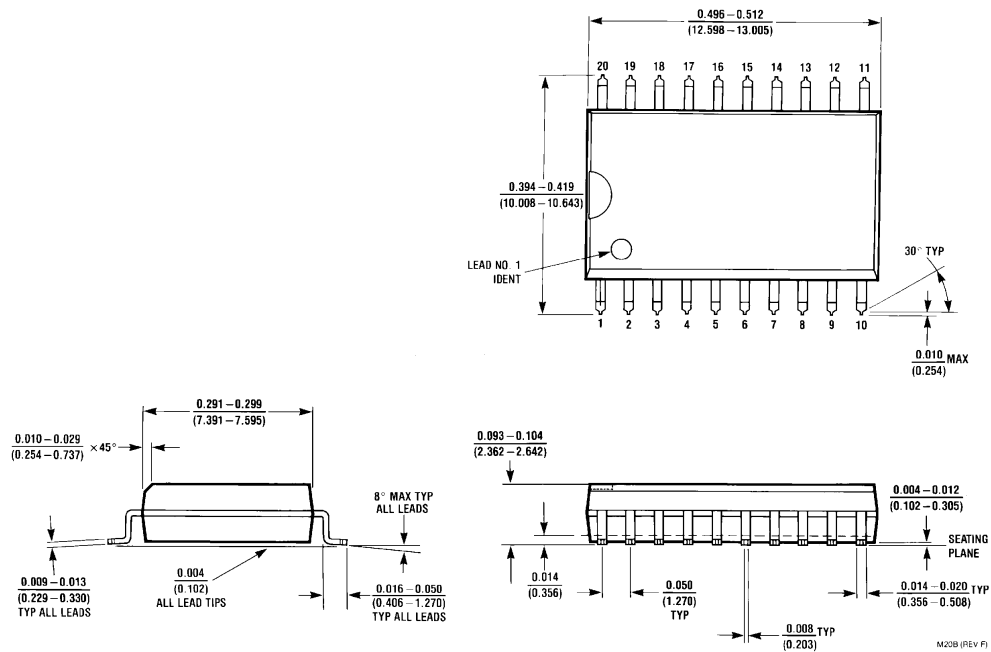
Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings ^(Note 1)				Recommended Operating Conditions			
Storage Temperature		-65°C to +150°C		Free Air Ambient Temperature		0°C to +70°C	
Ambient Temperature under Bias		-55°C to +125°C		Supply Voltage		+4.5V to +5.5V	
Junction Temperature under Bias		-55°C to +150°C					
V _{CC} Pin Potential to Ground Pin		-0.5V to +7.0V					
Input Voltage (Note 2)		-0.5V to +7.0V					
Input Current (Note 2)		-30 mA to +5.0 mA					
Voltage Applied to Output							
in HIGH State (with V _{CC} = 0V)							
Standard Output		-0.5V to V _{CC}					
3-STATE Output		-0.5V to +5.5V					
Current Applied to Output							
in LOW State (Max)		twice the rated I _{OL} (mA)					
Note 1: Absolute maximum ratings are values beyond which the device may be damaged or have its useful life impaired. Functional operation under these conditions is not implied. Note 2: Either voltage limit or current limit is sufficient to protect inputs.							
DC Electrical Characteristics							
Symbol	Parameter	Min	Typ	Max	Units	V _{CC}	Conditions
V _{IH}	Input HIGH Voltage	2.0			V		Recognized as a HIGH Signal
V _{IL}	Input LOW Voltage			0.8	V		Recognized as a LOW Signal
V _{CD}	Input Clamp Diode Voltage			-1.2	V	Min	I _{IN} = -18 mA
V _{OH}	Output HIGH Voltage	10% V _{CC} 5% V _{CC}	2.5 2.7		V	Min	I _{OH} = -1 mA I _{OH} = -1 mA
V _{OL}	Output LOW Voltage	10% V _{CC}		0.5	V	Min	I _{OL} = 20 mA
I _{IH}	Input HIGH Current			5.0	μA		V _{IN} = 2.7V
I _{BVI}	Input HIGH Current Breakdown Test			7.0	μA	Max	V _{IN} = 7.0V
I _{CEX}	Output HIGH Leakage Current			50	μA	Max	V _{OUT} = V _{CC}
V _{ID}	Input Leakage Test	4.75			V	0.0	I _{ID} = 1.9 μA All Other Pins Grounded
I _{OD}	Output Leakage Circuit Current			3.75	μA	0.0	V _{IOD} = 150 mV All Other Pins Grounded
I _{IL}	Input LOW Current			-0.6 -1.8 -2.4	mA mA mA	Max Max Max	V _{IN} = 0.5V (S _n) V _{IN} = 0.5V (A _n , B _n) V _{IN} = 0.5V (C _n)
I _{OS}	Output Short-Circuit Current	-60		-150	mA	Max	V _{OUT} = 0V
I _{CC}	Power Supply Current		59	89	mA	Max	

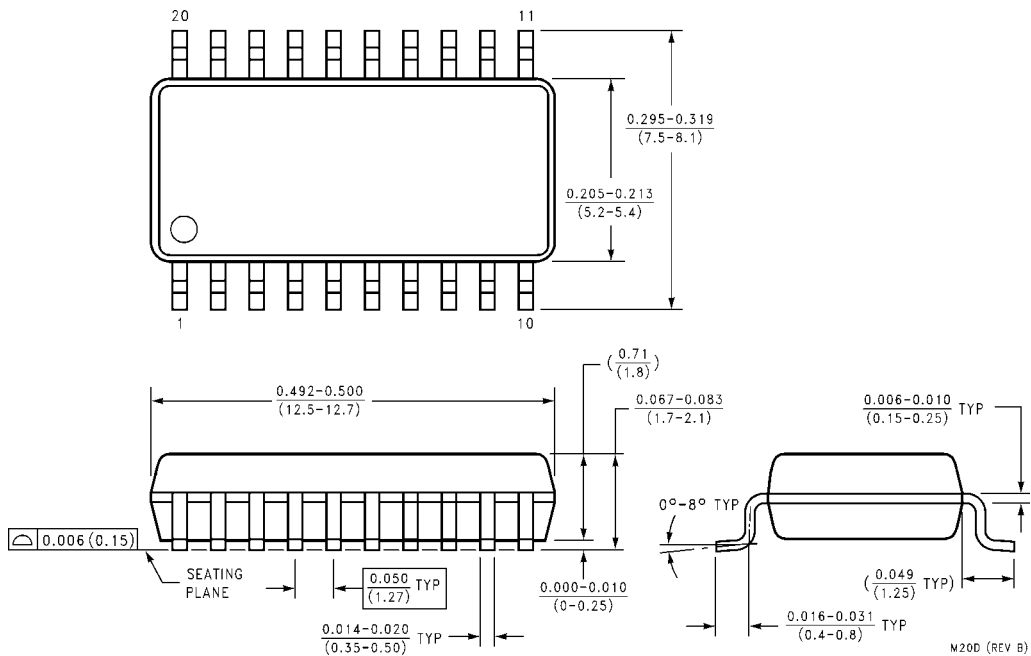
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AC Electrical Characteristics							
Symbol	Parameter	T _A = +25°C V _{CC} = +5.0V C _L = 50 pF			T _A = 0°C to +70°C V _{CC} = +5.0V C _L = 50 pF		Units
		Min	Typ	Max	Min	Max	
t _{PLH}	Propagation Delay	2.5	8.1	12.0	2.5	13.0	ns
t _{PHL}	C _n to F _i	2.5	5.7	8.0	2.5	9.0	
t _{PLH}	Propagation Delay	4.0	10.4	15.0	4.0	16.0	ns
t _{PHL}	Any A or B to Any F	3.5	8.2	11.0	3.5	12.0	
t _{PLH}	Propagation Delay	4.5	8.3	20.5	4.5	21.5	ns
t _{PHL}	S _i to F _i	4.0	8.2	15.0	4.0	16.0	
t _{PLH}	Propagation Delay	3.5	6.4	10.0	3.5	11.0	ns
t _{PHL}	A _i or B _i to $\overline{G}$	3.5	6.8	10.0	3.0	11.0	
t _{PLH}	Propagation Delay	2.5	7.2	10.5	2.5	11.5	ns
t _{PHL}	A _i or B _i to $\overline{P}$	3.5	6.5	9.5	3.5	10.5	
t _{PLH}	Propagation Delay	4.0	7.8	12.0	4.0	13.0	ns
t _{PHL}	S _i to $\overline{G}$ or $\overline{P}$	4.5	10.2	13.5	4.5	14.5	

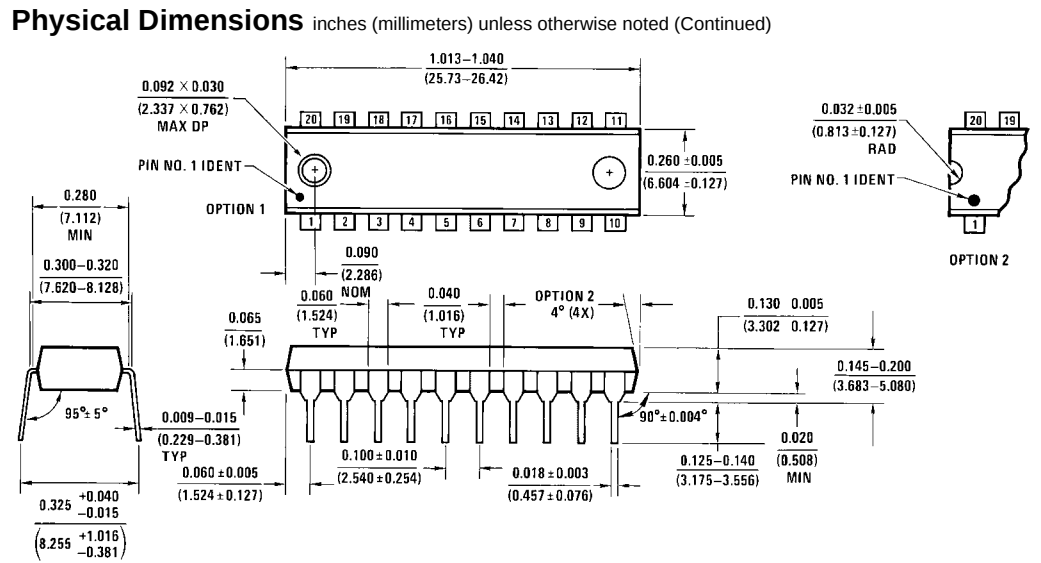
Physical Dimensions inches (millimeters) unless otherwise noted



20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide Package Number M20B



20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide Package Number M20D



**20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide
Package Number N20A**

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