



September 1983
Revised January 2005

MM74HC74A

Dual D-Type Flip-Flop with Preset and Clear

General Description

The MM74HC74A utilizes advanced silicon-gate CMOS technology to achieve operating speeds similar to the equivalent LS-TTL part. It possesses the high noise immunity and low power consumption of standard CMOS integrated circuits, along with the ability to drive 10 LS-TTL loads.

This flip-flop has independent data, preset, clear, and clock inputs and Q and $\bar{Q}$ outputs. The logic level present at the data input is transferred to the output during the positive-going transition of the clock pulse. Preset and clear are independent of the clock and accomplished by a low level at the appropriate input.

The 74HC logic family is functionally and pinout compatible with the standard 74LS logic family. All inputs are protected from damage due to static discharge by internal diode clamps to V_{CC} and ground.

Features

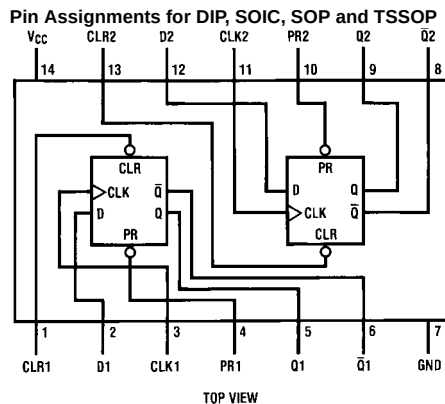
- Typical propagation delay: 20 ns
- Wide power supply range: 2–6V
- Low quiescent current: 40 μ A maximum (74HC Series)
- Low input current: 1 μ A maximum
- Fanout of 10 LS-TTL loads

Ordering Code:

Order Number	Package Number	Package Description
MM74HC74AM	M14A	14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
MM74HC74AMX_NL	M14A	Pb-Free 14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
MM74HC74ASJ	M14D	Pb-Free 14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
MM74HC74AMTC	MTC14	14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
MM74HC74AMTCX_NL	MTC14	Pb-Free 14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
MM74HC74AN	N14A	14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.
Pb-Free package per JEDEC J-STD-020B.

Connection Diagram



Truth Table

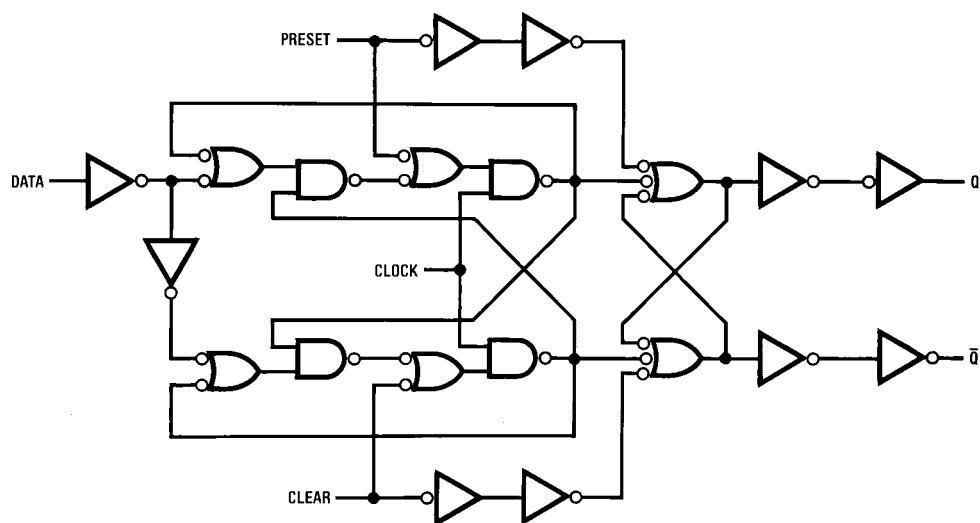
Inputs				Outputs	
PR	CLR	CLK	D	Q	$\bar{Q}$
L	H	X	X	H	L
H	L	X	X	L	H
L	L	X	X	H (Note 1)	H (Note 1)
H	H	$\uparrow$	H	H	L
H	H	$\uparrow$	L	L	H
H	H	L	X	Q0	$\bar{Q}$ 0

Note: Q0 = the level of Q before the indicated input conditions were established.

Note 1: This configuration is nonstable; that is, it will not persist when preset and clear inputs return to their inactive (HIGH) level.

MM74HC74A

Logic Diagram



MM74HC74A

AC Electrical Characteristics						
V _{CC} = 5V, T _A = 25°C, C _L = 15 pF, t _r = t _f = 6 ns						
Symbol	Parameter	Conditions	Typ	Guaranteed Limit		Units
f _{MAX}	Maximum Operating Frequency		72	30		MHz
t _{PHL} , t _{PLH}	Maximum Propagation Delay Clock to Q or $\overline{Q}$		10	30		ns
t _{PHL} , t _{PLH}	Maximum Propagation Delay Preset or Clear to Q or $\overline{Q}$		17	40		ns
t _{REM}	Minimum Removal Time, Preset or Clear to Clock		6	5		ns
t _s	Minimum Setup Time Data to Clock		10	20		ns
t _H	Minimum Hold Time Clock to Data		0	0		ns
t _W	Minimum Pulse Width Clock, Preset or Clear		8	16		ns

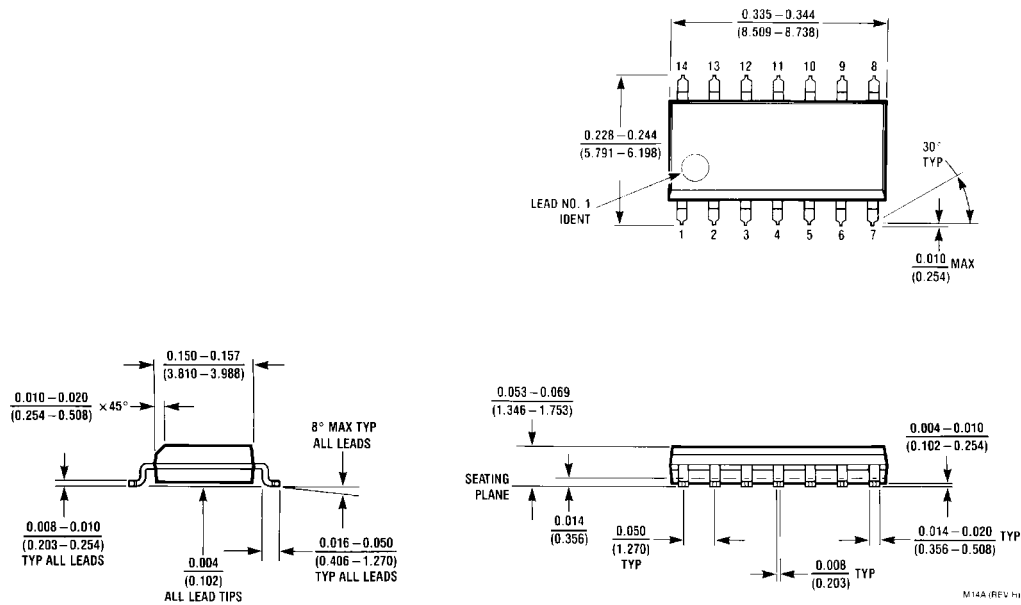
AC Electrical Characteristics

C_L = 50 pF, t_r = t_f = 6 ns (unless otherwise specified)

Symbol	Parameter	Conditions	V _{CC}	T _A = 25°C		T _A = -40 to 85°C	T _A = -55 to 125°C	Units
				Typ	Guaranteed Limits			
f _{MAX}	Maximum Operating Frequency		2.0V	22	6	5	4	MHz
			4.5V	72	30	24	20	MHz
			6.0V	94	35	28	24	MHz
t _{PHL} , t _{PLH}	Maximum Propagation Delay Clock to Q or $\overline{Q}$		2.0V	34	110	140	165	ns
			4.5V	12	22	28	33	ns
			6.0V	10	19	24	28	ns
t _{PHL} , t _{PLH}	Maximum Propagation Delay Preset or Clear To Q or $\overline{Q}$		2.0V	66	150	190	225	ns
			4.5V	20	30	38	45	ns
			6.0V	16	26	33	38	ns
t _{REM}	Minimum Removal Time Preset or Clear To Clock		2.0V	20	50	65	75	ns
			4.5V	6	10	13	15	ns
			6.0V	5	9	11	13	ns
t _s	Minimum Setup Time Data to Clock		2.0V	35	80	100	120	ns
			4.5V	10	16	20	24	ns
			6.0V	8	14	17	20	ns
t _H	Minimum Hold Time Clock to Data		2.0V		0	0	0	ns
			4.5V		0	0	0	ns
			6.0V		0	0	0	ns
t _W	Minimum, Pulse Width Clock, Preset or Clear		2.0V	30	80	101	119	ns
			4.5V	9	16	20	24	ns
			6.0V	8	14	17	20	ns
t _{TLH} , t _{THL}	Maximum Output Rise and Fall Time		2.0V	25	75	95	110	ns
			4.5V	7	15	19	22	ns
			6.0V	6	13	16	19	ns
t _r , t _f	Maximum Input Rise and Fall Time		2.0V		1000	1000	1000	ns
			4.5V		500	500	500	ns
			6.0V		400	400	400	ns
C _{PD}	Power Dissipation Capacitance (Note 6)	(per flip-flop)		80				pF
C _{IN}	Maximum Input Capacitance			5	10	10	10	pF

Note 6: C_{PD} determines the no load dynamic power consumption, P_D = C_{PD} V_{CC}² f + I_{CC} V_{CC}, and the no load dynamic current consumption, I_S = C_{PD} V_{CC} f + I_{CC}.

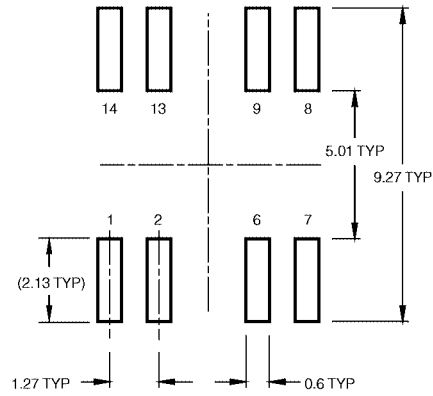
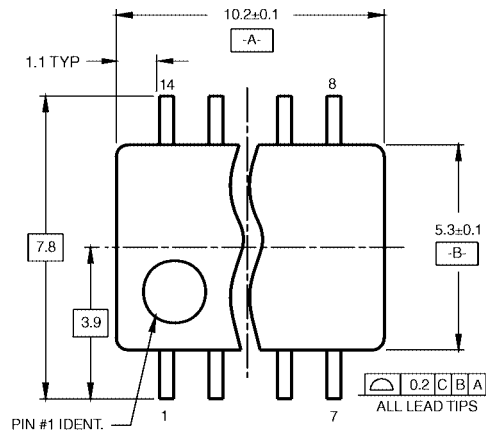
Physical Dimensions inches (millimeters) unless otherwise noted



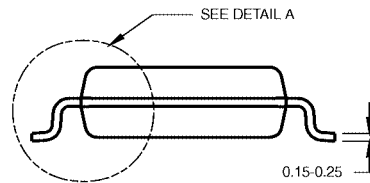
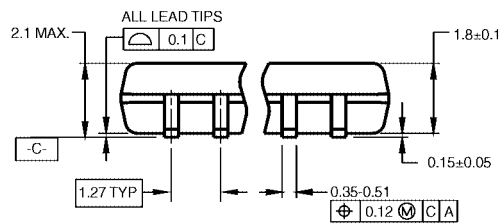
**14-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-012, 0.150" Narrow
Package Number M14A**

MM74HC74A

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

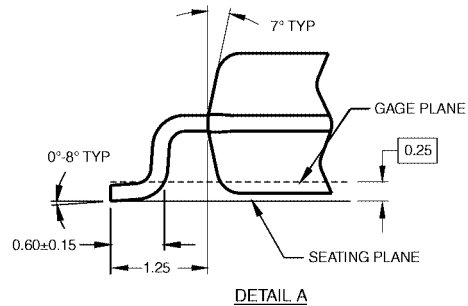


LAND PATTERN RECOMMENDATION



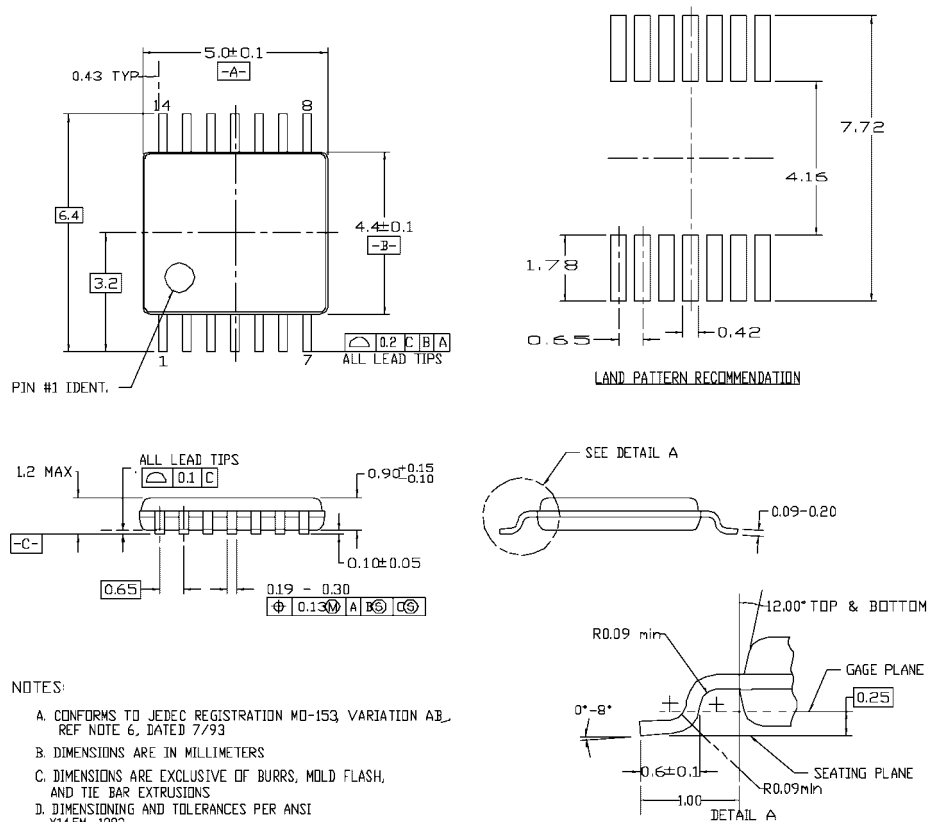
- NOTES:
A. CONFORMS TO EIAJ EDR-7320 REGISTRATION, ESTABLISHED IN DECEMBER, 1998.
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.

M14DRevB1



Pb-Free 14-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M14D

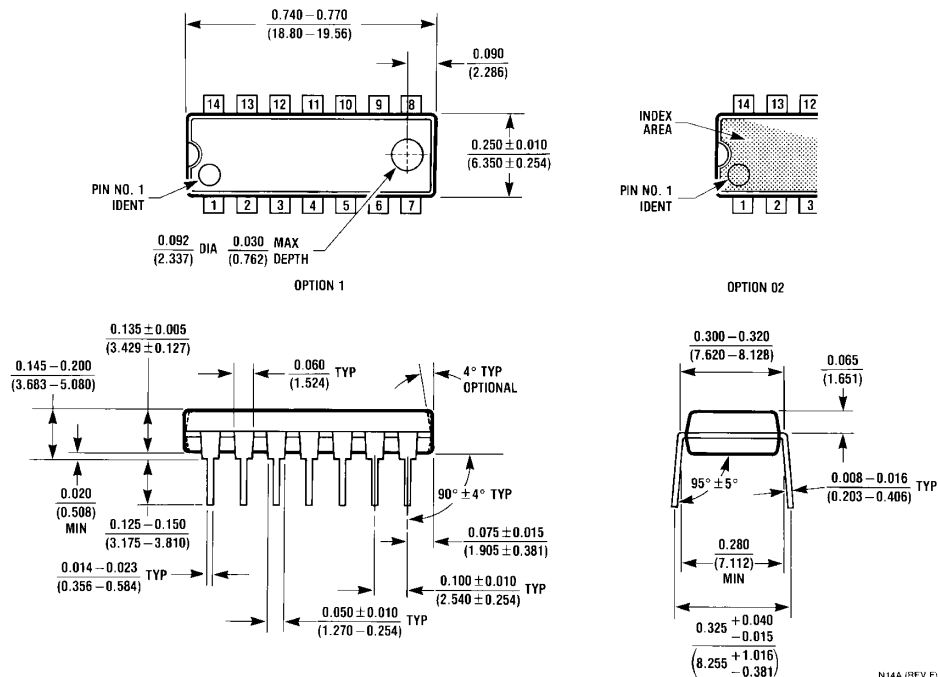
Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



MTC14revD

**14-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
Package Number MTC14**

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)



**14-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide
Package Number N14A**

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