



June 1999
Revised November 2000

74LVT162240 • 74LVTH162240

Low Voltage 16-Bit Inverting Buffer/Line Driver with 3-STATE Outputs and 25Ω Series Resistors in the Outputs

General Description

The LVT162240 and LVTH162240 contain sixteen inverting buffers with 3-STATE outputs designed to be employed as a memory and address driver, clock driver, or bus oriented transmitter/receiver. The device is nibble controlled. Individual 3-STATE control inputs can be shorted together for 8-bit or 16-bit operation.

The LVT162240 and LVTH162240 are designed with equivalent 25Ω series resistance in both the HIGH and LOW states of the output. This design reduces line noise in applications such as memory address drivers, clock drivers, and bus transceivers/transmitters.

The LVTH162240 data inputs include bushold, eliminating the need for external pull-up resistors to hold unused inputs.

These inverting buffers and line drivers are designed for low-voltage (3.3V) V_{CC} applications, but with the capability to provide a TTL interface to a 5V environment. The LVT162240 and LVTH162240 are fabricated with an advanced BiCMOS technology to achieve high speed operation similar to 5V ABT while maintaining a low power dissipation.

Features

- Input and output interface capability to systems at 5V V_{CC}
- Outputs include equivalent series resistance of 25Ω to make external termination resistors unnecessary and reduce overshoot and undershoot
- Bushold data inputs eliminate the need for external pull-up resistors to hold unused inputs (74LVTH162240), also available without bushold feature (74LVT162240).
- Live insertion/extraction permitted
- Power Up/Down high impedance provides glitch-free bus loading
- Functionally compatible with the 74 series 162240
- Latch-up performance exceeds 500 mA
- ESD performance:
 - Human-body model > 2000V
 - Machine model > 200V
 - Charged-device model > 1000V

Ordering Code:

Order Number	Package Number	Package Description
74LVT162240MEA (Note 1)	MS48A	48-Lead Small Shrink Outline Package (SSOP), JEDEC MO-118, 0.300 Wide
74LVT162240MTD (Note 1)	MTD48	48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide
74LVTH162240MEA	MS48A	48-Lead Small Shrink Outline Package (SSOP), JEDEC MO-118, 0.300 Wide [TUBE]
74LVTH162240MEX (Note 2)	MS48A	48-Lead Small Shrink Outline Package (SSOP), JEDEC MO-118, 0.300 Wide [TAPE and REEL]
74LVTH162240MTD	MTD48	48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide [TUBE]
74LVTH162240MTX (Note 2)	MTD48	48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide [TAPE and REEL]

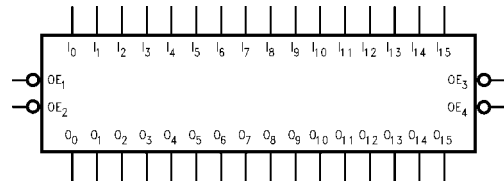
Note 1: Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

Note 2: Use this Order Number to receive devices in Tape and Reel.

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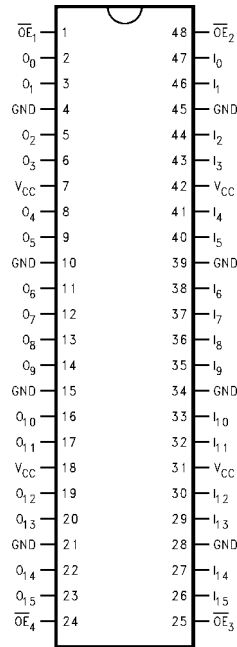
Logic Symbol



Pin Descriptions

Pin Names	Description
\overline{OE}_n	Output Enable Inputs (Active LOW)
I_0-I_{15}	Inputs
$\overline{O}_0-\overline{O}_{15}$	3-STATE Outputs

Connection Diagram



Truth Table

Inputs		Outputs
\overline{OE}_1	I_0-I_3	$\overline{O}_0-\overline{O}_3$
L	L	H
L	H	L
H	X	Z
Inputs		Outputs
\overline{OE}_2	I_4-I_7	$\overline{O}_4-\overline{O}_7$
L	L	H
L	H	L
H	X	Z
Inputs		Outputs
\overline{OE}_3	I_8-I_{11}	$\overline{O}_8-\overline{O}_{11}$
L	L	H
L	H	L
H	X	Z
Inputs		Outputs
\overline{OE}_4	$I_{12}-I_{15}$	$\overline{O}_{12}-\overline{O}_{15}$
L	L	H
L	H	L
H	X	Z

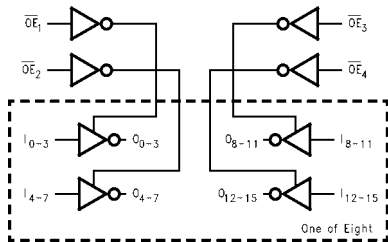
H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Immaterial
 Z = High Impedance

Functional Description

The LVT162240 and LVTH162240 contain sixteen inverting buffers with 3-STATE standard outputs. The device is nibble (4 bits) controlled with each nibble functioning identically, but independent of the other. The control pins may be shorted together to obtain full 16-bit operation. The

3-STATE outputs are controlled by an Output Enable (\overline{OE}_n) input for each nibble. When \overline{OE}_n is LOW, the outputs are in 2-state mode. When \overline{OE}_n is HIGH, the outputs are in the high impedance mode, but this does not interfere with entering new data into the inputs.

Logic Diagram



Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

Absolute Maximum Ratings (Note 3)					
Symbol	Parameter	Value	Conditions		Units
V _{CC}	Supply Voltage	-0.5 to +4.6			V
V _I	DC Input Voltage	-0.5 to +7.0			V
V _O	Output Voltage	-0.5 to +7.0	Output in 3-STATE		V
		-0.5 to +7.0	Output in HIGH or LOW State (Note 4)		
I _{IK}	DC Input Diode Current	-50	V _I < GND		mA
I _{OK}	DC Output Diode Current	-50	V _O < GND		mA
I _O	DC Output Current	64	V _O > V _{CC} Output at HIGH State		mA
		128	V _O > V _{CC} Output at LOW State		
I _{CC}	DC Supply Current per Supply Pin	±64			mA
I _{GND}	DC Ground Current per Ground Pin	±128			mA
T _{STG}	Storage Temperature	-65 to +150			°C

Recommended Operating Conditions					
Symbol	Parameter	Min	Max	Units	
V _{CC}	Supply Voltage	2.7	3.6	V	
V _I	Input Voltage	0	5.5	V	
I _{OH}	HIGH-Level Output Current		-12	mA	
I _{OL}	LOW-Level Output Current		12	mA	
T _A	Free Air Operating Temperature	-40	+85	°C	
Δt/ΔV	Input Edge Rate, V _{IN} = 0.8V–2.0V, V _{CC} = 3.0V	0	10	ns/V	

Note 3: Absolute Maximum continuous ratings are those values beyond which damage to the device may occur. Exposure to these conditions or conditions beyond those indicated may adversely affect device reliability. Functional operation under absolute maximum rated conditions is not implied.

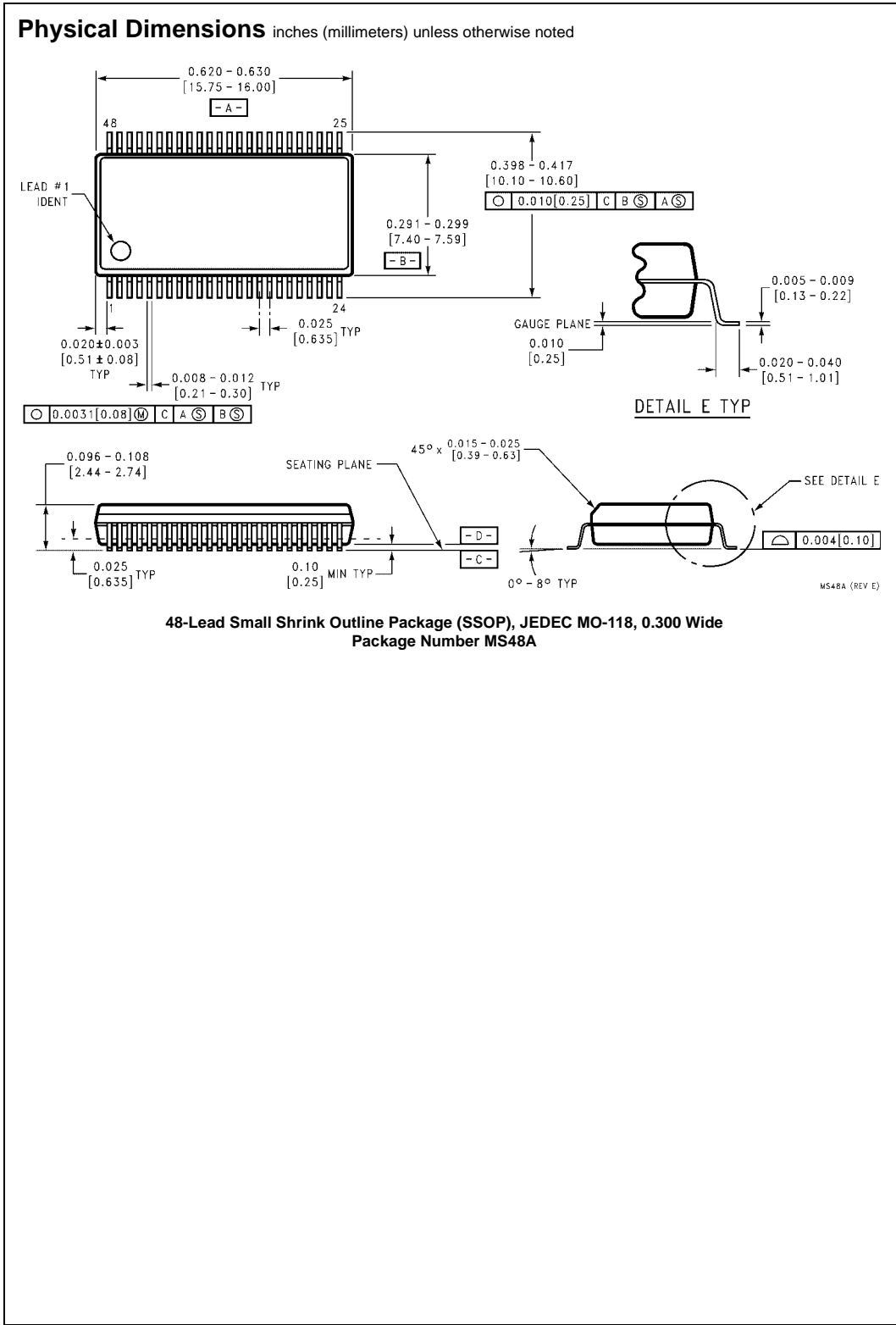
Note 4: I_O Absolute Maximum Rating must be observed.

DC Electrical Characteristics

Symbol	Parameter	V _{CC} (V)	T _A = -40°C to +85°C			Units	Conditions
			Min	Typ (Note 5)	Max		
V _{IK}	Input Clamp Diode Voltage	2.7			-1.2	V	I _I = -18 mA
V _{IH}	Input HIGH Voltage	2.7–3.6	2.0			V	V _O ≤ 0.1V or V _O ≥ V _{CC} - 0.1V
V _{IL}	Input LOW Voltage	2.7–3.6			0.8	V	
V _{OH}	Output HIGH Voltage	2.7–3.6	V _{CC} -0.2			V	I _{OH} = -100 μA
		3.0	2.0			V	I _{OH} = -12 mA
V _{OL}	Output LOW Voltage	2.7			0.2	V	I _{OL} = 100 μA
		3.0			0.8	V	I _{OL} = 12 mA
I _{I(HOLD)} (Note 6)	Bushold Input Minimum Drive	3.0	75			μA	V _I = 0.8V
			-75			μA	V _I = 2.0V
I _{I(OD)} (Note 6)	Bushold Input Over-Drive Current to Change State	3.0	500			μA	(Note 7)
			-500			μA	(Note 8)
I _I	Input Current	3.6			10	μA	V _I = 5.5V
		Control Pins	3.6		±1		V _I = 0V or V _{CC}
		Data Pins	3.6		-5		V _I = 0V
					1	V _I = V _{CC}	
I _{OFF}	Power Off Leakage Current	0			±100	μA	0V ≤ V _I or V _O ≤ 5.5V
I _{PU/PD}	Power Up/Down 3-STATE Current	0–1.5V			±100	μA	V _O = 0.5V to 3.0V V _I = GND or V _{CC}
I _{OZL}	3-STATE Output Leakage Current	3.6			-5	μA	V _O = 0.5V
I _{OZH}	3-STATE Output Leakage Current	3.6			5	μA	V _O = 3.0V
I _{OZH+}	3-STATE Output Leakage Current	3.6			10	μA	V _{CC} < V _O ≤ 5.5V
I _{CCH}	Power Supply Current	3.6			0.19	mA	Outputs HIGH
I _{CCL}	Power Supply Current	3.6			5	mA	Outputs LOW
I _{CCZ}	Power Supply Current	3.6			0.19	mA	Outputs Disabled

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DC Electrical Characteristics (Continued)							
Symbol	Parameter	V _{CC} (V)	T _A = -40°C to +85°C			Units	Conditions
			Min	Typ (Note 5)	Max		
t _{CCZ+}	Power Supply Current	3.6			0.19	mA	V _{CC} ≤ V _O ≤ 5.5V, Outputs Disabled
ΔI _{CC}	Increase in Power Supply Current (Note 9)	3.6			0.2	mA	One Input at V _{CC} - 0.6V Other Inputs at V _{CC} or GND
<p>Note 5: All typical values are at V_{CC} = 3.3V, T_A = 25°C.</p> <p>Note 6: Applies to bushold versions only (74LVTH162240).</p> <p>Note 7: An external driver must source at least the specified current to switch from LOW-to-HIGH.</p> <p>Note 8: An external driver must sink at least the specified current to switch from HIGH-to-LOW.</p> <p>Note 9: This is the increase in supply current for each input that is at the specified voltage level rather than V_{CC} or GND.</p>							
Dynamic Switching Characteristics (Note 10)							
Symbol	Parameter	V _{CC} (V)	T _A = 25°C			Units	Conditions C _L = 50 pF, R _L = 500Ω
			Min	Typ	Max		
V _{OLP}	Quiet Output Maximum Dynamic V _{OL}	3.3		0.8		V	(Note 11)
V _{OLV}	Quiet Output Minimum Dynamic V _{OL}	3.3		-0.8		V	(Note 11)
<p>Note 10: Characterized in SSOP package. Guaranteed parameter, but not tested.</p> <p>Note 11: Max number of outputs defined as (n). n-1 data inputs are driven 0V to 3V. Output under test held LOW.</p>							
AC Electrical Characteristics							
Symbol	Parameter	T _A = -40°C to +85°C, C _L = 50 pF, R _L = 500Ω					Units
		V _{CC} = 3.3V ± 0.3V			V _{CC} = 2.7V		
		Min	Typ (Note 12)	Max	Min	Max	
t _{PLH}	Propagation Delay Data to Output	1.0		4.0	1.0	4.8	ns
t _{PHL}		1.0		4.0	1.0	4.6	
t _{PZH}	Output Enable Time	1.0		4.8	1.0	5.7	ns
t _{PZL}		1.0		4.9	1.0	6.1	
t _{PHZ}	Output Disable Time	2.0		4.9	2.0	5.4	ns
t _{PLZ}		2.0		4.5	2.0	4.5	
t _{OSHL}	Output to Output Skew (Note 13)			1.0		1.0	ns
t _{OSLH}							
<p>Note 12: All typical values are at V_{CC} = 3.3V, T_A = 25°C.</p> <p>Note 13: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t_{OSHL}) or LOW-to-HIGH (t_{OSLH}).</p>							
Capacitance (Note 14)							
Symbol	Parameter	Conditions			Typical	Units	
C _{IN}	Input Capacitance	V _{CC} = 0V, V _I = 0V or V _{CC}			4	pF	
C _{OUT}	Output Capacitance	V _{CC} = 3.0V, V _O = 0V or V _{CC}			8	pF	
<p>Note 14: Capacitance is measured at frequency f = 1 MHz, per MIL-STD-883, Method 3012.</p>							



Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

PIN #1 IDENT.

ALL LEAD TIPS

LAND PATTERN RECOMMENDATION

SEE DETAIL A

12.00° TOP & BOTTOM

R0.16

R0.31

GAGE PLANE

1.25

0°-8°

0.60±0.10

1.00

SEATING PLANE

DIMENSIONS ARE IN MILLIMETERS

NOTES:

- CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AB, REF NOTE 6, DATE 7/93.
- DIMENSIONS ARE IN MILLIMETERS.
- DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
- DIMENSIONS AND TOLERANCES PER ANS Y14.5M, 1982.

MTD48RevB1

**48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide
Package Number MTD48**

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- A critical component in any component of a life support device or system whose failure to perform can be reasonably expected to cause the failure of the life support device or system, or to affect its safety or effectiveness.

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