19-3482; Rev 0; 10/04

EVALUATION KIT AVAILABLE

HD/SD Switchable Video Filters and Buffers

General Description

The MAX7454/MAX7455 triple-channel video reconstruction filters and buffers are ideal for high definition (HD), standard definition progressive scan/noninterlaced (SDp), and standard definition interlaced (SDi) television applications. These devices are a fully integrated solution for filtering and buffering HD and/or SDp/SDi TV signals in component video output format (Y P_B P_R or RGB). The MAX7454/MAX7455 are compatible with the 1080i, 720p, 480p, and 480i scanning system standards. In addition to having an HD/SD switchable frequency response, the magnitude response can be optimized by approximately 15% by a control input.

The input and output signals are DC-coupled to the MAX7454/MAX7455, eliminating the large output AC-coupling capacitors normally used. The MAX7454/MAX7455 output buffers drive a $2V_{P-P}$ video signal into a standard 150Ω load. The MAX7454 has a gain of +6dB and the MAX7455 has a gain of +12dB. Both devices are available in a 20-pin TSSOP package and are fully specified over the upper commercial (0°C to +85°C) temperature range.

Applications

Set-Top Boxes

Direct-Broadcast Satellite (DBS) Receiver

DVD Players

Hard-Disk Recorders

HDTV (LCD, PDP, DLP)

Professional Cameras

Pin Configuration appears at end of data sheet.

Features

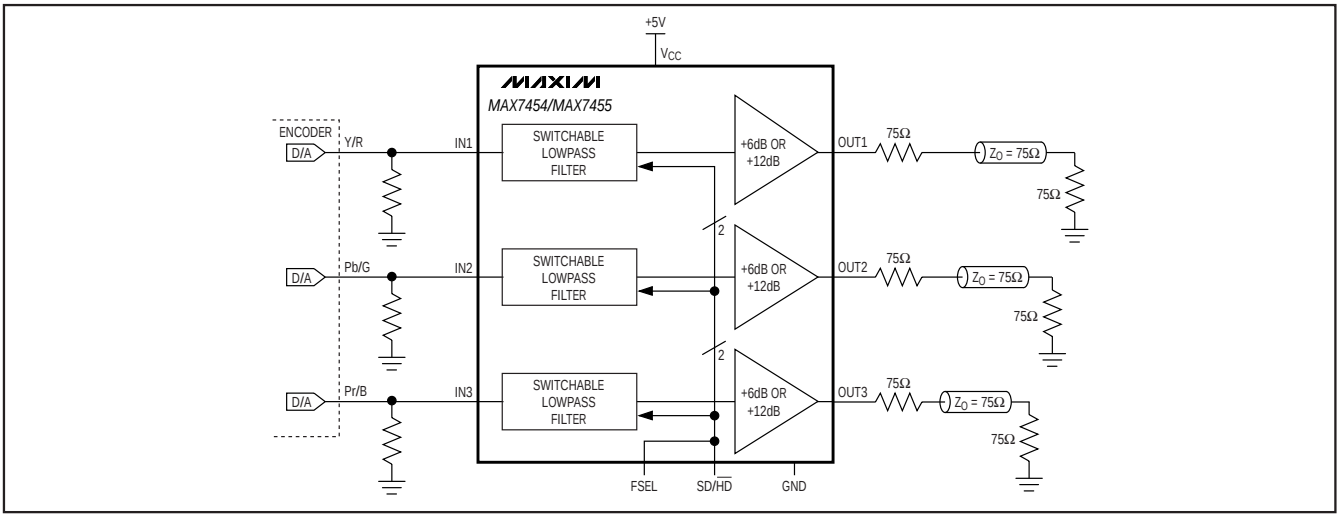
- **30MHz High Definition (HD)/10MHz Standard Definition (SD) Switchable Video Reconstruction Filter**
- **15% Magnitude Response Adjustment**
- **Passband: -2.3dB at 30MHz**
  -0.40dB at 10MHz
  -0.10dB at 5MHz
- **Stopband: -55dB at 74MHz (HDTV)**
  -62dB at 27MHz (SDTV)
- **Output Blank Level <1V for DC-Coupled Output**
- **+6dB Gain (MAX7454) or +12dB Gain (MAX7455)**
- **Direct Coupled Input, Zero Tilt**
- **Direct Coupled Output, No Large Output Capacitor**
- **Drives $2V_{P-P}$ Signal in 150Ω Video Load**
- **Small 20-Pin TSSOP Package**
- **Single +5V Supply**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	BUFFER GAIN (dB)
MAX7454UUP	0°C to +85°C	20 TSSOP-EP**	+6
MAX7454UUP+*	0°C to +85°C	20 TSSOP-EP**	+6
MAX7455UUP*	0°C to +85°C	20 TSSOP-EP**	+12
MAX7455UUP+*	0°C to +85°C	20 TSSOP-EP**	+12

+Indicates lead-free packaging.
**Future product—contact factory for availability.*
***EP = Exposed pad.*

Typical Operating Circuit



ABSOLUTE MAXIMUM RATINGS

V_{CC} to GND .....-0.3V to +6V
IN1, IN2, IN3 to GND.....-0.3V to (V_{CC} + 0.3V)
OUT1, OUT2, OUT3 to GND .....-0.3V to (V_{CC} + 0.3V)
SD/$\overline{HD}$, FSEL to GND .....-0.3V to (V_{CC} + 0.3V)
Continuous Power Dissipation (T_A = +70°C)
20-Pin TSSOP (derate 21.7mW/°C above +70°C) 1739.1mW
Maximum Current into IN1, IN2, IN3, SD/$\overline{HD}$, FSEL .....±50mA
Operating Temperature Range
MAX745_UUP .....0°C to +85°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C
Junction Temperature .....+150°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{CC} = +5V ±5%, R_{LOAD} = 150Ω to GND, C_{LOAD} = 0 to 20pF to GND, SD/$\overline{HD}$ = GND, FSEL = V_{CC}, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{CC} = +5V and T_A = +25°C.)

PARAMETERS	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
HD-Filter Passband Response	A_{PB}	f = 100kHz to 26MHz, FSEL = GND	-3.5	-2.5		dB
		f = 100kHz to 26MHz, FSEL = V_{CC}	-2.6	-1.7		
		f = 100kHz to 30MHz, FSEL = V_{CC}	-3.6	-2.3		
HD-Filter Stopband Attenuation	A_{SB}	f = 74MHz, FSEL = GND	45	55		dB
SD-Filter Passband Response		f = 10MHz, SD/$\overline{HD}$ = V_{CC}, FSEL = V_{CC}	-0.65	-0.40		dB
SD-Filter Stopband Attenuation		f = 27MHz, SD/$\overline{HD}$ = V_{CC}, FSEL = GND	50	62		dB
HD Group Delay Deviation	Δt_G	100kHz to 26MHz, relative to 100kHz; FSEL = V_{CC}		5		ns
HD Group Delay Matching	$t_{G(MATCH)}$	Channel to channel, 100kHz to 2MHz; FSEL = V_{CC}		0.1		ns
SD Group Delay Deviation	Δt_G	100kHz to 5.75MHz, relative to 100kHz; SD/$\overline{HD}$ = V_{CC}, FSEL = V_{CC}		2		ns
		100kHz to 10MHz, relative to 100kHz; SD/$\overline{HD}$ = V_{CC}, FSEL = V_{CC}		12		
SD Group Delay Matching	$t_{G(MATCH)}$	Channel to channel, 100kHz to 500kHz; FSEL = V_{CC}		2		ns
Total Harmonic Distortion	THD	Gain = +2V/V, V_{OUT} = $2V_{P-P}$ video signal 100kHz to 26MHz		-45		dB
Differential Gain	dG	5-step modulated staircase (Note 1)		0.3		%
Differential Phase	dθ	5-step modulated staircase (Note 1)		0.2		Degrees
Signal-to-Noise Ratio	SNR	Output signal ($2V_{P-P}$) to RMS noise (100kHz to 30MHz)	62	67		dB
Line Time Distortion	H_{DIST}	Deviations in a line with an 18µs, 100 IRE bar (Note 2)		±1	±3	mV
Input Voltage Range		MAX7454, THD > -30dB, f_{IN} = 4.43MHz	0		1.2	V
		MAX7455, THD > -30dB, f_{IN} = 4.43MHz	0		0.6	
Total Output DC Variation		MAX7454, V_{IN} = 0.3V, FSEL = GND; SD/$\overline{HD}$ = V_{CC}	-0.25		+0.25	mV
		MAX7454, V_{IN} = 0.3V, FSEL = GND; SD/$\overline{HD}$ = GND	-0.25		+0.25	
Field Time Distortion	V_{DIST}	130 lines, 18µs, 100 IRE bars		±1	±10	mV

ELECTRICAL CHARACTERISTICS (continued)

(V_{CC} = +5V ±5%, R_{LOAD} = 150Ω to GND, C_{LOAD} = 0 to 20pF to GND, SD/$\overline{HD}$ = GND, FSEL = V_{CC}, T_A = T_{MIN} to T_{MAX}, unless otherwise noted. Typical values are at V_{CC} = +5V and T_A = +25°C.)

PARAMETERS	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Input Leakage Current	I_{IN}			±10		nA
Input Capacitance	C_{IN}			5		pF
Low-Frequency Gain Accuracy		f_{IN} = 100kHz	-2.5		+2.5	%
Low-Frequency Gain Matching		f_{IN} = 100kHz, maximum difference between any two input channels		0	1.2	%
Dynamic Output Swing		THD > -30dB	2.4			V_{P-P}
Channel-to-Channel Isolation		DC to 1MHz		70		dB
Power-Supply Rejection Ratio	PSRR	V_{IN} = 100mV_{P-P} at 5MHz		35		dB
		V_{IN} =10mV_{P-P} at 26MHz		25		
Supply Voltage Range	V_{CC}		4.75	5	5.25	V
Supply Current	I_{CC}	No load		220	235	mA
LOGIC INPUTS (SD/$\overline{HD}$, FSEL)						
Input High Voltage	V_{IH}		2.4			V
Input Low Voltage	V_{IL}				0.8	V
Input Current		Digital inputs = V_{CC} or 0V			±10	µA

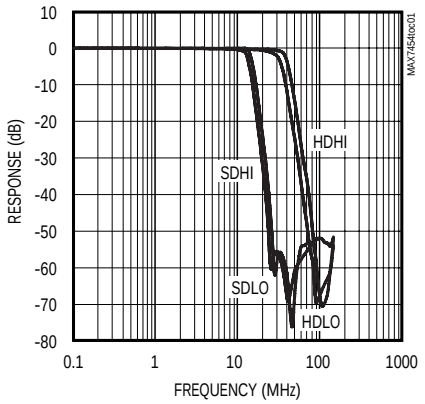
Note 1: The differential gain and differential phase specifications apply to standard-definition composite video signals only.

Note 2: This applies for an anti-aliasing filtering application using a 0.1µF input capacitor. This does not apply for a video reconstruction application, since there is no input-coupling capacitor.

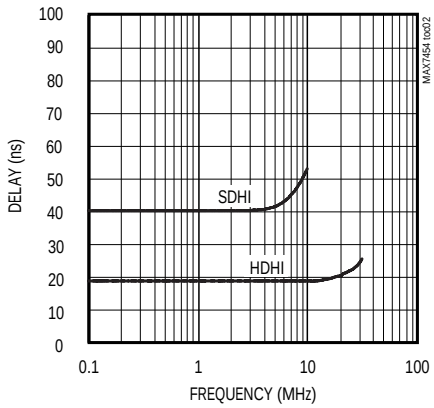
Typical Operating Characteristics

(R_{LOAD} = 150Ω to GND, V_{CC} = +5V, and T_A = +25°C.)

MAGNITUDE RESPONSE (PASSBAND PLUS STOPBAND)



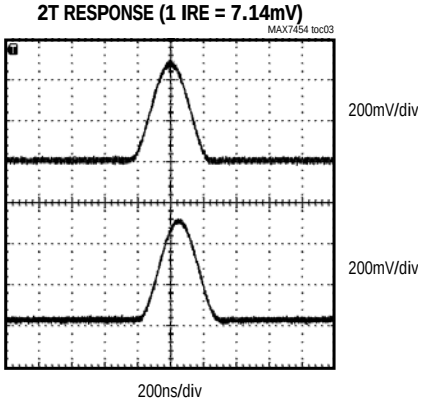
GROUP DELAY



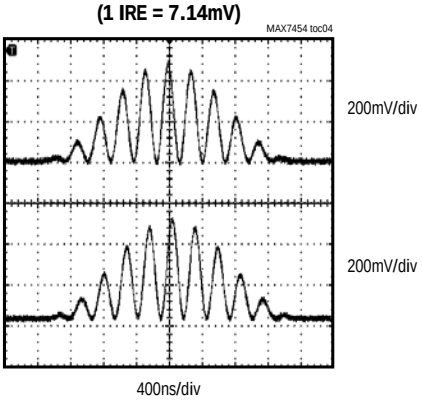
Typical Operating Characteristics (continued)

(R_{LOAD} = 150Ω to GND, V_{CC} = +5V, and T_A = +25°C.)

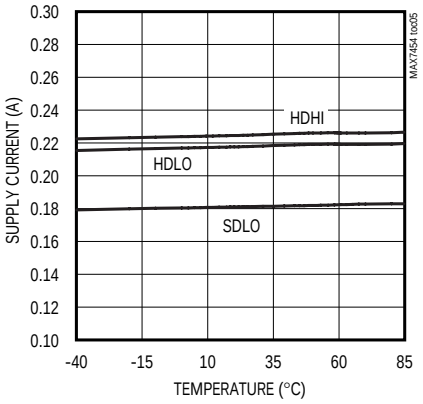
2T RESPONSE (1 IRE = 7.14mV)



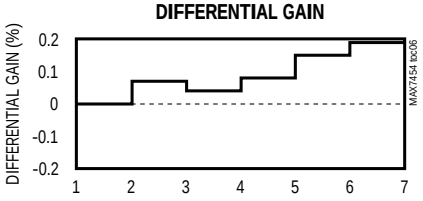
MODULATED 12.5T RESPONSE (1 IRE = 7.14mV)



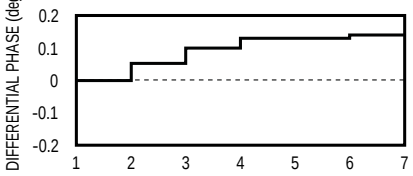
SUPPLY CURRENT vs. TEMPERATURE



DIFFERENTIAL GAIN



DIFFERENTIAL PHASE



Pin Description

PIN	NAME	FUNCTION
1, 3, 5, 7, 11, 12, 15, 18	GND	Ground
2	IN1	Video Input 1
4	IN2	Video Input 2
6	IN3	Video Input 3
8	SD/$\overline{HD}$	SD/HD Select. Selects between HD or SD magnitude response. Connect to GND to choose HD bandwidth response.
9	FSEL	Frequency Select. Selects either a low or high setting for both HD and SD frequency response (see the *Frequency Adjusting* section).
10, 13, 16, 19	V_{CC}	+5V Power Supply. Bypass to GND with a 0.1µF capacitor. See the *Power-Supply Bypassing and Layout Considerations* section.
14	OUT3	Video Output 3
17	OUT2	Video Output 2
20	OUT1	Video Output 1
—	EP	Exposed Pad. The exposed pad is internally connected to ground.

Detailed Description

The MAX7454/MAX7455 are ideal for use in consumer electronic products such as HD-compatible cable-TV set-top boxes or DBS receiver decoders, which process video signals in component output format. The MAX7454/MAX7455 support both the 1080i and the 720p scanning formats for HDTV as well as the 480i and 480p formats for SDi and SDp TV. The reconstruction filters take three signals out of a video digital-to-analog converter (DAC) or an encoder and smooth the signals with appropriate filtering. FSEL and SD/$\overline{HD}$ select the filter frequency response for SDp, SDi, and HDTV (see Table 1). The outputs are connected directly to standard 150Ω video loads.

The *Typical Operating Circuit* illustrates the internal structure of the MAX7454/MAX7455. The lowpass filter attenuates the high-frequency contents of the input, and the output amplifier drives a standard video load.

Filter

Filter response

The video filter features an elliptic-type response with a steep transition band response to achieve a wider passband response along with an excellent stopband response. In addition, the filter has been optimized to give a good time domain response with low overshoot. The stopband offers 62dB (typ) of attenuation at sampling frequencies of 27MHz and above for SDTV and 55dB (typ) of stopband attenuation for frequencies of 74MHz and above for HDTV (see the *Typical Operating Characteristics*).

Table 1. Frequency Selection Control

MODE	SD/$\overline{HD}$	FSEL
HD Low	GND	GND
HD High	GND	V_{CC}
SD Low	V_{CC}	GND
SD High	V_{CC}	V_{CC}

Frequency Adjusting

SD/$\overline{HD}$ selects the HD or SD mode. In HD or SD mode, FSEL allows optimization of the passband or stopband performance by adjusting the cutoff frequency. If passband performance is the priority, set FSEL high for the maximum passband performance with a small compromise in stopband attenuation. If stopband performance is more important, set FSEL low for the maximum stopband attenuation with a small compromise in passband.

Due to the steep transition band response, the MAX7454/MAX7455 can be used in both progressive scan and interlaced video signals. The stopband attenuation at 27MHz or higher is >62dB.

Output Buffer

The output buffer on the MAX7454/MAX7455 drives a $2V_{P-P}$ signal into a 150Ω video load. It is intended to be DC-coupled per the digital TV standard. No output AC-

coupling capacitors are required when driving a cable, thereby eliminating the normal adverse effects caused by these large capacitors. The output DC level is controlled to limit the DC voltage on the cable so the blanking level of the video signal is always less than 1V, meeting the digital TV specification. See the *Output DC Level* section for more information.

The output of the MAX7454/MAX7455 can also be AC-coupled when driving a high-impedance load. In anti-aliasing applications, when the optimum bias point for the converter needs to be established, the MAX7454/MAX7455 can drive a high impedance (typ >1kΩ) through an AC-coupling capacitor.

Gain Options

The MAX7454 features an overall gain of +6dB, while the MAX7455 features an overall gain of +12dB.

Output DC Level

The MAX7454/MAX7455 are DC-coupled circuits. The nominal DC or nominal instantaneous AC voltage on the outputs of the MAX7454/MAX7455 can be determined by the following equations:

$$V_{OUT} = 2 \times V_{IN} + 0.8V \text{ (MAX7454)}$$

$$V_{OUT} = 4 \times V_{IN} + 0.8V \text{ (MAX7455)}$$

For example, in the MAX7454, 0V on the input results in an output nominal voltage of 0.8V, and a 0.3V input (typical blanking level) results in an output nominal level of 1.4V.

Applications Information

Input Considerations

The inputs on the MAX7454/MAX7455 are normally DC-coupled. Thus, no AC-coupling capacitors are required. The input voltage range includes ground and typically extends up to 1.2V. If the input is from a typical single supply current output DAC or encoder it can be connected directly to the MAX7454/MAX7455. The board trace should be kept as short as possible to minimize the parasitic stray capacitance. The MAX7454/MAX7455 contribute 5pF of capacitance. For example, a total capacitance on the input of approximately 20pF causes a 100MHz pole if the DAC termination resistor is 75Ω. A pole at 100MHz introduces an additional 0.5dB passband attenuation at 30MHz.

The input to the MAX7454/MAX7455 can be AC-coupled. In this case, it is important to set the DC bias properly to ensure that the negative peak of the video signal is as near to zero volts as possible. The bias can be fixed or a video clamp can be used. A video clamp is preferable because it limits the total swing of the signal by holding the blanking level of the signal constant.

Output Considerations

The outputs of the MAX7454/MAX7455 are normally DC-coupled. No AC-coupling capacitors are required. The MAX7454/MAX7455 connect directly to the video cable with a 75Ω series termination resistor. The other end of the cable should also be properly terminated with a 75Ω resistor. Because of the inherent divide-by-two of this configuration the peak-to-peak amplitude as well as the DC level of the signal are divided by two. The biasing on the output of the MAX7454/MAX7455 is such that the blanking level of the video signal on the cable is always less than 1V, which complies with digital TV requirements.

Anti-Aliasing Filter

The MAX7454/MAX7455 can be used as an anti-aliasing filter to eliminate out-of-band noise in an analog-to-digital video-sampling system. The output of the MAX7454/MAX7455 can be DC- or AC-coupled. This decision depends on the input range of the analog-to-digital converter and the required accuracy of the resulting digital blanking level. The output blanking level of the MAX7454/MAX7455 is 1.4V with the negative peak of the signal at 0.8V and the positive peak white at 2.8V. This assumes a $1V_{P-P}$ input signal with the negative peak at 0V. See the *Electrical Characteristics* table for the specified variations of these values. If the DC and peak levels are not compatible with the data-converter input, the outputs of the MAX7454/MAX7455 need to be AC-coupled. Choose an AC-coupling capacitor value that ensures that the lowest frequency content in the video signal is passed and the line time distortion is kept within desired limits. The resulting capacitor value is dependent on the input impedance of the converter circuit. Use a video clamp to re-establish the DC level.

Power-Supply Bypassing and Layout Considerations

The MAX7454/MAX7455 operate from a single +5V supply. Bypass each V_{CC} to GND with a 0.1µF capacitor and an additional 1µF capacitor in parallel if any significant low-frequency disturbances are present in the vicinity of the MAX7454/MAX7455. Use an extensive ground plane to ensure optimum performance. The three V_{CC} pins (pins 13, 16, and 19) that supply the individual channels can be connected together and bypassed as one, provided the components are close to the pins. Bypass the remaining V_{CC} pin (pin 10) separately with the same 0.1µF and 1µF capacitor combination.

Place the input and output termination resistors as close to the device as possible. Alternatively, the terminations may be placed further from the device if the PC board

traces are designed to be a controlled impedance of 75Ω. Regardless, the parasitic capacitance should be kept as low as possible to avoid performance degradation in the frequency response at 30MHz.

Refer to the MAX7454/MAX7455 evaluation kit for a proven PC board layout.

Exposed Pad and Heat Dissipation

The TSSOP package of the MAX7454/MAX7455 has an exposed pad on its bottom. This pad is electrically connected to GND. Do not route signals under the package.

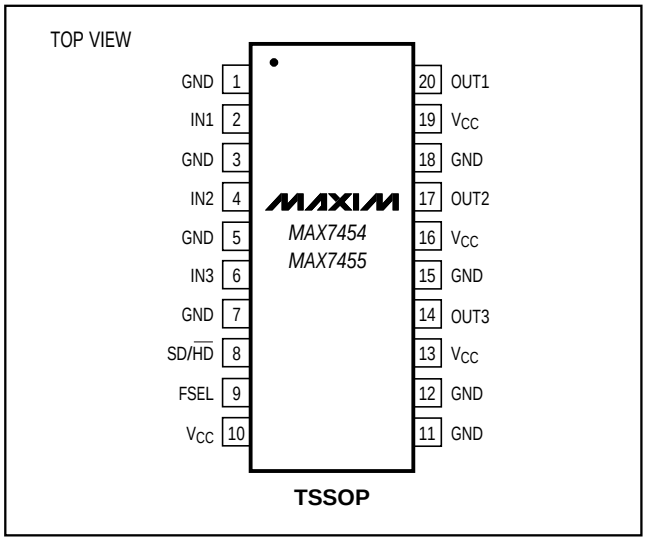
Heat dispersion is a very important issue for the MAX7454/MAX7455. The design of the PC board area associated with and in the vicinity of the device is important in achieving an adequate thermal resistance to keep the temperature of the MAX7454/MAX7455 within the specified limits.

The thermal resistance of the 20-pin TSSOP package is 60°C/W from die to ambient in free air. The thermal resistance from the die to the package surface (case) is 2°C/W. The net thermal resistance on a practical board is between these two numbers. The typical power dissipation of the MAX7454/MAX7455 is 1.2W. To keep the die temperature within specified limits, the maximum net thermal resistance should not exceed 30°C/W. This value is calculated assuming a worst-case ambient temperature of +85°C and the maximum die temperature.

The use of a 2-layer board with a good ground plane is recommended. Place copper directly under the MAX7454/MAX7455 package so that it matches the outline of the plastic encapsulated area. Place via holes in this area to electrically and thermally connect it to the ground plane. Use as many vias as possible for maximum heat transfer.

One tested board is a 4-layer board using FR-4 material and 1oz copper. It has equal areas of metal on the top side and bottom side that coincide with the plastic encapsulated area of the 20-pin TSSOP package. The two middle layers are power and ground planes. The board has 21 15-mil plated-through via holes between the top, bottom, and ground plane layers. This board was measured and has a total thermal resistance of 25°C/W, less than the 30°C/W goal.

Pin Configuration



Chip Information

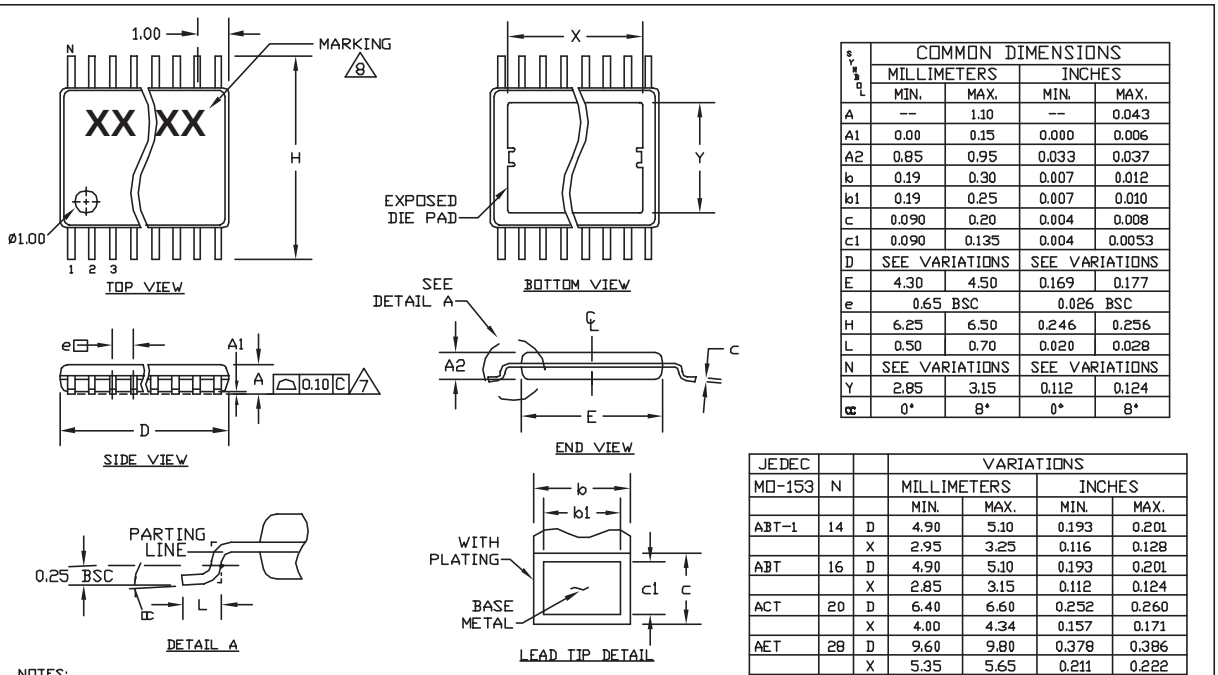
TRANSISTOR COUNT: 19191

PROCESS: BiCMOS

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)

TSSOP 4.4mm BODY.EPS



SYMBOL	COMMON DIMENSIONS			
	MILLIMETERS		INCHES	
	MIN.	MAX.	MIN.	MAX.
A	--	1.10	--	0.043
A1	0.00	0.15	0.000	0.006
A2	0.85	0.95	0.033	0.037
b	0.19	0.30	0.007	0.012
b1	0.19	0.25	0.007	0.010
c	0.090	0.20	0.004	0.008
c1	0.090	0.135	0.004	0.0053
D	SEE VARIATIONS		SEE VARIATIONS	
E	4.30	4.50	0.169	0.177
e	0.65 BSC		0.026 BSC	
H	6.25	6.50	0.246	0.256
L	0.50	0.70	0.020	0.028
N	SEE VARIATIONS		SEE VARIATIONS	
Y	2.85	3.15	0.112	0.124
α	0°	8°	0°	8°

JEDEC			VARIATIONS			
MO-153	N		MILLIMETERS		INCHES	
			MIN.	MAX.	MIN.	MAX.
ABT-1	14	D	4.90	5.10	0.193	0.201
		X	2.95	3.25	0.116	0.128
ABT	16	D	4.90	5.10	0.193	0.201
		X	2.85	3.15	0.112	0.124
ACT	20	D	6.40	6.60	0.252	0.260
		X	4.00	4.34	0.157	0.171
AET	28	D	9.60	9.80	0.378	0.386
		X	5.35	5.65	0.211	0.222

NOTES:
1. DIMENSIONS D AND E DO NOT INCLUDE FLASH.
2. MOLD FLASH OR PROTRUSIONS NOT TO EXCEED 0.15mm PER SIDE.
3. CONTROLLING DIMENSION: MILLIMETERS.
4. MEETS JEDEC OUTLINE MO-153. SEE JEDEC VARIATIONS TABLE.
5. "N" REFERS TO NUMBER OF LEADS.
6. EXPOSED PAD FLUSH WITH BOTTOM OF PACKAGE WITHIN .002".
7. THE LEAD TIPS MUST LIE WITHIN A SPECIFIED ZONE. THIS TOLERANCE ZONE IS DEFINED BY TWO PARALLEL PLANES. ONE PLANE IS THE SEATING PLANE, DATUM [-C-]; THE OTHER PLANE IS AT THE SPECIFIED DISTANCE FROM [-C-] IN THE DIRECTION INDICATED.
8. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
9. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.

-DRAWING NOT TO SCALE-

DALLAS SEMICONDUCTOR MAXIM

TITLE: PACKAGE OUTLINE, TSSOP, 4.40 MM BODY, EXPOSED PAD

APPROVAL	DOCUMENT CONTROL NO.	REV.	
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