19-1014; Rev 0; 10/07

查询"MAX8821ETI+"供应商

White LED Charge Pump with Mono Class D Audio Amp and Dual LDO

MAX8821

General Description

The MAX8821 integrates a charge pump for white LEDs, an audio loudspeaker amplifier, and two low-noise LDOs controlled by an I²C control interface. The high-efficiency, adaptive-mode inverting charge pump drives up to six LEDs with constant current for uniform brightness. The LED current is controlled by an I²C interface and adjusts from 0.1mA to 25.6mA per LED into 32 pseudo-logarithmic steps. Independent voltages for each LED maximize efficiency even with large LED forward voltage (V_F) mismatch. An internal temperature derating function reduces the current above +40°C to protect the LEDs.

The high-efficiency mono Class D audio amplifier delivers up to 2W into a 4Ω speaker from a 5V input supply. The amplifier features proprietary filterless Active Emissions Limiting (AEL) technology. AEL prevents high-frequency emissions resulting from conventional Class D free-wheeling behavior in the presence of an inductive load. The amplifier offers two modulation schemes: a fixed-frequency mode (FFM) and a spread-spectrum mode (SSM) that reduce EMI-radiated emissions due to the modulation frequency. The amplifier also has robust output protection and high power-supply rejection ratio (PSRR). Click-and-pop suppression is active during power-up/down, enable/disable, and for all mode changes. The amplifier's gain is adjustable through an I²C interface, from -3dB to +24dB in 10 3dB steps. Differential inputs improve common-mode noise rejection.

The LDOs in the MAX8821 are designed for low-noise operation. Each LDO output voltage can be individually programmed by the I²C interface. Both LDO1 and LDO2 have a high 70dB PSRR rating.

The MAX8821 includes soft-start, thermal shutdown, open-circuit, and short-circuit protections, and is available in a compact 28-pin, Thin QFN, 4mm x 4mm package (0.8mm max height).

Applications

Cell Phones and Smartphones

PDAs, Digital Cameras, Camcorders

MP3 Players, GPS Devices

Features

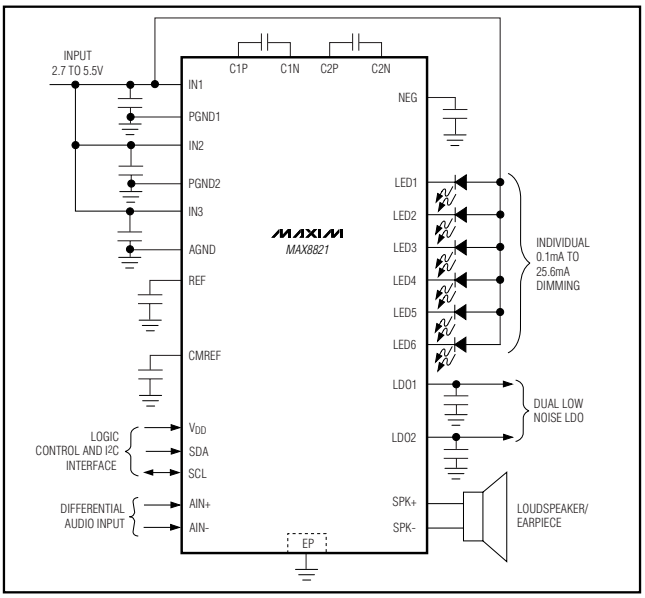
- **White LED Inverting Charge Pump**
  - **Independent Adaptive Current Regulators for Each LED**
  - **6 Low-Dropout Current Regulators**
  - **Flexible I²C Dimming Control for Each LED**
  - **Ramp-Up/Down, Current Control for Each LED**
  - **Low 70µA (typ) Quiescent Current**
  - **T_A Derating Function Protects LEDs**
- **Mono 2W Class D Loudspeaker Amplifier**
  - **85% Efficiency (R_L = 8Ω, P_{OUT} = 600mW)**
  - **Low 0.05% THD+N at 1kHz**
  - **High 65dB PSRR at 1kHz**
  - **Fully Differential Inputs**
  - **-3dB to +24dB Gain Settings in 3dB Steps**
  - **Integrated Click-and-Pop Suppression**
  - **Low Quiescent Current**
- **Dual Low-Noise LDO**
  - **45µV_{RMS} Output Noise, 70dB PSRR**
  - **Flexible I²C-Controlled Output Voltages**
  - **200mA and 300mA Output Current Drive**

Ordering Information

PART	TEMP RANGE	PIN-PACKAGE	PKG CODE
MAX8821ETI+	-40°C to +85°C	28 Thin QFN 4mm x 4mm	T2844-1

+Denotes a lead-free package.

Typical Operating Circuit



For pricing, delivery, and ordering information, please contact Maxim Direct at 1-888-629-4642, or visit Maxim's website at www.maxim-ic.com.

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ABSOLUTE MAXIMUM RATINGS

IN1, IN2, IN3, V_{DD} to AGND .....-0.3V to +6.0V
SCL, SDA to AGND .....-0.3V to (V_{DD} + 0.3V)
IN1, IN2, IN3 to NEG .....-0.3V to +6.0V
AGND to C2N .....-0.3V to +6.0V
C1P, C2P to AGND .....-0.3V to (V_{IN1} + 0.3V)
LED_, C1N, C2N to NEG.....-0.3V to (V_{IN1} + 0.3V)
LDO1, LDO2, REF to AGND .....-0.3V to (V_{IN3} + 0.3V)
CMREF, AIN+, AIN-, SPK+, SPK-
to AGND.....-0.3V to (V_{IN2} + 0.3V)
IN1, IN2 to IN3.....-0.3V to +0.3V
PGND1, PGND2 to AGND.....-0.3V to +0.3V
SPK+, SPK- Short Circuit to PGND2 or IN2 .....Continuous
Continuous Power Dissipation (T_A = +70°C)
28-Pin, Thin QFN 4mm x 4mm
(derate 28.6mW/°C above +70°C).....2286mW
Junction Temperature.....+150°C
Storage Temperature Range .....-65°C to +150°C
Lead Temperature (soldering, 10s) .....+300°C

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V_{IN1} = V_{IN2} = V_{IN3} = V_{DD} = 3.6V, V_{AGND} = V_{PGND1} = V_{PGND2} = 0V, circuit of Figure 2, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
V_{IN1}, V_{IN2}, V_{IN3} Operating Voltage			2.7		5.5	V
V_{DD} Operating Range			1.5		5.5	V
Undervoltage Lockout (UVLO) Threshold	V_{IN3} rising		2.25	2.45	2.65	V
UVLO Hysteresis				100		mV
V_{DD} Shutdown Threshold			0.450	0.865	1.350	V
IN1, IN2, IN3 Shutdown Supply Current (All Outputs Off)	V_{DD} = AGND	T_A = +25°C		0.1	1	µA
		T_A = +85°C		0.1		
	V_{DD} = 3.6V	T_A = +25°C		2	10	
		T_A = +85°C		2		
No-Load Supply Current	Charge pump inactive, 2 LEDs at 0.1mA setting, audio amplifier disabled, LDO1 and LDO2 disabled			70	120	µA
	LED driver disabled, audio amplifier disabled, and LDO1 and LDO2 enabled			170	250	
	Charge pump active, 1MHz switching, all LEDs at 25.6mA setting, audio amplifier disabled, LDO1 and LDO2 disabled			1.50	4.00	mA
	LED driver disabled, audio amplifier enabled, LDO1 and LDO2 disabled			6.6	20	
Thermal Shutdown				+160		°C
Thermal-Shutdown Hysteresis				20		°C
CHARGE PUMP						
Switching Frequency (f_{SW})	SYNC = 0			1000		kHz
	SYNC = 1, SW_MODE = 00		450	550	650	
	SYNC = 1, SW_MODE = 01		575	700	825	
	SYNC = 1, SW_MODE = 10			625 ± 25		

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ELECTRICAL CHARACTERISTICS (continued)

(V_{IN1} = V_{IN2} = V_{IN3} = V_{DD} = 3.6V, V_{AGND} = V_{PGND1} = V_{PGND2} = 0V, circuit of Figure 2, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
Soft-Start Time					0.1		ms
Regulation Voltage	(V_{IN1} - V_{NEG})				5		V
Open-Loop NEG Output Resistance	(0.5 x V_{IN1} - V_{NEG}) / I_{NEG}				1.75	3.5	Ω
Output Current	V_{IN1} = 3.2V, LED V_{FMAX} = 3.9V			154			mA
NEG Discharge Resistance in Shutdown	All LEDs disabled				10		kΩ
LED_ CURRENT REGULATORS							
Current Setting Range	$I_{LED_}$			0.1		25.6	mA
Current Accuracy	25.6mA setting	T_A = +25°C		-2	±1	+2	%
		T_A = -40°C to derating function start temperature (enabled by I^2C)		-5		+5	
	0.1mA setting, T_A = +25°C			-30	±5	+30	
Current-Derating-Function Start Temperature					+40		°C
Current-Derating-Function Slope	T_A = +40°C to +85°C				-1.67		%/°C
$R_{DS\ ON}$	Charge pump inactive				2.3	4.6	Ω
	Charge pump active				5	14	
Dropout Voltage	25.6mA setting (Note 2)	Charge pump inactive			72	120	mV
		Charge pump active			120	360	
Current Regulator Switchover Threshold	Charge pump inactive to active, $V_{LED_}$ falling			125	150	175	mV
Current Regulator Switchover Hysteresis					100		mV
Leakage Current in Shutdown	All LEDs disabled	T_A = +25°C			0.01	1	µA
		T_A = +85°C			0.1		
Off Blink Time	B7, B6 or B3, B2, SYNC = 0, Table 11		00		524		ms
			01		1048		
			10		2097		
			11		4194		
On Blink Time	B5, B4 or B1, B0, SYNC = 0, Table 11		00		66		ms
			01		131		
			10		262		
			11		524		
Ramp-Up/Down Time	LED__RU: B7, B6 or B3, B2 LED__RD: B5, B4 or B1, B0 SYNC = 0, Tables 8, 9, 10 (Note 3)		00		262		ms
			01		524		
			10		1048		
			11		2097		

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ELECTRICAL CHARACTERISTICS (continued)

(V_{IN1} = V_{IN2} = V_{IN3} = V_{DD} = 3.6V, V_{AGND} = V_{PGND1} = V_{PGND2} = 0V, circuit of Figure 2, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	CONDITIONS			MIN	TYP	MAX	UNITS
AUDIO AMPLIFIER							
Common-Mode Bias Voltage				0.95 x (V_{IN3} / 2)	V_{IN3} / 2	1.05 x (V_{IN3} / 2)	V
Output Offset Voltage	V_{AIN+} = V_{AIN-} = V_{IN3} / 2, audio gain = 0dB				±1		mV
Common-Mode Input Voltage				0.5		V_{IN3} - 1.2V	V
Audio Gain	Table 15, B3:B0				-3		dB
					0		
					3		
					6		
					9		
					12		
					15		
					18		
					21		
					24		
Audio Gain Accuracy				-3		+3	%
Input Resistance	Audio gain = -3dB			54.4	99.0	143.5	kΩ
	Audio gain = 0dB			49.1	89.2	129.3	
	Audio gain = 3dB			43.1	78.4	113.7	
	Audio gain = 6dB			36.8	66.9	97.0	
	Audio gain = 9dB			30.5	55.5	80.5	
	Audio gain = 12dB			24.6	44.7	64.8	
	Audio gain = 15dB			19.3	35.2	51.0	
	Audio gain = 18dB			14.8	26.9	39.0	
	Audio gain = 21dB			11.1	20.2	29.3	
	Audio gain = 24dB			8.2	15.0	22.0	
Common-Mode Rejection Ratio	V_{IN2} = V_{IN3} = 3.6V				46		dB
	f = 1kHz, V_{IN2} = V_{IN3} = 3.6V				46		
Power-Supply Rejection Ratio	V_{AIN+} = V_{AIN-} = V_{IN3} / 2, 100mV_{P-P} at V_{IN3}		f = 217Hz		65		dB
			f = 20kHz		50		
Output Power	THD+N = 1%, f = 1kHz (Note 4)	V_{IN3} = 3.6V	R_L = 8Ω	0.36	0.5		W
			R_L = 4Ω		0.85		
		V_{IN3} = 5V	R_L = 8Ω	0.8	1.1		
			R_L = 4Ω		2.0		
Total Harmonic Distortion Plus Noise	R_L = 8Ω, f = 1kHz, P_{OUT} = 0.25W, V_{IN2} = V_{IN3} = 3.6V				0.05		%

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ELECTRICAL CHARACTERISTICS (continued)

($V_{IN1} = V_{IN2} = V_{IN3} = V_{DD} = 3.6V$, $V_{AGND} = V_{PGND1} = V_{PGND2} = 0V$, circuit of Figure 2, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Signal-to-Noise Ratio	$R_L = 8\Omega$, f = 1kHz, P_{OUT} = 0.25W, $V_{IN2} = V_{IN3} = 3.6V$	Fixed-frequency mode (FFM)		91		dB
		Spread-spectrum mode (SSM)		89		
		FFM A weighted		93		
		SSM A weighted		91		
Oscillator Frequency (f_{osc})	SW_MODE = 00		900	1100	1300	kHz
	SW_MODE = 01		1150	1400	1650	
	SW_MODE = 10			1250 ±50		
Differential Input Resistance	Shutdown mode only			100		kΩ
Output Current Limit	SPK+, SPK- short circuited to PGND2 or to IN2			2		A
Wake-Up Delay After Short Circuit				110		µs
LDO1						
Output Voltage V_{LDO1}	3.6V ≤ V_{IN3} ≤ 5.5V, 1mA ≤ I_{LDO1} ≤ 300mA		1.164	1.200	1.236	V
Maximum Output Current			300			mA
Output Current Limit	V_{LDO1} = 0V		400	650	1000	mA
Dropout Voltage	I_{LDO1} = 200mA, T_A = +25°C (Note 5)			150	300	mV
Line Regulation	V_{IN3} stepped from 3.4V to 5.5V, I_{LDO1} = 150mA			2.4		mV
Load Regulation	I_{LDO1} stepped from 1mA to 300mA			25		mV
Power-Supply Rejection $\Delta V_{IN3}/\Delta V_{LDO1}$	10Hz to 10kHz, I_{LDO1} = 30mA			70		dB
Output Voltage Noise (RMS)	100Hz to 100kHz, I_{LDO1} = 30mA			45		μV_{RMS}

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ELECTRICAL CHARACTERISTICS (continued)

(V_{IN1} = V_{IN2} = V_{IN3} = V_{DD} = 3.6V, V_{AGND} = V_{PGND1} = V_{PGND2} = 0V, circuit of Figure 2, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Programmable Output Voltage	I_{LDO1} = 50mA control bits B3:B0; see Table 13	0000	1.164	1.2	1.236	V
		0001	1.261	1.3	1.339	
		0010	1.455	1.5	1.545	
		0011	1.552	1.6	1.648	
		0100	1.746	1.8	1.854	
		0101	1.843	1.9	1.957	
		0110	1.940	2.0	2.060	
		0111	2.231	2.3	2.369	
		1000	2.425	2.5	2.575	
		1001	2.522	2.6	2.678	
		1010	2.619	2.7	2.781	
		1011	2.716	2.8	2.884	
		1100	2.813	2.9	2.987	
		1101	2.910	3.0	3.090	
		1110	3.007	3.1	3.193	
		1111	3.104	3.2	3.296	
Shutdown Output Impedance	LDO1 disabled through I^2C			1		kΩ
LDO2						
Output Voltage V_{LDO2}	3.6V ≤ V_{IN3} ≤ 5.5V, 1mA ≤ I_{LDO2} ≤ 200mA		1.455	1.500	1.545	V
Maximum Output Current			200			mA
Output Current Limit	V_{LDO2} = 0V		250	550	750	mA
Dropout Voltage	I_{LDO2} = 133mA, T_A = +25°C (Note 5)			100	200	mV
Line Regulation	V_{IN3} stepped from 3.4V to 5.5V, I_{LDO2} = 100mA			2.4		mV
Load Regulation	I_{LDO2} stepped from 1mA to 200mA			25		mV
Power-Supply Rejection $\Delta V_{IN3}/\Delta V_{LDO2}$	10Hz to10kHz, I_{LDO2} = 20mA			70		dB
Output Voltage Noise (RMS)	100Hz to100kHz, I_{LDO2} = 20mA			45		μV_{RMS}

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ELECTRICAL CHARACTERISTICS (continued)

(V_{IN1} = V_{IN2} = V_{IN3} = V_{DD} = 3.6V, V_{AGND} = V_{PGND1} = V_{PGND2} = 0V, circuit of Figure 2, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	CONDITIONS		MIN	TYP	MAX	UNITS
Programmable Output Voltage	I_{LDO2} = 50mA control bits B3:B0; see Table 14	0000	1.455	1.5	1.545	V
		0001	1.552	1.6	1.648	
		0010	1.746	1.8	1.854	
		0011	1.940	2.0	2.060	
		0100	2.134	2.2	2.266	
		0101	2.231	2.3	2.369	
		0110	2.328	2.4	2.472	
		0111	2.425	2.5	2.575	
		1000	2.522	2.6	2.678	
		1001	2.619	2.7	2.781	
		1010	2.716	2.8	2.884	
		1011	2.813	2.9	2.987	
		1100	2.910	3.0	3.090	
		1101	3.007	3.1	3.193	
		1110	3.104	3.2	3.296	
		1111	3.201	3.3	3.399	
Shutdown Output Impedance	LDO2 disabled through I²C			1		kΩ
I²C INTERFACE (Figure 8)						
Logic Input High Voltage			0.7 x V_{DD}			V
Logic Input Low Voltage					0.3 x V_{DD}	V
Logic Input Current	V_{IL} = 0V or V_{IH} = V_{DD}	T_A = +25°C	-1	0.01	+1	µA
		T_A = +85°C		0.1		
SDA Output Low Voltage	I_{SDA} = 3mA			0.03	0.4	V
I²C Clock Frequency					400	kHz
Bus-Free Time Between START and STOP	t_{BUF}		1.3			µs
Hold Time Repeated START Condition	t_{HD_STA}		0.6	0.1		µs
SCL Low Period	t_{LOW}		1.3	0.2		µs
SCL High Period	t_{HIGH}		0.6	0.2		µs
Setup Time Repeated START Condition	t_{SU_STA}		0.6	0.1		µs

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White LED Charge Pump with Mono Class D Audio Amp and Dual LDO

ELECTRICAL CHARACTERISTICS (continued)

(V_{IN1} = V_{IN2} = V_{IN3} = V_{DD} = 3.6V, V_{AGND} = V_{PGND1} = V_{PGND2} = 0V, circuit of Figure 2, T_A = -40°C to +85°C, unless otherwise noted. Typical values are at T_A = +25°C.) (Note 1)

PARAMETER	CONDITIONS	MIN	TYP	MAX	UNITS
SDA Hold Time	t_{HD_DAT}	0	-0.01		µs
SDA Setup Time	t_{SU_DAT}	100	50		ns
Setup Time for STOP Condition	t_{SU_STO}	0.6	0.1		µs

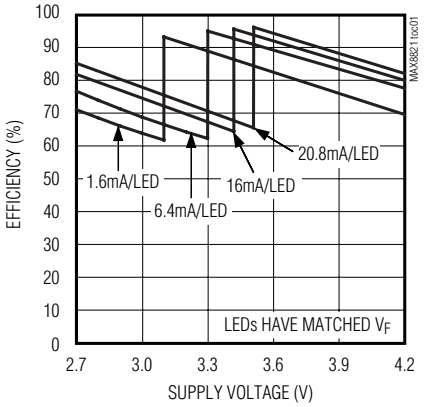
Note 1: Limits are 100% production tested at T_A = +25°C. Limits over the operating temperature range are guaranteed by design.
Note 2: Dropout voltage is defined as the LED_ to GND voltage when the current into LED_ drops 10% from the value at $V_{LED_}$ = 0.5V.
Note 3: Ramp-up time is from 0mA to full scale; ramp-down time is from full scale to 0mA.
Note 4: Output power is specified by a combination of a functional output current test and characterization analysis.
Note 5: The dropout voltage is defined as $V_{IN_}$ - V_{OUT} when V_{OUT} is 100mV below the nominal value of V_{OUT}. The specification only applies when V_{OUT} ≥ 3.0V.

Typical Operating Characteristics

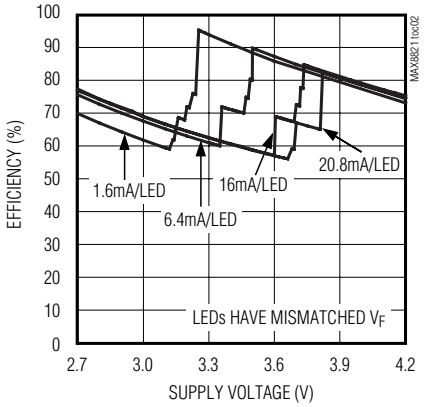
(V_{IN1} = V_{IN2} = V_{IN3} = V_{DD} = 3.6V, V_{AGND} = V_{PGND1} = V_{PGND2} = 0V, circuit of Figure 2, T_A = +25°C, unless otherwise noted.)

LED CHARGE PUMP

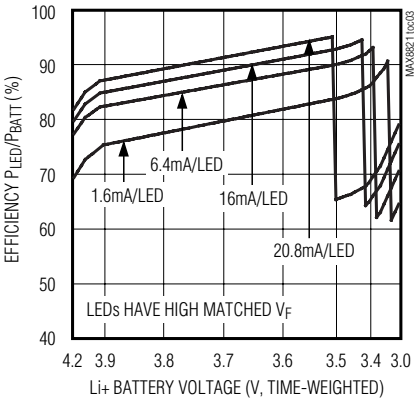
EFFICIENCY vs. SUPPLY VOLTAGE (DRIVING SIX LEDS)



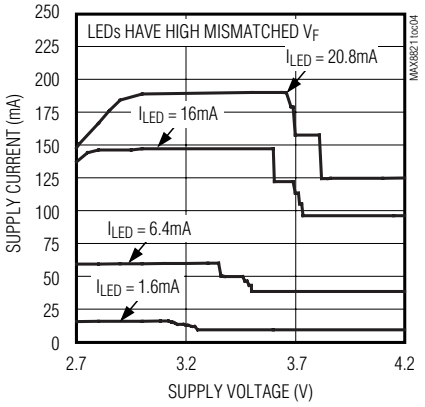
EFFICIENCY vs. SUPPLY VOLTAGE (DRIVING SIX LEDS)



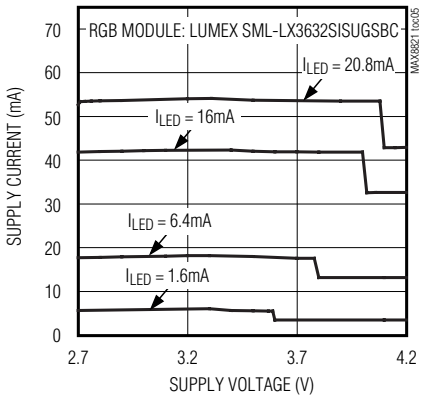
EFFICIENCY vs. Li+ BATTERY VOLTAGE DRIVING SIX LEDs



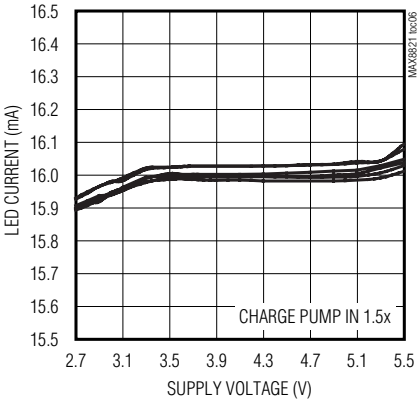
SUPPLY CURRENT vs. SUPPLY VOLTAGE (DRIVING SIX LEDs)



SUPPLY CURRENT vs. SUPPLY VOLTAGE (RGB MODULE)



LED CURRENT MATCHING vs. SUPPLY VOLTAGE (16mA/LED)



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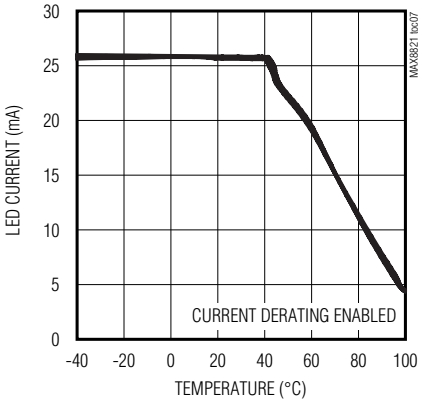
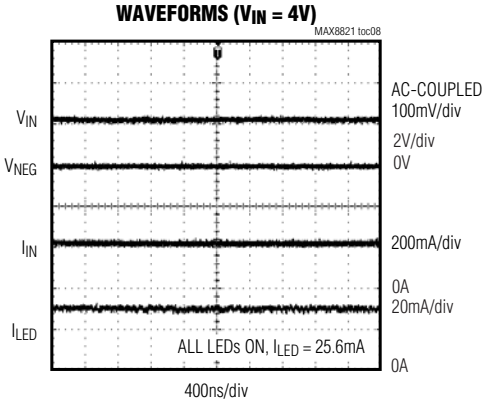
Typical Operating Characteristics (continued)

($V_{IN1} = V_{IN2} = V_{IN3} = V_{DD} = 3.6V$, $V_{AGND} = V_{PGND1} = V_{PGND2} = 0V$, circuit of Figure 2, $T_A = +25°C$, unless otherwise noted.)

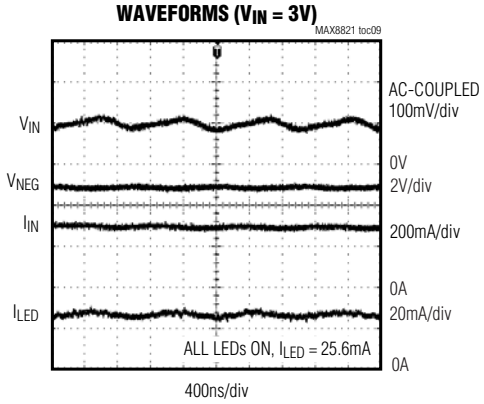
LED CURRENT vs. AMBIENT TEMPERATURE



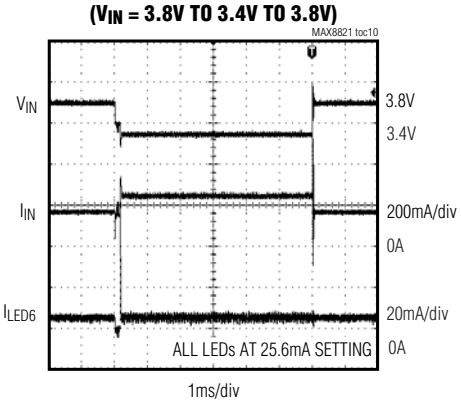
1x MODE OPERATING WAVEFORMS (V_{IN} = 4V)



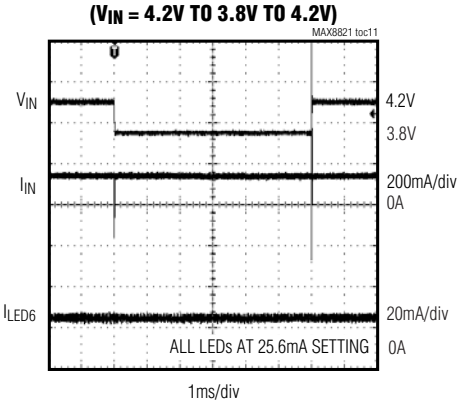
1.5x MODE OPERATING WAVEFORMS (V_{IN} = 3V)



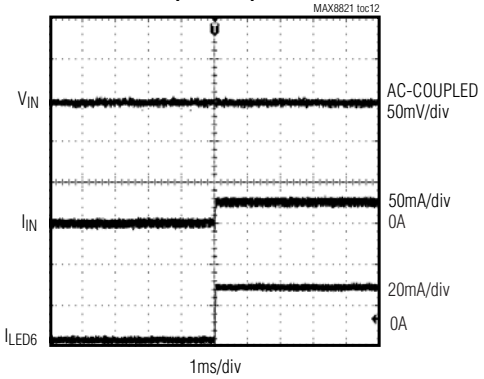
LED LINE TRANSIENT WITH MODE CHANGE (V_{IN} = 3.8V TO 3.4V TO 3.8V)



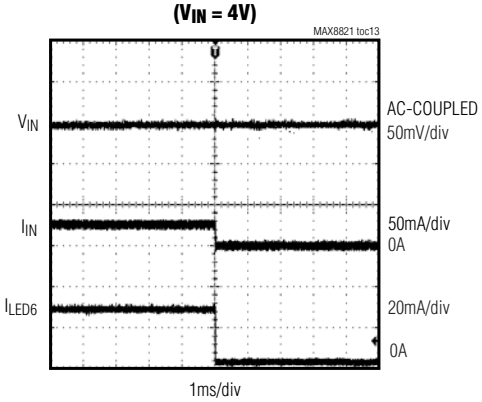
LED LINE TRANSIENT WITH MODE CHANGE (V_{IN} = 4.2V TO 3.8V TO 4.2V)



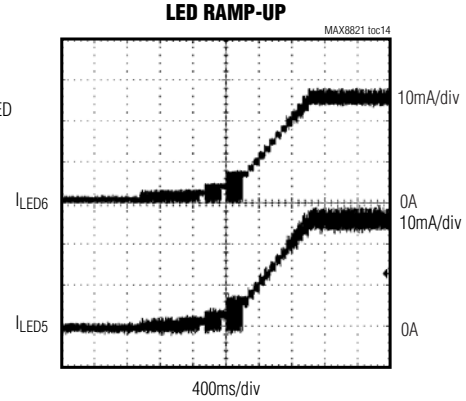
LED STARTUP WAVEFORMS (V_{IN} = 4V)



LED SHUTDOWN WAVEFORMS (V_{IN} = 4V)



LED RAMP-UP



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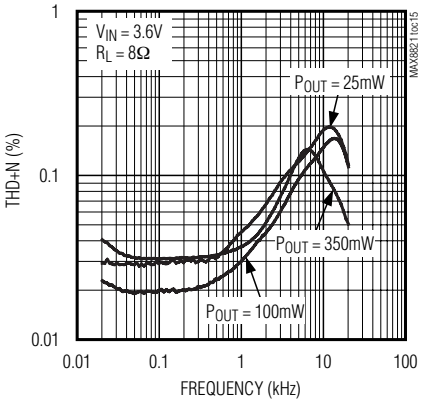
White LED Charge Pump with Mono Class D Audio Amp and Dual LDO

Typical Operating Characteristics (continued)

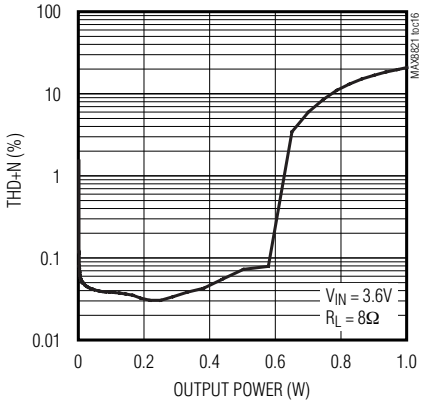
(V_{IN1} = V_{IN2} = V_{IN3} = V_{DD} = 3.6V, V_{AGND} = V_{PGND1} = V_{PGND2} = 0V, circuit of Figure 2, T_A = +25°C, unless otherwise noted.)

CLASS D AMP

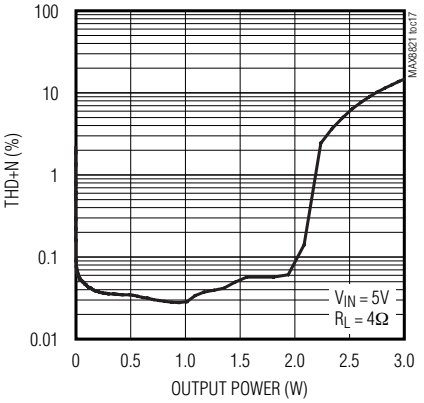
TOTAL HARMONIC DISTORTION PLUS NOISE vs. FREQUENCY



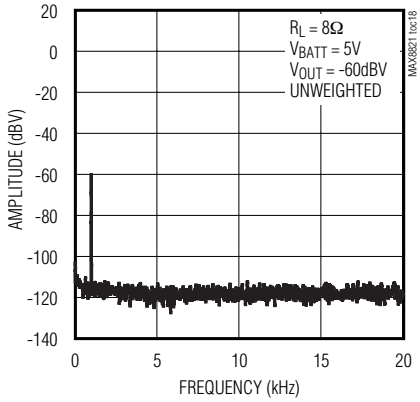
TOTAL HARMONIC DISTORTION vs. OUTPUT POWER



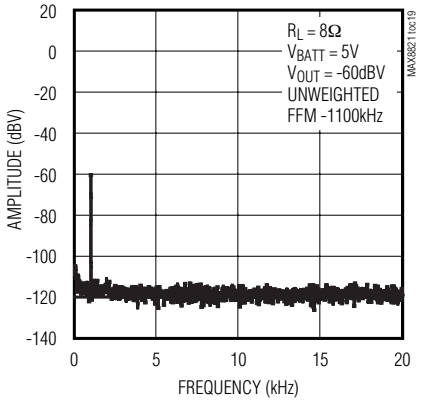
TOTAL HARMONIC DISTORTION vs. OUTPUT POWER



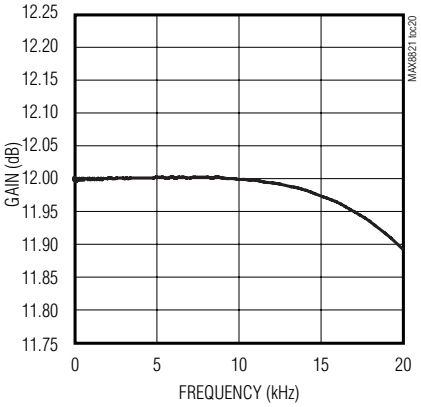
SPREAD-SPECTRUM-MODE OUTPUT SPECTRUM vs. FREQUENCY



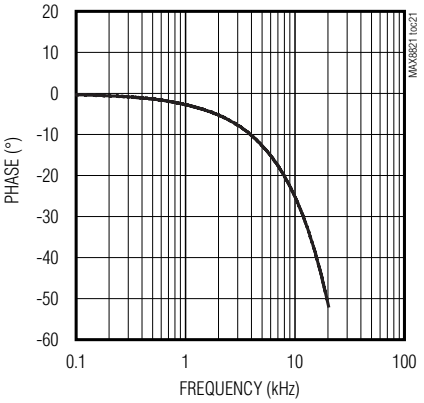
FIXED-FREQUENCY-MODE OUTPUT SPECTRUM vs. FREQUENCY



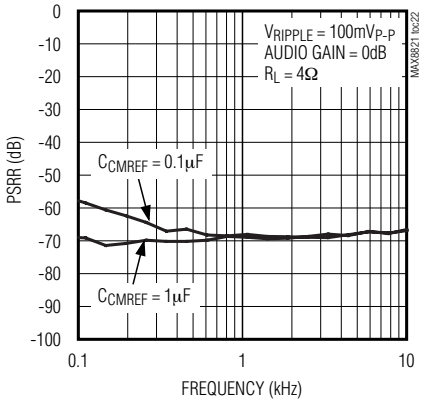
AUDIO AMPLIFIER GAIN vs. FREQUENCY



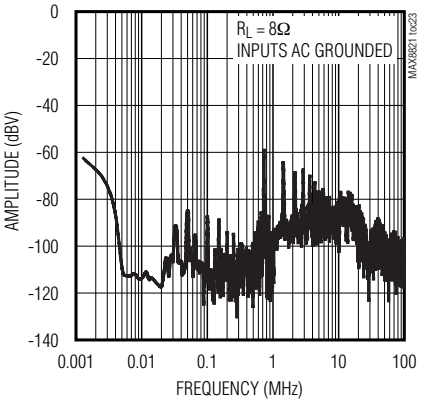
AUDIO AMPLIFIER PHASE vs. FREQUENCY



AUDIO AMPLIFIER PSRR vs. FREQUENCY



WIDEBAND OUTPUT SPECTRUM SPREAD-SPECTRUM MODE



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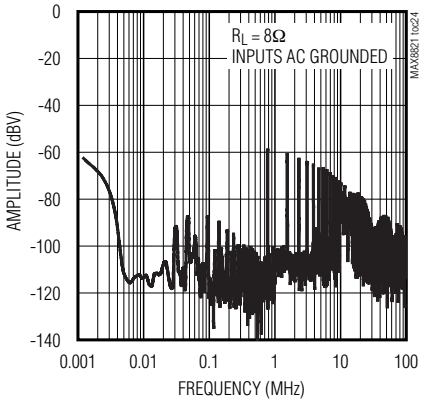
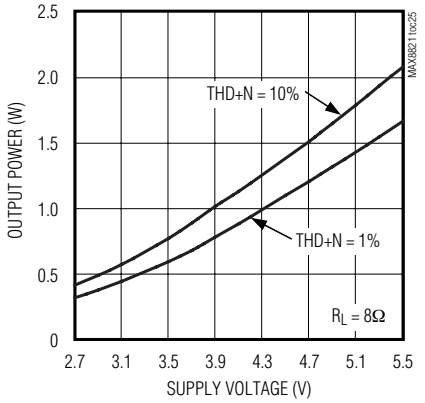
Typical Operating Characteristics (continued)

($V_{IN1} = V_{IN2} = V_{IN3} = V_{DD} = 3.6V$, $V_{AGND} = V_{PGND1} = V_{PGND2} = 0V$, circuit of Figure 2, $T_A = +25°C$, unless otherwise noted.)

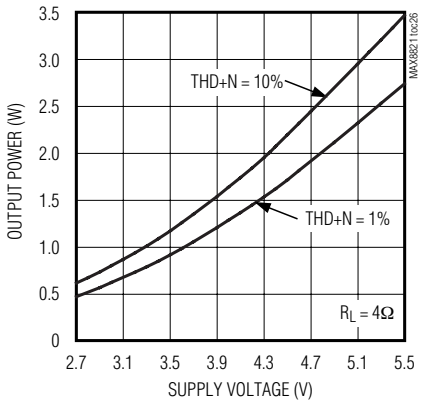
WIDEBAND OUTPUT SPECTRUM FIXED-FREQUENCY MODE



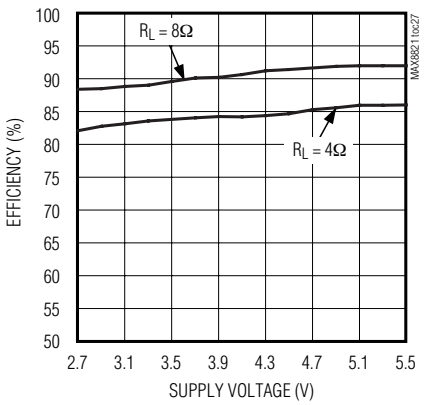
OUTPUT POWER vs. SUPPLY VOLTAGE



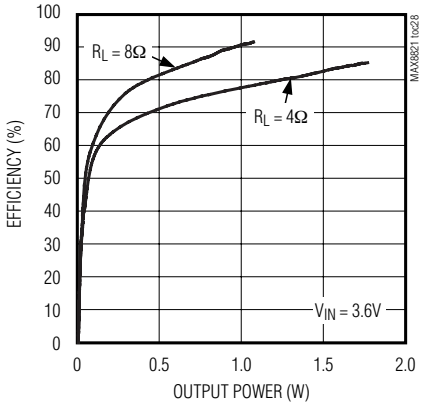
OUTPUT POWER vs. SUPPLY VOLTAGE



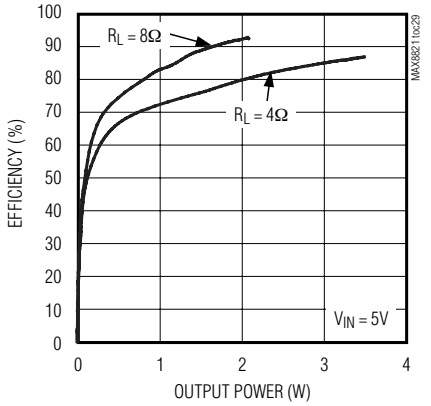
EFFICIENCY vs. SUPPLY VOLTAGE



EFFICIENCY vs. OUTPUT POWER



EFFICIENCY vs. OUTPUT POWER



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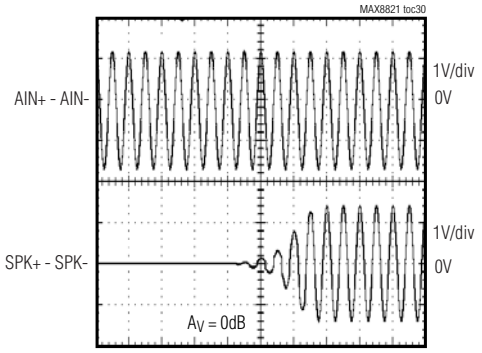
White LED Charge Pump with Mono Class D Audio Amp and Dual LDO

Typical Operating Characteristics

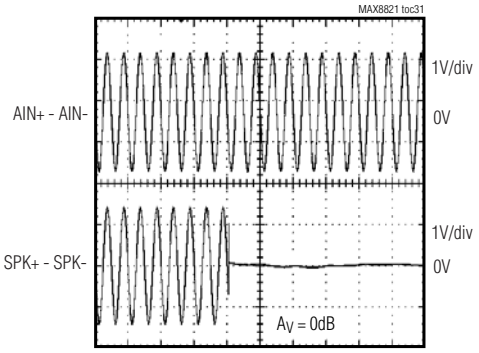
($V_{IN1} = V_{IN2} = V_{IN3} = V_{DD} = 3.6V$, $V_{AGND} = V_{PGND1} = V_{PGND2} = 0V$, circuit of Figure 2, $T_A = +25°C$, unless otherwise noted.)

DUAL LDOs

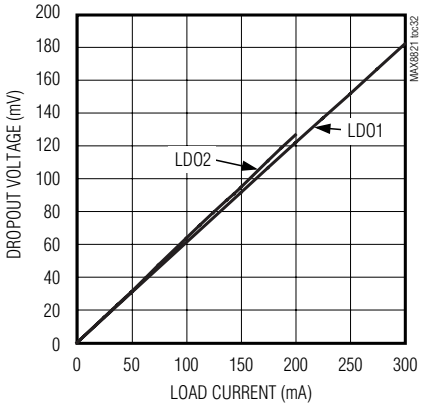
STARTUP WAVEFORMS



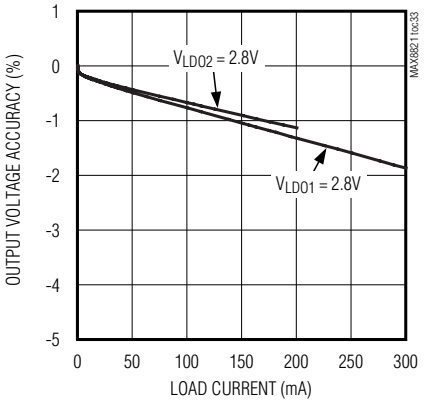
SHUTDOWN WAVEFORMS



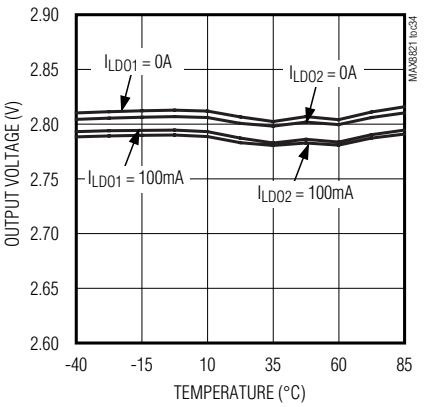
LDO DROPOUT VOLTAGE vs. LOAD CURRENT



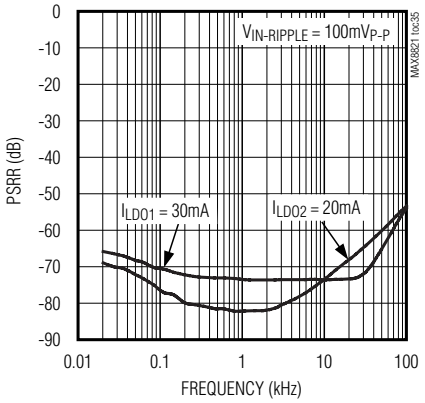
LDO OUTPUT VOLTAGE ACCURACY vs. LOAD CURRENT



LDO OUTPUT VOLTAGE vs. TEMPERATURE



LDO PSRR vs. FREQUENCY



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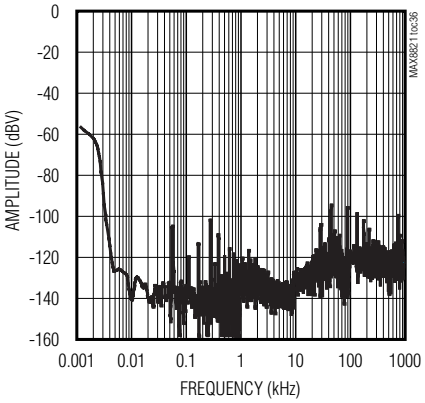
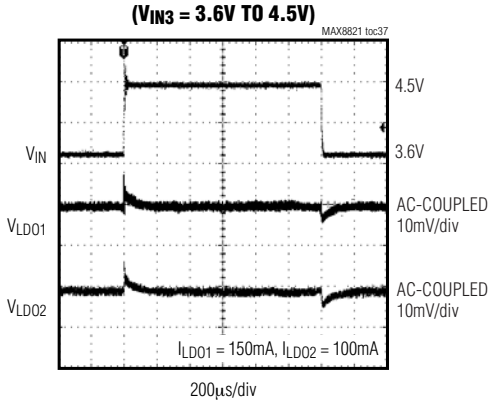
Typical Operating Characteristics

($V_{IN1} = V_{IN2} = V_{IN3} = V_{DD} = 3.6V$, $V_{AGND} = V_{PGND1} = V_{PGND2} = 0V$, circuit of Figure 2, $T_A = +25°C$, unless otherwise noted.)

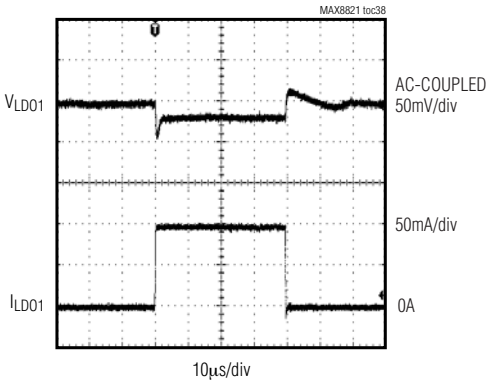
LDO OUTPUT SPECTRUM



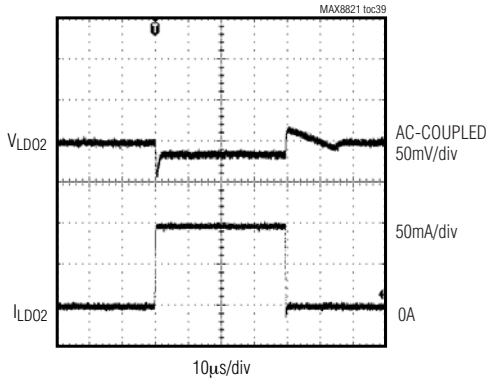
LDO LINE TRANSIENT (V_{IN3} = 3.6V TO 4.5V)



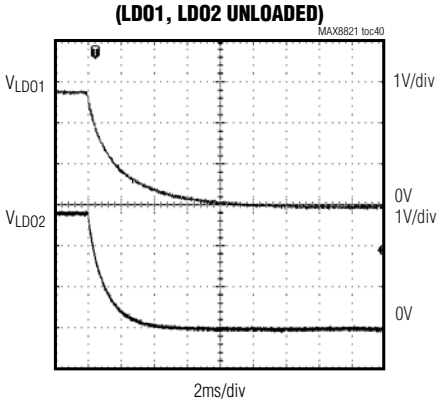
LDO1 LOAD TRANSIENT



LDO2 LOAD TRANSIENT



LDO SHUTDOWN RESPONSE (LDO1, LDO2 UNLOADED)



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White LED Charge Pump with Mono Class D Audio Amp and Dual LDO

Pin Description

PIN	NAME	FUNCTION
1	V_{DD}	I^2C Input Supply Voltage. The V_{DD} supply range is 1.5V to 5.5V. Drive V_{DD} high to enable the I^2C control. Drive V_{DD} low to place the IC into shutdown mode.
2	CMREF	Audio Common-Mode Reference Voltage. Bypass CMREF with a 0.1µF ceramic capacitor to AGND as close as possible to the IC.
3	AIN+	Noninverting Audio Input
4	AIN-	Inverting Audio Input
5	PGND2	Audio Amplifier Power Ground. Connect PGND2 to the system ground plane.
6	SPK-	Audio Amplifier Negative Output
7	SPK+	Audio Amplifier Positive Output
8	IN2	Audio Amplifier Output Buffer Supply Voltage Input. The input voltage range is 2.7V to 5.5V. Connect IN2 directly to IN1 and IN3. Bypass IN2 to PGND2 with a 1µF ceramic capacitor as close as possible to the IC. IN2 is high impedance during shutdown.
9	LDO2	200mA LDO Output. Bypass LDO2 to AGND with a 1µF ceramic capacitor. LDO2 is disabled through the I^2C interface.
10	LDO1	300mA LDO Output. Bypass LDO1 to AGND with a 2.2µF ceramic capacitor. LDO1 is disabled through the I^2C interface.
11	SCL	I^2C Clock Input. Data is read on the rising edge of V_{SCL}.
12	SDA	I^2C Data Input. Data is read on the rising edge of V_{SCL}..
13	AGND	Analog Ground. Connect AGND to the system ground plane. AGND is also internally connected to the exposed paddle.
14	REF	Reference Bypass. Bypass REF with a 0.1µF ceramic capacitor to AGND as close as possible to the IC.
15–20	LED1–LED6	LED Current Regulators. Current flowing into LED_ is based upon the internal I^2C registers. Connect LED_ to the cathodes of the external LEDs. LED_ is high impedance during shutdown. If unused, short LED_ to IN1 to disable the regulator.
21	NEG	Charge-Pump Negative Output. Connect a 1µF ceramic capacitor from NEG to AGND. In shutdown, an internal 10kΩ resistor connects NEG to AGND.
22	C2N	Transfer Capacitor 2 Negative Connection. Connect a 1µF ceramic capacitor from C2P to C2N.
23	C1N	Transfer Capacitor 1 Negative Connection. Connect a 1µF ceramic capacitor from C1P to C1N.
24	C2P	Transfer Capacitor 2 Positive Connection. Connect a 1µF ceramic capacitor from C2P to C2N.
25	C1P	Transfer Capacitor 1 Positive Connection. Connect a 1µF ceramic capacitor from C1P to C1N.
26	IN1	Charge-Pump Supply Voltage Input. The input voltage range is 2.7V to 5.5V. Connect IN1 directly to IN2 and IN3. Bypass IN1 to PGND1 with a 2.2µF ceramic capacitor as close as possible to the IC. IN1 is high impedance during shutdown.
27	PGND1	Charge-Pump Power Ground. Connect PGND1 to the system ground plane.
28	IN3	Input Voltage Supply for LDO1, LDO2, REF, Class D Preamplifier, and Class D Amplifier Modulator Core. The input voltage range is 2.7V to 5.5V. Connect IN3 directly to IN1 and IN2. Bypass IN3 to AGND with a 2.2µF ceramic capacitor as close as possible to the IC. IN3 is high impedance during shutdown.
—	EP	Exposed Paddle. Connect the exposed paddle to AGND directly under the IC. Exposed paddle is internally connected to AGND.

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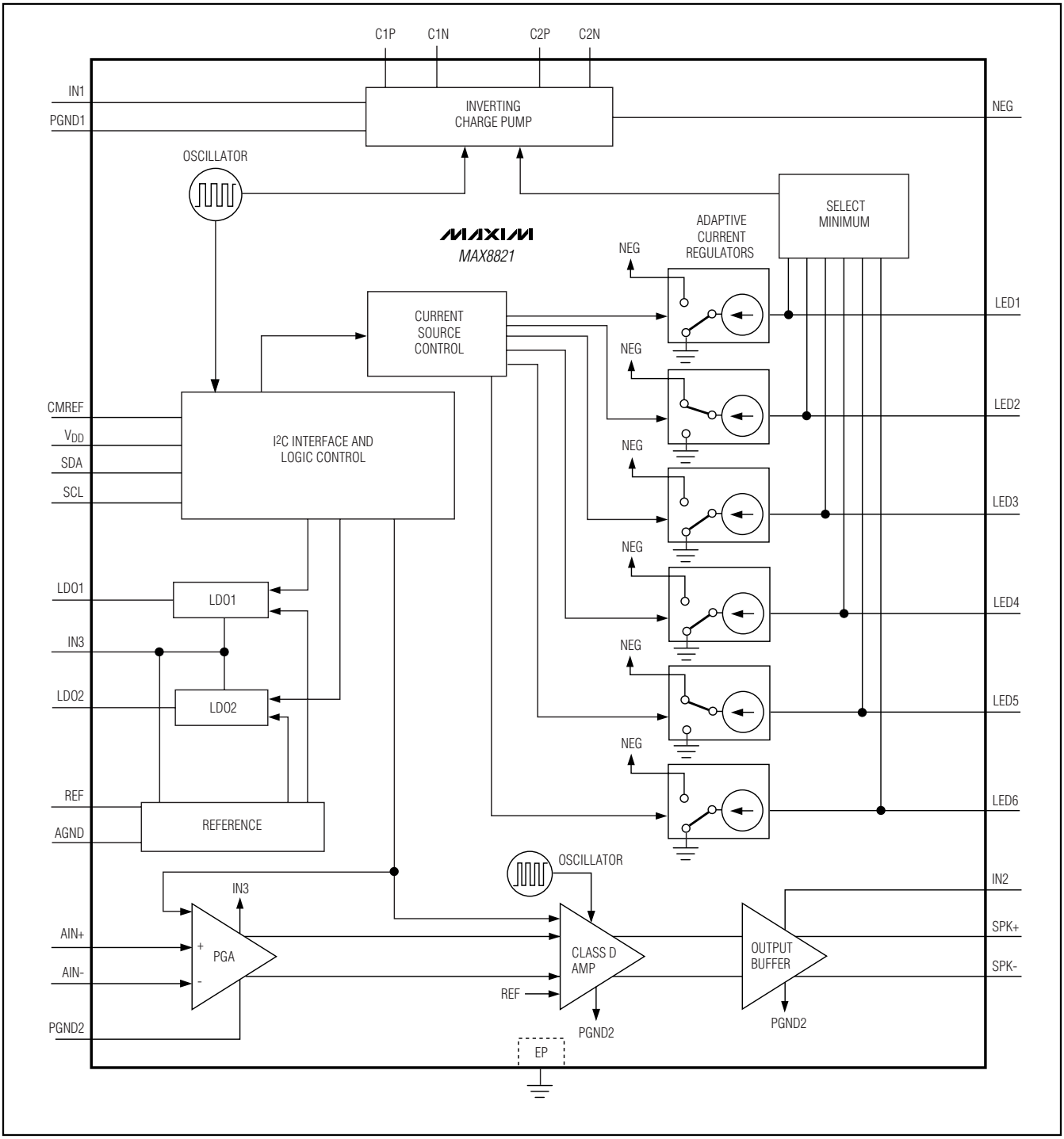

Figure 1. Block Diagram

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White LED Charge Pump with Mono Class D Audio Amp and Dual LDO

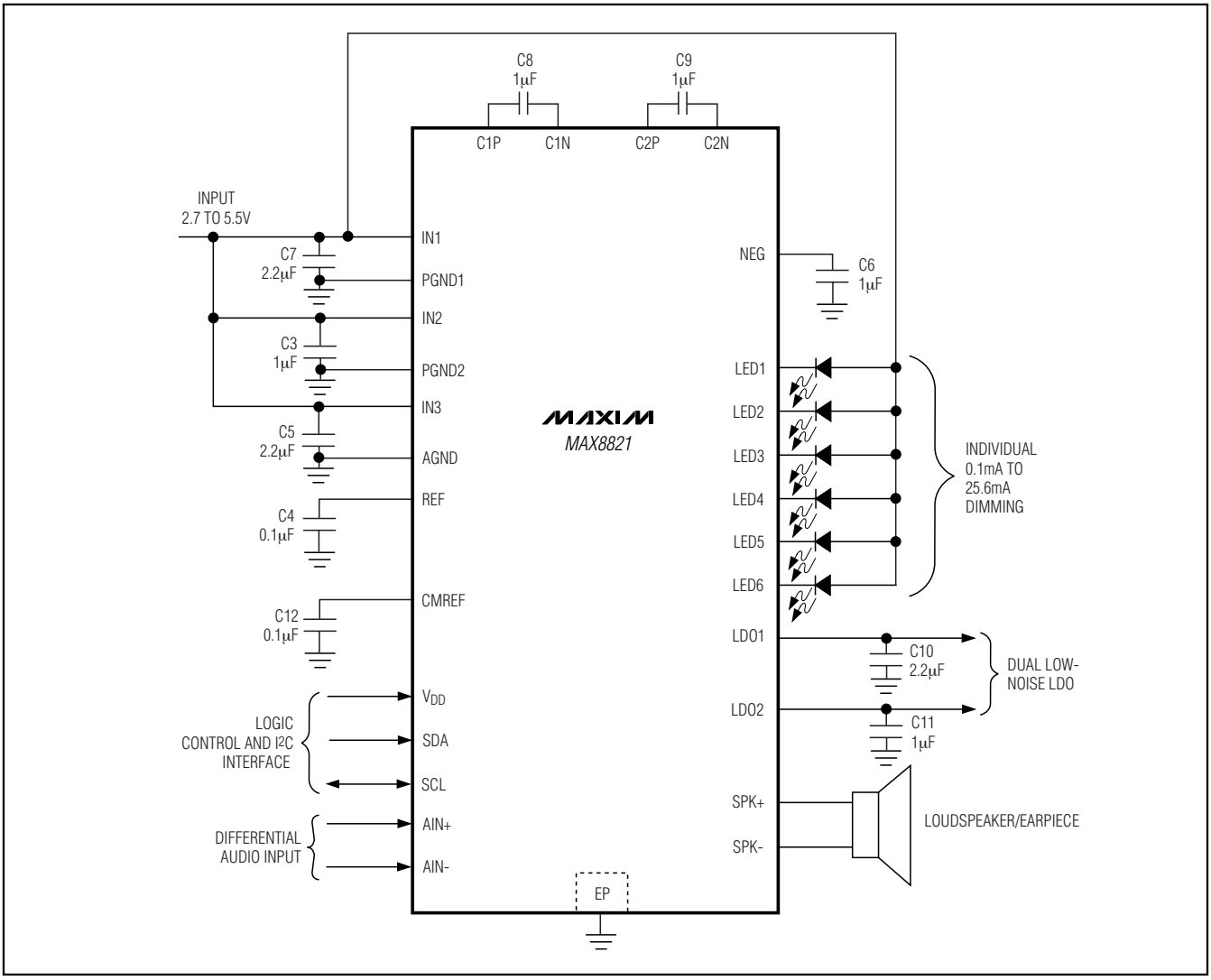

Figure 2. Typical Application Circuit

Detailed Description

The MAX8821 integrates a charge pump for white LED display backlighting, an audio loudspeaker amplifier, and dual LDO for camera functions. It includes soft-start, thermal shutdown, open-circuit and short-circuit protections for the white LEDs, audio amplifier, and LDOs. Figure 1 is the block diagram, and Figure 2 shows the typical application circuit.

LED Charge Pump

The MAX8821 features an inverting charge pump and six current regulators capable of 25.6mA each to drive six LEDs. The current regulators are matched to within ±1% (typ), providing uniform white LED brightness for LCD backlight applications. To maximize efficiency, the current regulators operate with as little as 0.15V voltage drop. Individual white LED current regulators conduct current to GND or NEG to extend usable battery life. In the case of mismatched forward voltage of white LEDs, only the white LEDs requiring higher voltage are switched to direct current to NEG instead of GND, further raising efficiency and reducing battery current drain. The regulation scheme is optimized to ensure low EMI and low input ripple. The on-chip ambient temperature derating function safely allows bright 25.6mA

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full-scale output current while automatically reducing current gradually above +40°C in accordance with popular LED ratings. The on-chip derating feature can be enabled, or disabled, using the I²C interface.

Current Regulator Switchover

When V_{IN} is higher than the forward voltage of the white LED plus the 0.15V headroom of the current regulator, the LED current returns through ground. If this condition is satisfied for all six white LEDs the charge pump remains inactive. When the input voltage drops so that the current regulator head room cannot be maintained for any of the individual white LEDs, the inverting charge pump activates and generates a voltage on NEG that is no greater than 5V below V_{IN}. Each current regulator contains circuitry that detects when it is in dropout and switches that current regulator return path from GND to NEG. Since this is done on an LED-by-LED basis, the LED current is switched for only the individual LED requiring higher voltage, thus minimizing power consumption.

Ramp-Up and Ramp-Down Function

The LED drivers in the MAX8821 provide ramp-up and ramp-down of LED current for smooth transitions between different brightness settings. A controlled ramp is used when the LED current level is changed, when the LEDs are enabled, and when the LEDs are disabled. The LED currents ramp up and down smoothly on a pseudo-log scaling of the LED current sources (Figures 3 and 4). Each LED source has an individual ramp control making it possible to ramp different LEDs at different rates. The ramp-up and ramp-down (t_{RAMP}) LED current times are controlled by the LED_RU and LED_RD control bits (Tables 8, 9, and 10). The LED_RP_EN bit enables and disables the ramps. The MAX8821 increases/decreases the current one step every $t_{RAMP}/32$ until the desired current is reached.

Blink Timer

The current regulators for LED5 and LED6 feature a blink function. The OFF and ON time for LED5 and LED6 can be set using the I²C interface (Table 11). See Figure 5.

Combining Blink Timer and Ramp Function

To combine the ramp function together with the blink timer for LED5 and/or LED6, special timing considerations need to be fulfilled. It is recommended to keep the ramp-up timer shorter than the ON blink timer and the ramp-down timer shorter than the OFF blink timer. Failing to comply with these timing constraints results in the LED_ not reaching the programmed current (LED_[4:0], Tables 6 and 7) during the ON time and the LED_ current not returning to 0mA during the off time. See the following equations to ensure proper operation:

$$t_{ON_BLINK} \geq \frac{t_{LED_RU}}{32}(LED_[4:0]+1)$$

$$t_{OFF_BLINK} \geq \frac{t_{LED_RD}}{32}(LED_[4:0]+1)$$

where LED_[4:0] is the programmed current set by I²C (see Tables 6 and 7).

Figure 6 shows combining ramp function and blink timer.

LED Short- and Open-Circuit Protection

If any LED fails as an open circuit, the corresponding LED_ is internally connected to ground and the charge pump is enabled. To disable the corresponding current regulator, short any unused LED_ to IN1. The MAX8821 contains special circuitry to detect this condition and disables the corresponding current regulator to avoid wasting battery power.

Temperature Derating

The MAX8821 contains a derating function that automatically limits the LED current at high temperatures in accordance with the recommended derating curve of popular white LEDs. The derating function enables the safe usage of higher LED current at room temperature, thus reducing the number of LEDs required to backlight the display. The derating circuit limits the LED current by reducing the LED current above +40°C at approximately 1.67%/°C. The temperature derating function is enabled/disabled using the I²C interface and by default is disabled.

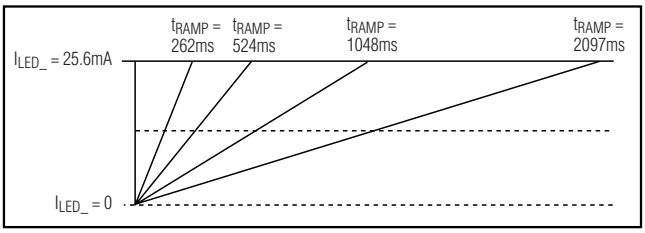

Figure 3. Ramp-Up Behavior

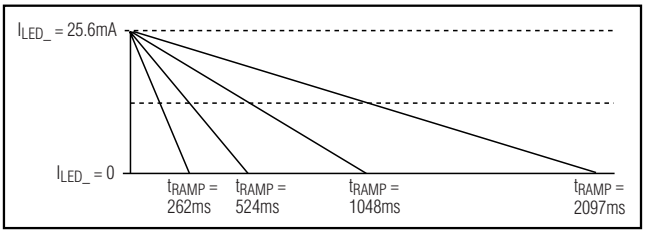

Figure 4. Ramp-Down Behavior

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White LED Charge Pump with Mono Class D Audio Amp and Dual LDO

Audio Amplifier

The audio amplifier in the MAX8821 is a 2W Class D loudspeaker amplifier. The amplifier features a low-power shutdown mode and industry-leading click-and-pop suppression. The amplifier also features a programmable gain control through an I²C interface. The amplifier operates from a single 2.7V to 5.5V supply (V_{IN3} = V_{IN2}) and features an internally generated common-mode bias voltage of V_{IN3} / 2 referenced to ground.

Click-and-Pop Suppression

The MAX8821 features Maxim's industry-leading click-and-pop suppression circuitry. During startup, the amplifier's common-mode bias voltage ramps to the DC bias point. When entering shutdown, the amplifier outputs are high impedance with 100kΩ between both inputs. This scheme minimizes the energy present in the audio band.

Class D Amplifier

The MAX8821 ultra-low-EMI, filterless, Class D audio power amplifier features several improvements to switch mode amplifier technology. The MAX8821 audio amplifier features output driver AEL circuitry to reduce EMI. Zero dead-time technology maintains state-of-the-art efficiency and THD+N performance by allowing the output MOSFETs to switch simultaneously without cross-conduction.

A unique filterless modulation scheme and spread-spectrum mode create a compact, flexible, low-noise, efficient audio power amplifier while occupying minimal board space. The differential input architecture reduces common-mode noise pickup with or without the use of input-coupling capacitors. The MAX8821 audio amplifier can also be configured as a single-ended input amplifier without performance degradation. The input capacitors C_{IN} (Figure 7) are required for single-ended input applications and are typically 1µF.

The output of the MAX8821 shuts down if the output current reaches approximately 2A. Each output MOSFET has its own short-circuit protection. This protection scheme allows the amplifier to survive shorts to either supply rail. After a thermal overload or short circuit, the device remains disabled for a minimum of 110µs before attempting to return to normal operation. The amplifier shuts down immediately and waits another 110µs before turning on if the fault condition remains. This operation causes the output to pulse during a persistent fault.

Comparators monitor the MAX8821 inputs and compare the complementary input voltages to the sawtooth waveform. The comparators trip when the input magnitude of the sawtooth exceeds their corresponding input voltage.

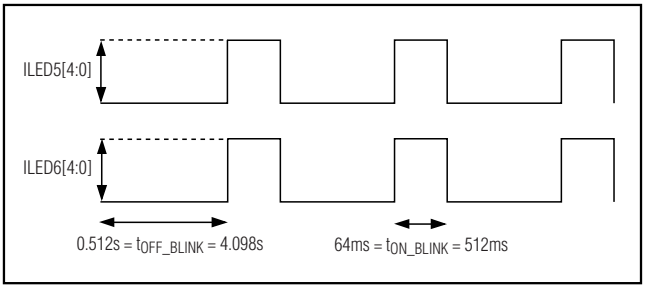

Figure 5. Blink Timer Behavior

Both comparators reset at a fixed time after the rising edge of the second comparator trip point, generating a minimum width pulse $t_{ON(MIN)}$ at the output of the second comparator. As the input voltage increases or decreases, the duration of the pulse at one output increases (the first comparator to trip), while the other output pulse duration remains at $t_{ON(MIN)}$. This causes the net voltage across the speaker (SPK+ - SPK-) to change.

Adjustable Differential Gain

The audio amplifier has an internal gain control. The gain of the input amplifiers is controlled through the I²C interface. The gain setting of the input amplifier can be set from -3dB to +24dB (Table 15). This allows the amplifier to be used for both hands-free and for receiver mode without any external components.

Input Filter

The fully differential amplifier inputs can be biased at voltages other than midsupply. The common-mode feedback circuit adjusts for input bias, ensuring the outputs are still biased at midsupply. Input capacitors are not required as long as the common-mode input voltage is within the specified range listed in the *Electrical Characteristics* table. If input capacitors are used, input capacitor C_{IN}, in conjunction with on-chip R_{INT}, forms a highpass filter that removes the DC bias from an incoming signal. The AC-coupling capacitor allows the amplifier to bias the signal to an optimum DC level. Assuming zero-source impedance, the -3dB point of the highpass filter is given by:

$$f_{-3dB} = \frac{1}{2 \times \pi \times R_{INT} \times C_{IN}}$$

Setting the -3dB corner too high affects the low-frequency response of the amplifier. Use capacitors with dielectrics that have low-voltage coefficients, such as aluminum electrolytic. Capacitors with high voltage coefficients, such as ceramics, can increase distortion at low frequencies.

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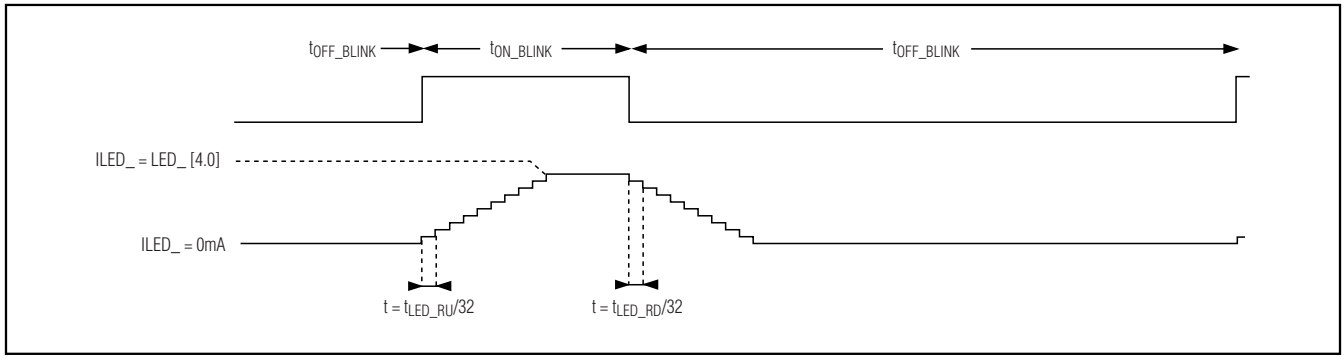

Figure 6. Combining Ramp Function and Blink Timer (Tables 10 and 11)

LDO1 and LDO2

The linear regulators are designed for low dropout and low quiescent current to maximize battery life. Both LDOs are controlled through the I²C interface, minimizing the number of control lines to the MAX8821. Each LDO has an individual control register (LDO1_CNTL and LDO2_CNTL, Tables 13 and 14). The I²C interface controls the output voltages, and the enable/disable state for both LDO1 and LDO2.

Thermal Shutdown

The MAX8821 includes a thermal-limit circuit that shuts down the IC at a junction temperature of approximately +160°C. The IC turns on after it cools by approximately 20°C.

Shutdown Mode

The MAX8821 can be put into two different shutdown modes. The first shutdown mode is achieved by driving V_{DD} low. In this mode, the I²C interface becomes disabled. The second shutdown is a lower power mode. To enter the low-power mode, disable LED_, audio amplifier, and LDOs through I²C. In lower power mode, the I²C interface is still active.

I²C Interface

The I²C serial interface consists of a serial-data line (SDA) and a serial-clock line (SCL). Standard I²C write-byte commands are used. Figure 8 shows a timing diagram for the I²C protocol. The MAX8821 is a slave-only device, relying upon a master to generate a clock signal. The master (typically a microprocessor) initiates data transfer on the bus and generates SCL to permit data transfer. A master device communicates to the MAX8821 by transmitting the proper 8-bit address followed by the 8-bit control byte. Each transmit sequence is framed by a START (A) condition and a STOP (L) condition. Each word transmitted over the bus is 8 bits long and is always followed by an acknowledge clock pulse (K).

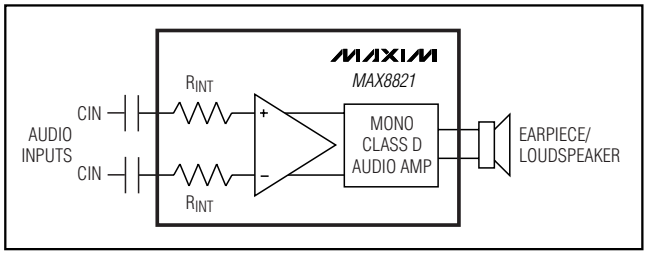

Figure 7. Optional Input Capacitors

Both SCL and SDA remain high when the interface is not busy. A master signals the beginning of a transmission with a START (A) condition by transitioning SDA from high to low while SCL is high. When the master has finished communicating with the slave, the master issues a STOP (L) condition by transitioning SDA from low to high while SCL is high. The bus is then free for another transmission. One data bit is transferred during each clock pulse. The data on SDA must remain stable while SCL is high.

Register Reset

The I²C register is reset back to the default value when either $V_{IN_}$ drops below the UVLO threshold or V_{DD} is driven low.

I²C Registers and Control

I²C Address

The MAX8821 acts as a slave transmitter/receiver. The slave address of the MAX8821 is preset to 1001110X, where "X" is the R/W bit. The address 0x9C is designated for write operations and 0x9D for read operations.

Use Table 1 as a register map to reference the control bits found in Tables 2–16.

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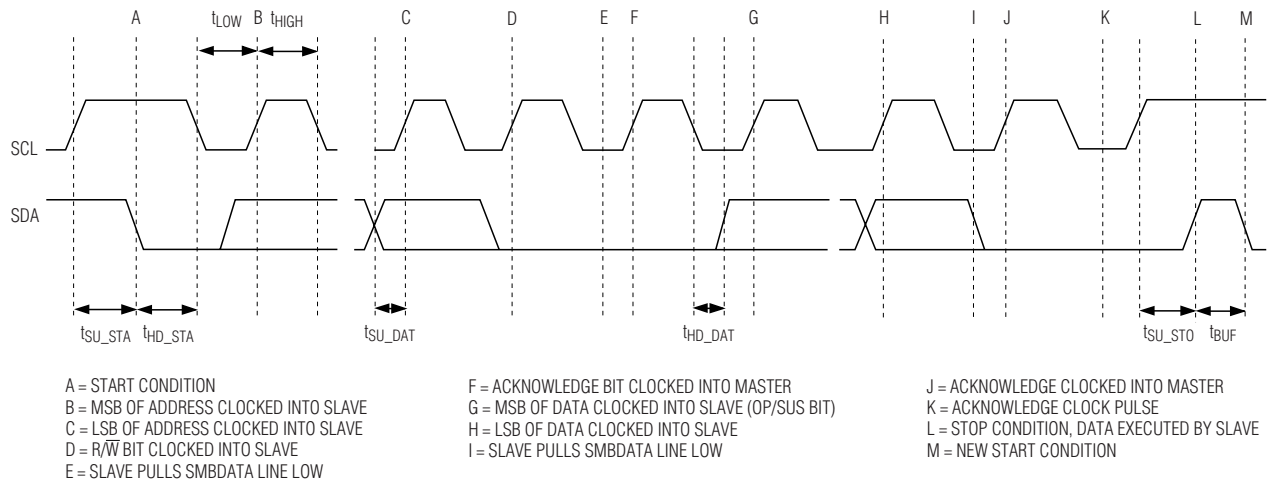

Figure 8. I2C Timing Diagram

Table 1. Register Map

NAME	GROUP ADDRESS (hexadecimal)	TABLE	TYPE	DESCRIPTION
LED1_CNTL	00	2	R/W	LED1 current regulator control
LED2_CNTL	01	3	R/W	LED2 current regulator control
LED3_CNTL	02	4	R/W	LED3 current regulator control
LED4_CNTL	03	5	R/W	LED4 current regulator control
LED5_CNTL	04	6	R/W	LED5 current regulator control
LED6_CNTL	05	7	R/W	LED6 current regulator control
RAMP1_CNTL	06	8	R/W	LED1 and LED2 ramp control
RAMP2_CNTL	07	9	R/W	LED3 and LED4 ramp control
RAMP3_CNTL	08	10	R/W	LED5 and LED6 ramp control
BLINK_CNTL	09	11	R/W	LED5 and LED6 blink control
LED_EN	0A	12	R/W	LED1–LED6 enable control
LDO1_CNTL	0B	13	R/W	LDO1 control
LDO2_CNTL	0C	14	R/W	LDO2 control
AUDIO_CNTL	0D	15	R/W	Audio amplifier, control clock, and frequency
PUMP_CNTL	0E	16	R/W	Charge-pump control setting and temperature derating enable/disable

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Table 2. LED1_CNTL (Address 0x00)

BIT	NAME	CODE	DESCRIPTION
B7, B6	N/A, do not use.		
B5	LED1_RP_EN	***0*** 1	***LED1 ramp-up/down disabled.*** LED1 ramp-up/down enabled.
B4–B0	LED1[4:0]	***00000***	***0.1mA***
		00001	0.2mA
		00010	0.3mA
		00011	0.4mA
		00100	0.5mA
		00101	0.6mA
		00110	0.7mA
		00111	0.8mA
		01000	1.0mA
		01001	1.2mA
		01010	1.4mA
		01011	1.6mA
		01100	2.0mA
		01101	2.4mA
		01110	2.8mA
		01111	3.2mA
		10000	4.0mA
		10001	4.8mA
		10010	5.6mA
		10011	6.4mA
		10100	8.0mA
		10101	9.6mA
		10110	11.2mA
		10111	12.8mA
		11000	14.4mA
		11001	16.0mA
		11010	17.6mA
		11011	19.2mA
		11100	20.8mA
		11101	22.4mA
		11110	24.0mA
		11111	25.6mA

Note: *Defaults in bold italics.*

Table 3. LED2_CNTL (Address 0x01)

BIT	NAME	CODE	DESCRIPTION
B7, B6	N/A, do not use.		
B5	LED2_RP_EN	***0*** 1	***LED2 ramp-up/down disabled.*** LED2 ramp-up/down enabled.
B4–B0	LED2[4:0]	***00000***	***0.1mA***
		00001	0.2mA
		00010	0.3mA
		00011	0.4mA
		00100	0.5mA
		00101	0.6mA
		00110	0.7mA
		00111	0.8mA
		01000	1.0mA
		01001	1.2mA
		01010	1.4mA
		01011	1.6mA
		01100	2.0mA
		01101	2.4mA
		01110	2.8mA
		01111	3.2mA
		10000	4.0mA
		10001	4.8mA
		10010	5.6mA
		10011	6.4mA
		10100	8.0mA
		10101	9.6mA
		10110	11.2mA
		10111	12.8mA
		11000	14.4mA
		11001	16.0mA
		11010	17.6mA
		11011	19.2mA
		11100	20.8mA
		11101	22.4mA
		11110	24.0mA
		11111	25.6mA

Note: *Defaults in bold italics.*

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Table 4. LED3_CNTL (Address 0x02)

BIT	NAME	CODE	DESCRIPTION
B7, B6	N/A, do not use.		
B5	LED3_RP_EN	***0*** 1	***LED3 ramp-up/down disabled.*** LED3 ramp-up/down enabled.
B4–B0	LED3[4:0]	***00000***	***0.1mA***
		00001	0.2mA
		00010	0.3mA
		00011	0.4mA
		00100	0.5mA
		00101	0.6mA
		00110	0.7mA
		00111	0.8mA
		01000	1.0mA
		01001	1.2mA
		01010	1.4mA
		01011	1.6mA
		01100	2.0mA
		01101	2.4mA
		01110	2.8mA
		01111	3.2mA
		10000	4.0mA
		10001	4.8mA
		10010	5.6mA
		10011	6.4mA
		10100	8.0mA
		10101	9.6mA
		10110	11.2mA
		10111	12.8mA
		11000	14.4mA
		11001	16.0mA
		11010	17.6mA
		11011	19.2mA
		11100	20.8mA
		11101	22.4mA
		11110	24.0mA
		11111	25.6mA

Note: *Defaults in bold italics.*

Table 5. LED4_CNTL (Address 0x03)

BIT	NAME	CODE	DESCRIPTION
B7, B6	N/A, do not use.		
B5	LED4_RP_EN	***0*** 1	***LED4 ramp-up/down disabled.*** LED4 ramp-up/down enabled.
B4–B0	LED4[4:0]	***00000***	***0.1mA***
		00001	0.2mA
		00010	0.3mA
		00011	0.4mA
		00100	0.5mA
		00101	0.6mA
		00110	0.7mA
		00111	0.8mA
		01000	1.0mA
		01001	1.2mA
		01010	1.4mA
		01011	1.6mA
		01100	2.0mA
		01101	2.4mA
		01110	2.8mA
		01111	3.2mA
		10000	4.0mA
		10001	4.8mA
		10010	5.6mA
		10011	6.4mA
		10100	8.0mA
		10101	9.6mA
		10110	11.2mA
		10111	12.8mA
		11000	14.4mA
		11001	16.0mA
		11010	17.6mA
		11011	19.2mA
		11100	20.8mA
		11101	22.4mA
		11110	24.0mA
		11111	25.6mA

Note: *Defaults in bold italics.*

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Table 6. LED5_CNTL (Address 0x04)

BIT	NAME	CODE	DESCRIPTION
B7, B6	N/A, do not use.		
B5	LED5_RP_EN	***0*** 1	***LED5 ramp-up/down disabled.*** LED5 ramp-up/down enabled.
B4–B0	LED5[4:0]	***00000***	***0.1mA***
		00001	0.2mA
		00010	0.3mA
		00011	0.4mA
		00100	0.5mA
		00101	0.6mA
		00110	0.7mA
		00111	0.8mA
		01000	1.0mA
		01001	1.2mA
		01010	1.4mA
		01011	1.6mA
		01100	2.0mA
		01101	2.4mA
		01110	2.8mA
		01111	3.2mA
		10000	4.0mA
		10001	4.8mA
		10010	5.6mA
		10011	6.4mA
		10100	8.0mA
		10101	9.6mA
		10110	11.2mA
		10111	12.8mA
		11000	14.4mA
		11001	16.0mA
		11010	17.6mA
		11011	19.2mA
		11100	20.8mA
		11101	22.4mA
		11110	24.0mA
		11111	25.6mA

Note: *Defaults in bold italics.*

Table 7. LED6_CNTL (Address 0x05)

BIT	NAME	CODE	DESCRIPTION
B7, B6	N/A, do not use.		
B5	LED6_RP_EN	***0*** 1	***LED6 ramp-up/down disabled.*** LED6 ramp-up/down enabled.
B4–B0	LED6[4:0]	***00000***	***0.1mA***
		00001	0.2mA
		00010	0.3mA
		00011	0.4mA
		00100	0.5mA
		00101	0.6mA
		00110	0.7mA
		00111	0.8mA
		01000	1.0mA
		01001	1.2mA
		01010	1.4mA
		01011	1.6mA
		01100	2.0mA
		01101	2.4mA
		01110	2.8mA
		01111	3.2mA
		10000	4.0mA
		10001	4.8mA
		10010	5.6mA
		10011	6.4mA
		10100	8.0mA
		10101	9.6mA
		10110	11.2mA
		10111	12.8mA
		11000	14.4mA
		11001	16.0mA
		11010	17.6mA
		11011	19.2mA
		11100	20.8mA
		11101	22.4mA
		11110	24.0mA
		11111	25.6mA

Note: *Defaults in bold italics.*

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Table 8. RAMP1_CNTL (Address 0x06)

BIT	NAME	DESCRIPTION	CODE	RAMP TIME (t_{RAMP}) (ms)
B7, B6	LED1_RU[1:0]	LED1 ramp-up control	***00***	***2^{18} x T_{QPCLK}***
B5, B4	LED1_RD[1:0]	LED1 ramp-down control	01	2^{19} x T_{QPCLK}
B3, B2	LED2_RU[1:0]	LED2 ramp-up control	10	2^{20} x T_{QPCLK}
B1, B0	LED2_RD[1:0]	LED2 ramp-down control	11	2^{21} x T_{QPCLK}

Notes: *T_{QPCLK} = 1 / f_{SW}; defaults in bold italics.*

Table 9. RAMP2_CNTL (Address 0x07)

BIT	NAME	DESCRIPTION	CODE	RAMP TIME (t_{RAMP}) (ms)
B7, B6	LED3_RU[1:0]	LED3 ramp-up control	***00***	***2^{18} x T_{QPCLK}***
B5, B4	LED3_RD[1:0]	LED3 ramp-down control	01	2^{19} x T_{QPCLK}
B3, B2	LED4_RU[1:0]	LED4 ramp-up control	10	2^{20} x T_{QPCLK}
B1, B0	LED4_RD[1:0]	LED4 ramp-down control	11	2^{21} x T_{QPCLK}

Notes: *T_{QPCLK} = 1 / f_{SW}; defaults in bold italics.*

Table 10. RAMP3_CNTL (Address 0x08)

BIT	NAME	DESCRIPTION	CODE	RAMP TIME (t_{RAMP}) (ms)
B7, B6	LED5_RU[1:0]	LED5 ramp-up control	***00***	***2^{18} x T_{QPCLK}***
B5, B4	LED5_RD[1:0]	LED5 ramp-down control	01	2^{19} x T_{QPCLK}
B3, B2	LED6_RU[1:0]	LED6 ramp-up control	10	2^{20} x T_{QPCLK}
B1, B0	LED6_RD[1:0]	LED6 ramp-down control	11	2^{21} x T_{QPCLK}

Notes: *T_{QPCLK} = 1 / f_{SW}; defaults in bold italics.*

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Table 11. BLINK_CNTL (Address 0x09)

BIT	NAME	CODE	BLINK TIME
B7, B6	LED5_OFF_BLINK	***00***	***2^{19} x T_{QPCLK}***
		01	2^{20} x T_{QPCLK}
		10	2^{21} x T_{QPCLK}
		11	2^{22} x T_{QPCLK}
B5, B4	LED5_ON_BLINK	***00***	***2^{16} x T_{QPCLK}***
		01	2^{17} x T_{QPCLK}
		10	2^{18} x T_{QPCLK}
		11	2^{19} x T_{QPCLK}
B3, B2	LED6_OFF_BLINK	***00***	***2^{19} x T_{QPCLK}***
		01	2^{20} x T_{QPCLK}
		10	2^{21} x T_{QPCLK}
		11	2^{22} x T_{QPCLK}
B1, B0	LED6_ON_BLINK	***00***	***2^{16} x T_{QPCLK}***
		01	2^{17} x T_{QPCLK}
		10	2^{18} x T_{QPCLK}
		11	2^{19} x T_{QPCLK}

Notes: *T_{QPCLK} = 1 / f_{SW}; defaults in bold italics.*

Table 12. LED_EN (Address 0xA)

BIT	NAME	CODE	DESCRIPTION
B7	LED1_EN	***0***	***LED current source is disabled.***
B6	LED2_EN		
B5	LED3_EN	1	LED current source is enabled.
B4	LED4_EN		
B3, B2	LED5_EN[1:0]	***00***	***LED current source is disabled.***
		01	LED current source is enabled.
B1, B0	LED6_EN[1:0]	10	LED current source controlled by blink timer.
		11	N/A, do not use.

Note: *Defaults in bold italics.*

Table 13. LDO1_CNTL (Address 0x0B)

BIT	NAME	CODE	DESCRIPTION
B7, B6	N/A, do not use.		
B5	LDO1_EN	***0***	***LDO1 is disabled.***
		1	LDO1 is enabled.
B4	LDO1_PD	***0***	***Active pulldown enabled during OFF condition.***
		1	Active pulldown disabled during OFF condition.
B3–B0	LDO1[3:0]	***0000***	***1.2V***
		0001	1.3V
		0010	1.5V
		0011	1.6V
		0100	1.8V
		0101	1.9V
		0110	2.0V
		0111	2.3V
		1000	2.5V
		1001	2.6V
		1010	2.7V
		1011	2.8V
		1100	2.9V
		1101	3.0V
		1110	3.1V
		1111	3.2V

Note: *Defaults in bold italics.*

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Table 14. LDO2_CNTL (Address 0x0C)

BIT	NAME	CODE	DESCRIPTION
B7, B6	N/A, do not use.		
B5	LDO2_EN	***0***	***LDO2 is disabled.***
		1	LDO2 is enabled.
B4	LDO2_PD	***0***	***Active pulldown enabled during OFF condition.***
		1	Active pulldown disabled during OFF condition.
B3–B0	LDO2[3:0]	***0000***	***1.5V***
		0001	1.6V
		0010	1.8V
		0011	2.0V
		0100	2.2V
		0101	2.3V
		0110	2.4V
		0111	2.5V
		1000	2.6V
		1001	2.7V
		1010	2.8V
		1011	2.9V
		1100	3.0V
		1101	3.1V
		1110	3.2V
		1111	3.3V

Note: *Defaults in bold italics.*

Table 15. AUDIO_CNTL (Address 0x0D)

BIT	NAME	CODE	DESCRIPTION
B7	SYNC	***0***	***Audio amplifier and charge-pump clocks are not synchronized.***
		1	Audio amplifier and charge-pump clocks are synchronized. Charge pump oscillator clock = audio clock / 2.
B6, B5	CLK_CNTL[1:0]	***00***	***Oscillator frequency 1100kHz, fixed-frequency mode.***
		01	Oscillator frequency 1400kHz, fixed-frequency mode.
		10	Oscillator frequency 1250kHz, spread-spectrum mode.
		11	Reserved for future use.
B4	AMP_EN	***0***	***Class D amplifier is disabled.***
		1	Class D amplifier is enabled.
B3–B0	AUDIO_GAIN[3:0]	***0000***	***-3dB***
		0001	0dB
		0010	3dB
		0011	6dB
		0100	9dB
		0101	12dB
		0110	15dB
		0111	18dB
		1000	21dB
		1001	24dB
		1010	N/A, do not use.
		1011	N/A, do not use.
		1100	N/A, do not use.
		1101	N/A, do not use.
		1110	N/A, do not use.
		1111	N/A, do not use.

Note: *Defaults in bold italics.*

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Table 16. PUMP_CNTL (Address 0x0E)

BIT	NAME	CODE	DESCRIPTION
B7–B3	N/A, do not use		
B2	TEMP_DR	***0***	***Temperature derating disabled.***
		1	Temperature derating enabled.
B1, B0	PUMP_CNTL [1:0]	***00***	***Charge pump automatically changes between 1x/1.5x mode.***
		01	Charge pump is forced into 1.5x mode regardless of input voltage.
		10	Charge pump is forced into 1.5x mode regardless of input voltage when audio amplifier is enabled. If the amplifier is not enabled, the charge pump automatically switches between 1x mode and 1.5x mode.
		11	N/A, do not use.

Note: *Defaults in bold italics.*

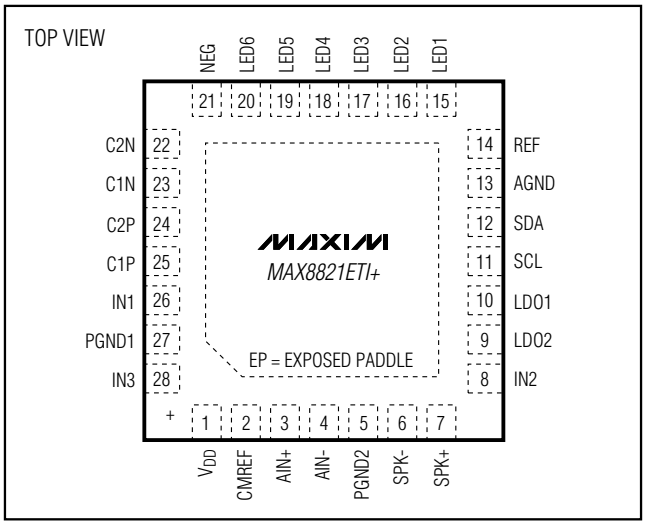
Applications Information

PCB Layout

PCB layout is essential for optimizing performance. Use large traces for the power-supply inputs and amplifier outputs to minimize losses due to parasitic trace resistance and to route heat away from the device. To avoid potential noise to the differential input audio signal and differential output audio signal, route the negative and positive traces in parallel. Also, avoid placing any RF or high-speed data signals in parallel to the audio signals. In some applications, such as GSM, extra noise reduction may be needed. To reduce the risk of noise, place 16pF ceramic capacitors from AIN+ to AGND, AIN- to AGND, OUT+ to AGND, OUT- to AGND, OUT+ to OUT-, and AIN+ to AIN-.

Proper grounding improves audio performance and prevents any digital switching noise from coupling into the audio signal. The Thin QFN package features an exposed thermal paddle on its undersides. This paddle lowers the thermal resistance of the package by providing a direct-heat conduction path from the die to the PCB. Connect the exposed paddle to AGND directly under the IC. Refer to the MAX8821 Evaluation Kit for an example of a PCB layout.

Pin Configuration



Chip Information

PROCESS: BiCMOS

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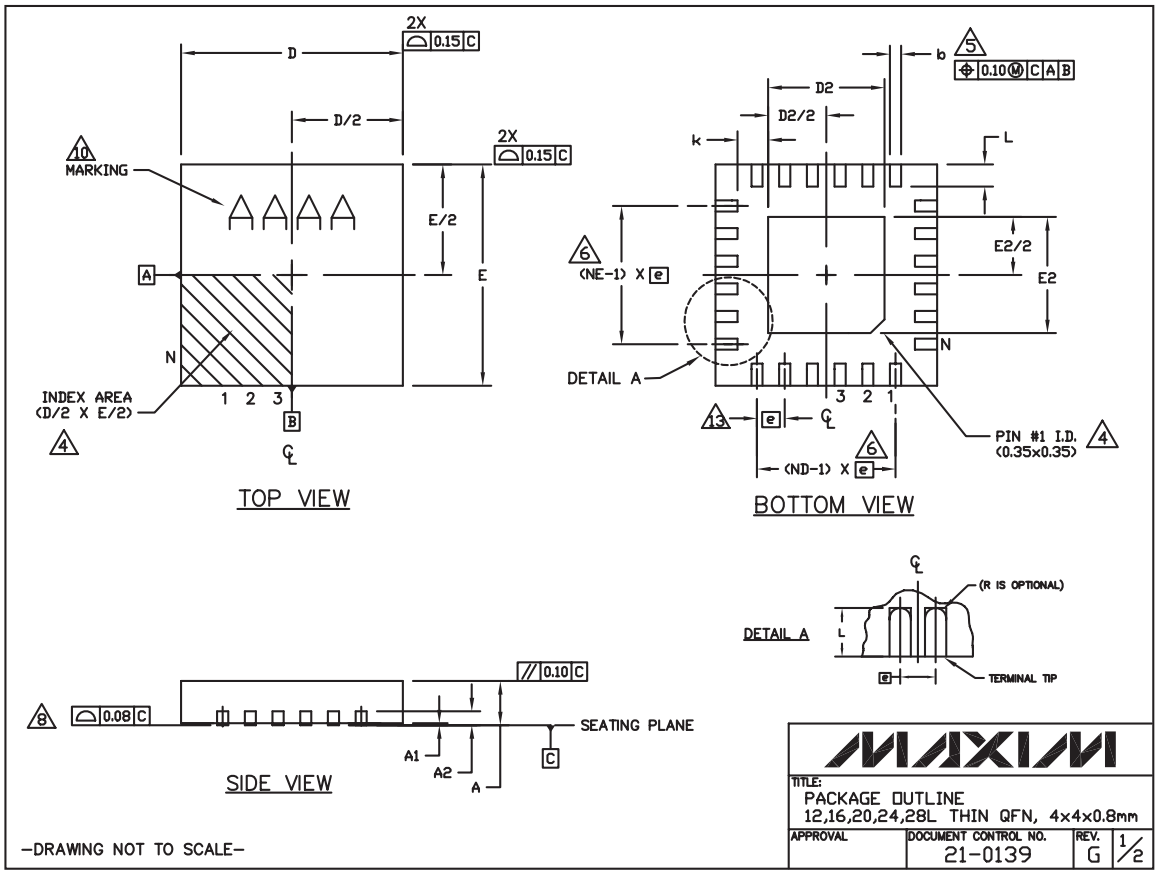
White LED Charge Pump with Mono Class D Audio Amp and Dual LDO

Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)



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Package Information (continued)

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information go to **www.maxim-ic.com/packages**.)

COMMON DIMENSIONS

PKG	12L 4x4			16L 4x4			20L 4x4			24L 4x4			28L 4x4		
REF.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80
A1	0.0	0.02	0.05	0.0	0.02	0.05	0.0	0.02	0.05	0.0	0.02	0.05	0.0	0.02	0.05
A2	0.20 REF			0.20 REF			0.20 REF			0.20 REF			0.20 REF		
b	0.25	0.30	0.35	0.25	0.30	0.35	0.20	0.25	0.30	0.18	0.23	0.30	0.15	0.20	0.25
D	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10
E	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10	3.90	4.00	4.10
e	0.80 BSC.			0.65 BSC.			0.50 BSC.			0.50 BSC.			0.40 BSC.		
k	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-
L	0.45	0.55	0.65	0.45	0.55	0.65	0.45	0.55	0.65	0.30	0.40	0.50	0.30	0.40	0.50
N	12			16			20			24			28		
ND	3			4			5			6			7		
NE	3			4			5			6			7		
Jedec Var.	WGGB			WGGC			WGGD-1			WGGD-2			WGGE		

EXPOSED PAD VARIATIONS

PKG. CODES	D2			E2		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
T1244-3	1.95	2.10	2.25	1.95	2.10	2.25
T1244-4	1.95	2.10	2.25	1.95	2.10	2.25
T1644-3	1.95	2.10	2.25	1.95	2.10	2.25
T1644-4	1.95	2.10	2.25	1.95	2.10	2.25
T2044-2	1.95	2.10	2.25	1.95	2.10	2.25
T2044-3	1.95	2.10	2.25	1.95	2.10	2.25
T2444-2	1.95	2.10	2.25	1.95	2.10	2.25
T2444-3	2.45	2.60	2.63	2.45	2.60	2.63
T2444-4	2.45	2.60	2.63	2.45	2.60	2.63
T2844-1	2.50	2.60	2.70	2.50	2.60	2.70

NOTES:
1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25mm AND 0.30mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220, EXCEPT FOR T2444-3, T2444-4 AND T2844-1.
10. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
11. COPLANARITY SHALL NOT EXCEED 0.08mm.
12. WARPAGE SHALL NOT EXCEED 0.10mm.
13. LEAD CENTERLINES TO BE AT TRUE POSITION AS DEFINED BY BASIC DIMENSION 'e', ±0.05.
14. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.
15. ALL DIMENSIONS ARE THE SAME FOR LEADED (-) & PbFREE (+) PACKAGE CODES.

-DRAWING NOT TO SCALE-

MAXIM

TITLE: PACKAGE OUTLINE 12,16,20,24,28L THIN QFN, 4x4x0.8mm

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