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REVISIONS

LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Add device types 03 and 04. Editorial changes throughout.	94-11-15	M. A. Frye
B	Changes in accordance with NOR 5962-R106-95.	95-04-12	M. A. Frye
C	Change t_{LZ}, t_{HZ}, and t_{TD} for device type 03 in table I. Editorial changes throughout. -rrp	98-10-05	R. MONNIN

THE ORIGINAL FIRST PAGE OF THIS DRAWING HAS BEEN REPLACED.

REV																			
SHEET																			
REV	C	C	C																
SHEET	15	16	17																

REV STATUS	REV	C	C	C	C	C	C	C	C	C	C	C	C	C
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

PREPARED BY
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Michael A. Frye

DRAWING APPROVAL DATE
91-08-01

REVISION LEVEL
C

DEFENSE SUPPLY CENTER COLUMBUS
COLUMBUS, OHIO 43216

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

MICROCIRCUIT, LINEAR, LINE DRIVER, QUAD DIFFERENTIAL , MONOLITHIC SILICON

SIZE	CAGE CODE	
A	**67268**	**5962-90765**

SHEET 1 OF 17

DSCC FORM 2233
APR 97

5962-E525-98

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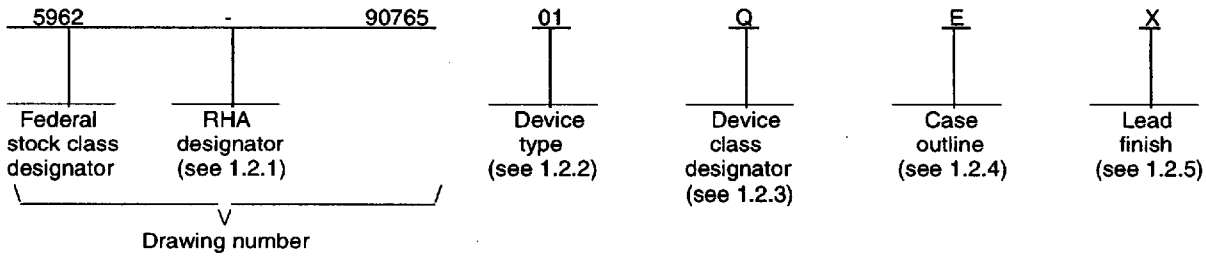
1. SCOPE

1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	96F172	RS-485 comparable quad differential line driver
02	96F174	RS-485 comparable quad differential line driver
03	55LBC172	RS-485 comparable quad differential line driver, low power
04	55LBC174	RS-485 comparable quad differential line driver, low power

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
E	GDIP1-T16 or CDIP2-T16	16	Dual-in-line
F	GDFP2-F16 or CDFP3-F16	16	Flat pack
2	CQCC1-N20	20	Square leadless chip carrier

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

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1.3 Absolute maximum ratings. 1/

Supply voltage (V_{CC})	7 V dc
Enable input voltage	5.5 V dc
Storage temperature range	-65°C to +150°C
Lead temperature (soldering, 60 seconds)	+300°C
Junction temperature (T_J):	
Device type 01, 02	+175°C
Device type 03, 04	+150°C
Power dissipation (P_D), T_A = +25°C 2/, device types 01, 02:	
Case E	1800 mW
Case F	1000 mW
Case 2	2000 mW
Power dissipation (P_D), T_A = +25°C 3/, device types 03, 04:	
Case E, 2	1375 mW
Case F	1000 mW
Thermal resistance, junction-to-case (θ_{JC})	See MIL-STD-1835
Thermal resistance, junction-to-ambient (θ_{JA}):	
Case E, device types 01, 02	80°C/W
Case E, device types 03, 04	85°C/W
Case F	140°C/W
Case 2	75°C/W

1.4 Recommended operating conditions.

Operating supply voltage range (V_{CC}):	
Device types 01, 02	4.5 V dc to 5.5 V dc
Device types 03, 04	4.75 V dc to 5.25 V dc
Ambient operating temperature range (T_A)	-55°C to +125°C
Common mode output voltage range (V_{OC})	-7 V dc to +12 V dc
High output current (I_{OH})	-60 mA
Low output current (I_{OL})	60 mA

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

DEPARTMENT OF DEFENSE

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

2/ Above T_A = +25°C, derate at a factor of 12.5 mW/°C for case E, 7.1 mW/°C for case F and 13.4 mW/°C for case 2.

3/ Above T_A = +25°C, derate at a factor of 11 mW/°C for cases E and 2, 8 mW/°C for case F.

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STANDARDS

DEPARTMENT OF DEFENSE

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-973 - Configuration Management.
MIL-STD-1835 - Interface Standard For Microcircuit Case Outlines.

HANDBOOKS

DEPARTMENT OF DEFENSE

MIL-HDBK-103 - List of Standard Microcircuit Drawings (SMD's).
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, and handbooks are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with 1.2.4 herein.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.3 Truth table(s). The truth table(s) shall be as specified on figure 2.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full ambient operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-HDBK-103. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

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TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Low level input voltage	V_{IL}	V_{CC} = 5.5 V	1	01, 02		0.8	V
			2, 3			0.7	
		V_{CC} = 5.25 V	1, 2, 3			0.8	
High level input voltage	V_{IH}	V_{CC} = 5.5 V	1, 2, 3	01, 02	2		V
		V_{CC} = 5.25 V		03, 04	2		
Input clamp voltage	V_{IC}	I_I = -18 mA, V_{CC} = 5.5 V	1, 2, 3	01, 02	-1.5		V
		I_I = -18 mA, V_{CC} = 5.25 V		03, 04	-1.5		
Differential output voltage	V_{OD1}	I_O = 0 mA, V_{CC} = 5.5 V	1, 2, 3	01, 02		6	V
	V_{OD2}	R_L = 54 Ω, V_{CC} = 4.5 V 2/	1, 2	01, 02	1.5		
			3		1.2		
		R_L = 54 Ω, V_{CC} = 4.75 V 2/	1, 2, 3	03, 04	1.1	5.0	
		R_L = 1000 Ω, V_{CC} = 4.5 V 2/	1, 2, 3	01, 02	2.0		
		R_L = 60 Ω, V_{CC} = 4.75 V 2/		03, 04	1.1	5.0	
Change in magnitude of V_{OD2} 3/	Delta V_{OD2}	R_L = 54 Ω, V_{CC} = 4.5 V	1, 2	01, 02	-200	200	mV
		R_L = 1000 Ω, V_{CC} = 4.5 V 4/	3		-400	400	
		R_L = 54 Ω, V_{CC} = 4.75 V	1, 2, 3	03, 04	-200	200	
Common mode output voltage	V_{OC}	R_L = 54 Ω, V_{CC} = 5.5 V	1, 2, 3	01, 02		3	V
		R_L = 1000 Ω, V_{CC} = 5.5 V				3	
		R_L = 54 Ω, V_{CC} = 5.25 V		03, 04	-1	3	

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ -55°C ≤ T_A ≤+125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Change in magnitude of 3/ V_{OC}	Delta V_{OC}	R_L = 54 Ω, V_{CC} = 4.5 V	1, 2, 3	01, 02	-200	200	mV
		R_L = 1000 Ω, V_{CC} = 4.5 V			-200	200	
		R_L = 54 Ω, V_{CC} = 4.75 V		03, 04	-200	200	
Output current with power off	I_O	V_O = -7 V to 12 V, V_{CC} = 0 V	1, 2, 3	01, 02	-50	50	µA
				01, 02	-100	100	
High impedance state output current	I_{OZ}	V_O = -7 V to 12 V, V_{CC} = 5.5 V, outputs disabled	1, 2, 3	01, 02	-50	50	µA
		V_O = -7 V to 12 V, V_{CC} = 5.25 V, outputs disabled		03, 04	-100	100	
Short circuit output current 5/	I_{OS}	V_O = -7 V, V_{CC} = 5.5 V	1, 2, 3	01, 02	-250		mA
		V_O = -7 V, V_{CC} = 5.25 V		03, 04	-250		
		V_O = 12 V, V_{CC} = 5.5 V		01, 02		250	
		V_O = 12 V, V_{CC} = 5.25 V		03, 04		250	
		V_O = 0 V, V_{CC} = 5.5 V		01, 02	-150		
		V_O = V_{CC} = 5.5 V				150	
High input current	I_{IH}	V_I = 2.4 V, V_{CC} = 5.5 V	1, 2, 3	01, 02		20	µA
		V_I = 2.4 V, V_{CC} = 5.25 V		03, 04		-100	
Low input current	I_{IL}	V_I = 0.4 V, V_{CC} = 5.5 V	1, 2, 3	01, 02	-50		µA
		V_I = 0.4 V, V_{CC} = 5.25 V		03, 04	-100		

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Supply current (all drivers)	I_{CC}	V_{CC} = 5.5 V, no load, outputs enabled	1, 2, 3	01, 02		50	mA
		V_{CC} = 5.25 V, no load, outputs enabled		03, 04		7	
		V_{CC} = 5.5 V, no load, outputs disabled		01, 02		30	
		V_{CC} = 5.25 V, no load, outputs disabled		03, 04		1.5	
Functional test	FT	See 4.4.1b	7, 8	All			
Propagation delay low to high level	t_{PLH}	R_L = 27 Ω, C_L = 15 pF, V_{CC} = 5 V, see figure 3	9	01, 02		16	ns
			10, 11			25	
Propagation delay high to low level	t_{PHL}	R_L = 27 Ω, C_L = 15 pF, V_{CC} = 5 V, see figure 3	9	01, 02		16	ns
			10, 11			25	
Output disable time from low level	t_{LZ}	R_L = 110 Ω, C_L = 50 pF, V_{CC} = 5 V, see figure 3	9	01, 02		25	ns
				03, 04		30	
			10, 11	01, 02		40	
				03		55	
				04		45	
Output disable time from high level	t_{HZ}	R_L = 110 Ω, C_L = 50 pF, V_{CC} = 5 V, see figure 3	9	01, 02		30	ns
				03		60	
				04		50	
			10, 11	01, 02		80	
				03		115	
				04		90	

See footnotes at end of table.

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TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ -55°C ≤ T_A ≤+125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Output to output delay time	t_{SKEW}	R_L = 60 Ω, V_{CC} = 5 V, see figure 3	9	01, 02		4	ns
			10, 11			10	
Output enable time to low level	t_{ZL}	R_L = 110 Ω, C_L = 50 pF, V_{CC} = 5 V, see figure 3	9	01, 02		40	ns
				03, 04		30	
			10, 11	01, 02		100	
				03, 04		40	
Output enable time to high level	t_{ZH}	R_L = 110 Ω, C_L = 50 pF, V_{CC} = 5 V, see figure 3	9	01, 02		32	ns
				03, 04		30	
			10, 11	01, 02		40	
				03, 04		40	
Differential output delay time	t_{DD}	R_L = 60 Ω, C_L = 15 pF, V_{CC} = 5 V, see figure 3	9	01, 02		22	ns
			10, 11			30	
		R_L = 54 Ω, C_L = 50 pF, V_{CC} = 5 V, see figure 3	9	03, 04	2	20	
			10, 11		2	40	
Differential output transition time	t_{TD}	R_L = 60 Ω, C_L = 15 pF, V_{CC} = 5 V, see figure 3	9	01, 02		22	ns
			10, 11			40	
		R_L = 54 Ω, C_L = 50 pF, V_{CC} = 5 V, see figure 3	9	03, 04	10	25	
			10, 11	03	4	60	
				04	4	40	

See footnotes at end of table.

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1/ All currents into device pins are positive; all currents out of the device pins are negative. All voltages are referenced to ground unless otherwise specified. Device types 01 and 03 has an active high and active low enable, common to all four drivers. Device types 02 and 04 has seperate active high enables for each driver pair.

2/ T_A = -55°C limit exceeds EIA standard RS-485 specification of 1.5 V maximum.

3/ Delta V_{OD2} and delta V_{OC} are the changes in magnitude of V_{OD2} and V_{OC} respectively, that occur when the input is changed from a high to a low level.

4/ T_A = -55°C limit exceeds EIA standard RS-485 specification ±200 mV maximum.

5/ Only one output at a time should be shorted, and the duration of the short circuit should not exceed one second.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DSCC-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-973.

3.9 Verification and review for device class M. For device class M, DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 53 (see MIL-PRF-38535, appendix A).

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Device types	01, 03		02, 04	
Case outlines	E and F	2	E and F	2
Terminal number	Terminal symbol			
1	1A	NC	1A	NC
2	1Y	1A	1Y	1A
3	1Z	1Y	1Z	1Y
4	E	1Z	E1, 2	1Z
5	2Z	E	2Z	E1, 2
6	2Y	NC	2Y	NC
7	2A	2Z	2A	2Z
8	GND	2Y	GND	2Y
9	3A	2A	3A	2A
10	3Y	GND	3Y	GND
11	3Z	NC	3Z	NC
12	$\overline{E}$	3A	E3, 4	3A
13	4Z	3Y	4Z	3Y
14	4Y	3Z	4Y	3Z
15	4A	$\overline{E}$	4A	E3, 4
16	V_{CC}	NC	V_{CC}	NC
17	----	4Z	----	4Z
18	----	4Y	----	4Y
19	----	4A	----	4A
20	----	V_{CC}	----	V_{CC}

NC = No connection

FIGURE 1. Terminal connections.

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Device types 01, 03

Input	Enables		Outputs	
A	E	$\overline{E}$	Y	Z
H	H	X	H	L
L	H	X	L	H
H	X	L	H	L
L	X	L	L	H
X	L	H	Z	Z

Device types 02, 04

Input	Enable	Outputs	
		Y	Z
H	H	H	L
L	H	L	H
X	L	Z	Z

H = High level
L = Low level
X = Don't care
Z = High impedance (off)

FIGURE 2. Truth table.

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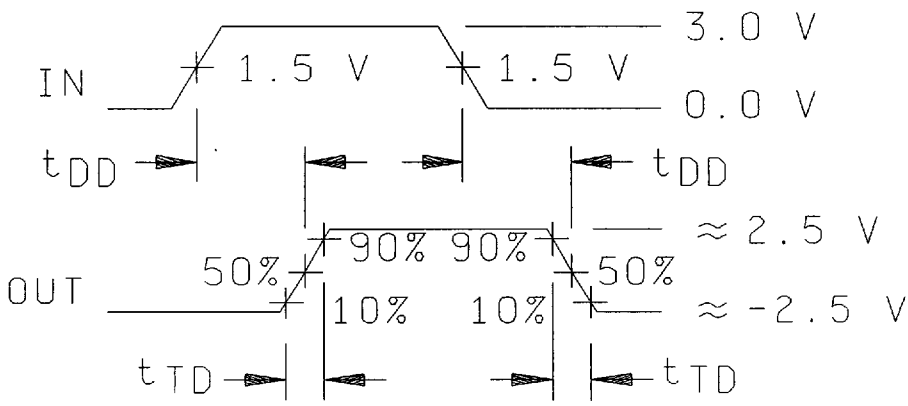
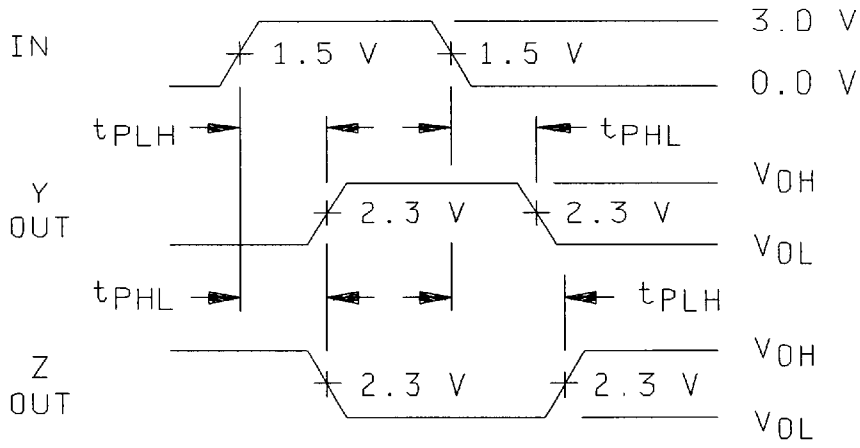


Differential output delay and transition times



Propagation delay times

FIGURE 3. Timing waveforms.

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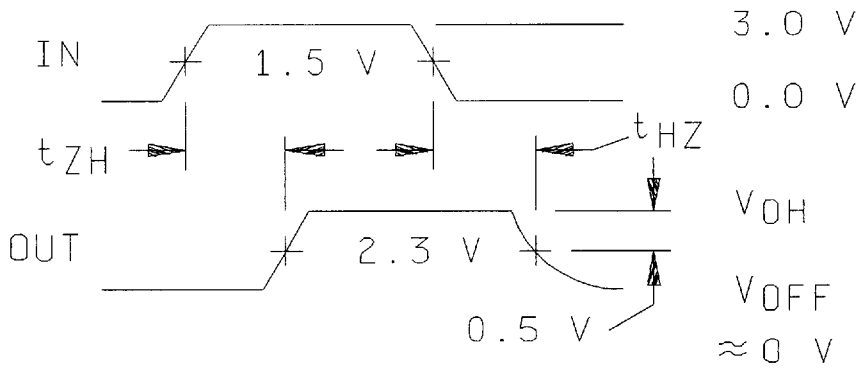
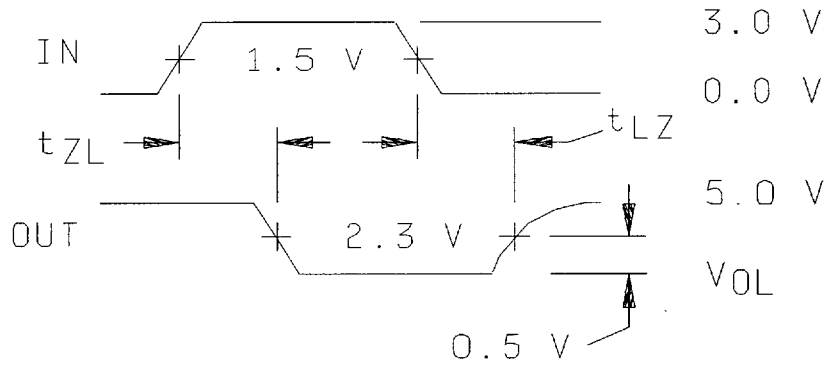


t_{ZH} and t_{HZ}



t_{ZL} and t_{LZ}

FIGURE 3. Timing waveforms - Continued.

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4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-PRF-38535 permits alternate in-line control testing. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

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TABLE II. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class M	Device class Q	Device class V
Interim electrical parameters (see 4.2)	1	----	1
Final electrical parameters (see 4.2)	1, 2, 3, 9 1/	1, 2, 3, 9 1/	1, 2, 3, 9 1/
Group A test requirements (see 4.4)	1, 2, 3, 7, 8, 9, 10, 11	1, 2, 3, 7, 8, 9, 10, 11	1, 2, 3, 7, 8, 9, 10, 11
Group C end-point electrical parameters (see 4.4)	1, 2, 3	1, 2, 3	1, 2, 3
Group D end-point electrical parameters (see 4.4)	1, 2, 3	1, 2, 3	1, 2, 3
Group E end-point electrical parameters (see 4.4)	----	----	----

1/ PDA applies to subgroup 1.

4.4.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. For device class M and Q, subgroups 7 and 8 tests shall be sufficient to verify the truth table.

c. Subgroups 4, 5, and 6 in table I, method 5005 of MIL-STD-883 shall be omitted.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition A, B, C or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

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4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table II herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table II herein.

c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform Defense Supply Center Columbus when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0525.

6.4 Comments. Comments on this drawing should be directed to DSCC-VA , Columbus, Ohio 43216-5000, or telephone (614) 692-0674.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

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6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DSCC-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

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STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 98-10-05

Approved sources of supply for SMD 5962-90765 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-9076501MEA	27014	DS96F172MJ/883
5962-9076501MFA	3/	DS96F172MW/883
5962-9076501M2A	27014	DS96F172ME/883
5962-9076501VEA	27014	DS96F172MJ-QMLV
5962-9076502MEA	27014	DS96F174MJ/883
5962-9076502MFA	27014	DS96F174MW/883
5962-9076502M2A	27014	DS96F174ME/883
5962-9076502VEA	27014	DS96F174MJ-QMLV

See footnotes at end of table.

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.

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Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-9076503QEA	01295	SNJ55LBC172J
5962-9076503QFA	01295	SNJ55LBC172W
5962-9076503Q2A	01295	SNJ55LBC172FK
5962-9076504QEA	01295	SNJ55LBC174J
5962-9076504QFA	01295	SNJ55LBC174W
5962-9076504Q2A	01295	SNJ55LBC174FK

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.
2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.
3/ Not available from an approved source of supply.

Vendor CAGE number	Vendor name and address
27014	National Semiconductor 2900 Semiconductor Drive P.O. Box 58090 Santa Clara, CA 95052-8090
01295	Texas Instruments Incorporated 13500 N. Central Expressway P.O. Box 655303 Dallas, TX 75265 Point of contact: I-20 at FM 1788 Midland, TX 79711-0448

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