

## Low Voltage Synchronous Buck Controller

The NCP1588 is a low cost PWM controller designed to operate from a 5 V or 12 V supply. This device is capable of producing an output voltage as low as 0.8 V. This device is capable of converting voltage from as low as 2.5 V. This 10-pin device provides an optimal level of integration to reduce size and cost of the power supply. The NCP1588 provides a 1.5 A gate driver design and an internally set 300 kHz oscillator. In addition to the 1.5 A gate drive capability, other efficiency enhancing features of the gate driver include adaptive non-overlap circuitry. The NCP1588 also incorporates an externally compensated error amplifier. Protection features include programmable short circuit protection and undervoltage lockout (UVLO).

### Features

- V<sub>CC</sub> Range from 4.5 to 13.2 V
- 300 kHz Internal Oscillator
- Boost Pin Operates to 26.4 V
- Voltage Mode PWM Control
- 0.8 V ±1.0% Internal Reference Voltage
- Adjustable Output Voltage
- Internal 1.5 A Gate Drivers
- 80% Max Duty Cycle
- Input Under Voltage Lockout
- Programmable Current Limit
- This is a Pb-Free Device

### Applications

- Graphics Cards
- Desktop Computers
- Servers / Networking
- DSP & FPGA Power Supply
- DC-DC Regulator Modules



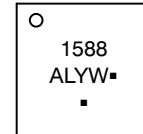
**ON Semiconductor®**

<http://onsemi.com>



**DFN10  
MT SUFFIX  
CASE 485C**

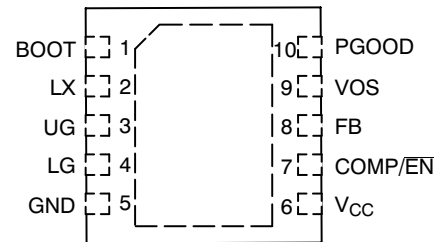
### MARKING DIAGRAM



1588 = Specific Device Code  
A = Assembly Location  
L = Wafer Lot  
Y = Year  
W = Work Week  
▪ = Pb-Free Device

(Note: Microdot may be in either location)

### PIN CONNECTIONS



(Top View)

### ORDERING INFORMATION

Device	Package	Shipping†
NCP1588MTR2G	DFN10 (Pb-Free)	3000/Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

# NCP1588

[查询"NCP1588MTR2G"供应商](#)

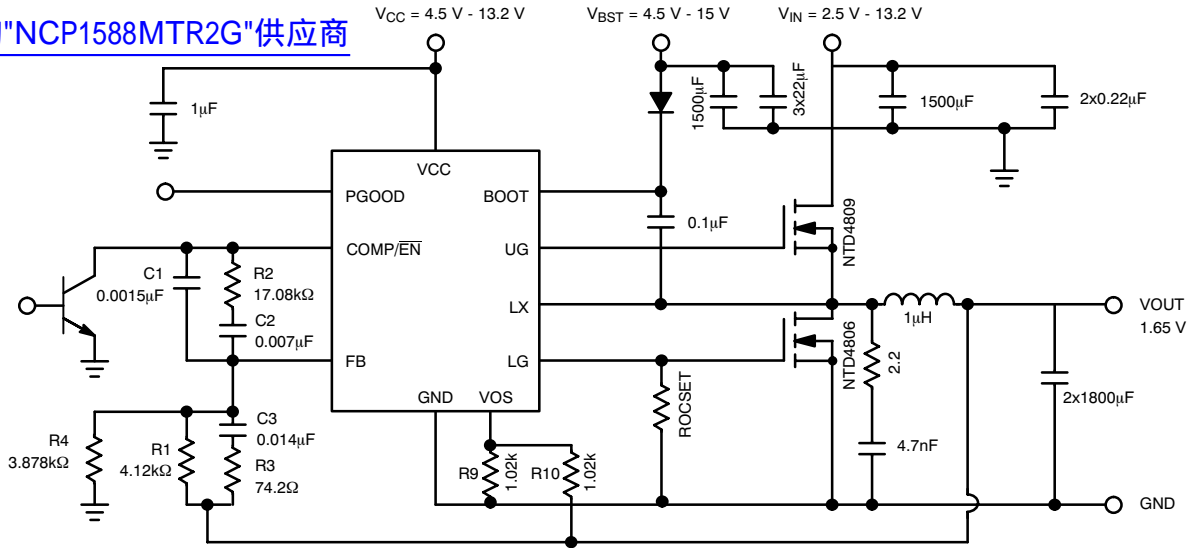


Figure 1. Typical Application Diagram

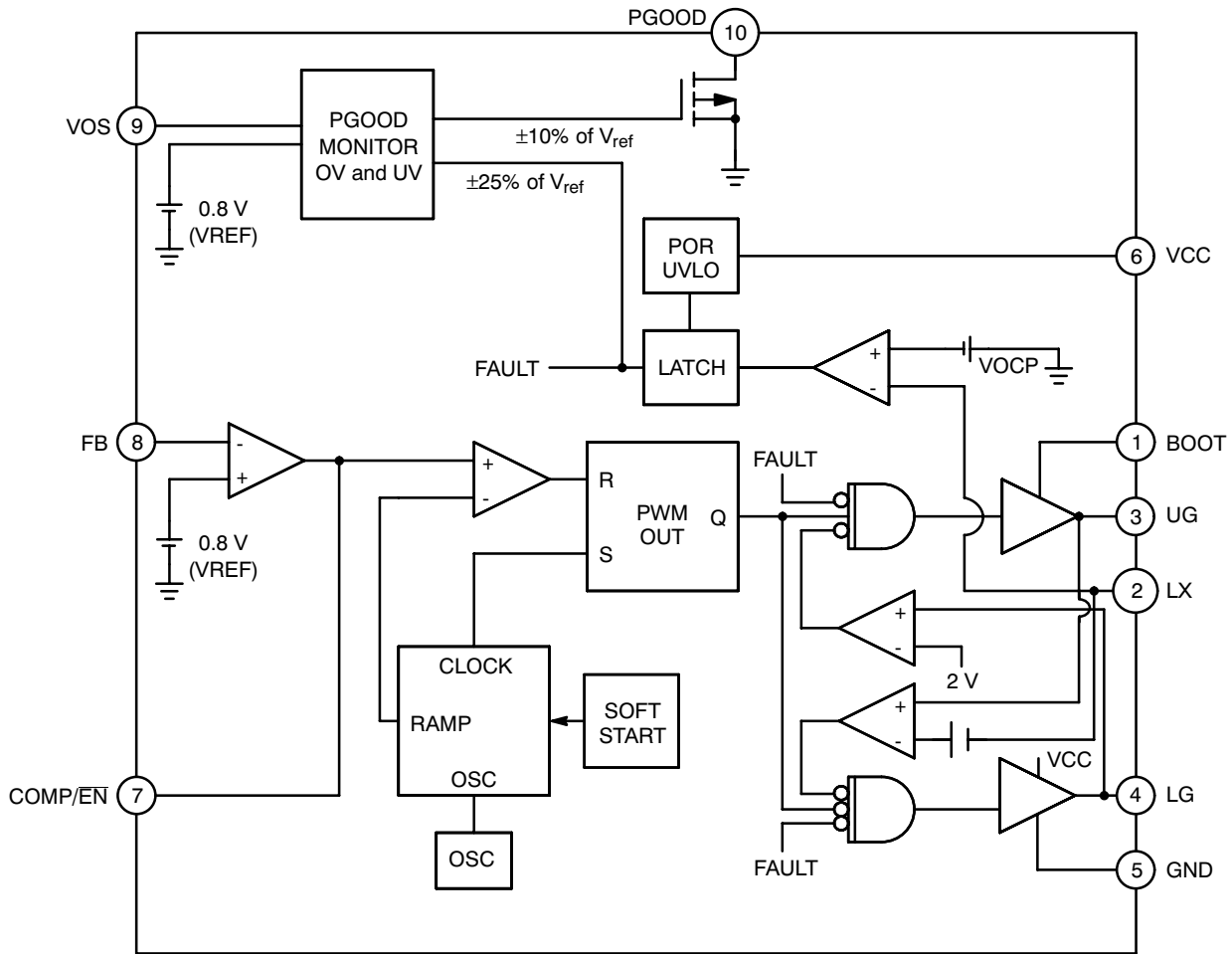


Figure 2. Detailed Block Diagram

# NCP1588

## PIN FUNCTION DESCRIPTION

Pin No.	Symbol	Description
1	BOOT	Supply rail for the floating top gate driver. To form a boost circuit, use an external diode to bring the desired input voltage to this pin (cathode connected to BOOT pin). Connect a capacitor ( $C_{BOOT}$ ) between this pin and the LX pin. Typical values for $C_{BOOT}$ range from 0.1 $\mu$ F to 1 $\mu$ F. Ensure that $C_{BOOT}$ is placed near the IC.
2	LX	Switch node pin. This is the reference for the floating top gate driver. Connect this pin to the source of the top MOSFET.
3	UG	Top gate MOSFET driver pin. Connect this pin to the gate of the top N-channel MOSFET.
4	LG	Bottom gate MOSFET driver pin. Connect this pin to the gate of the bottom N-channel MOSFET.
5	GND	IC ground reference. All control circuits are referenced to this pin.
6	$V_{CC}$	Supply rail for the internal circuitry. Operating supply range is 4.5 V to 13.2 V. Decouple with a 1 $\mu$ F capacitor to GND. Ensure that this decoupling capacitor is placed near the IC.
7	COMP/ $\overline{EN}$	Compensation Pin. This is the output of the error amplifier (EA) and the non-inverting input of the PWM comparator. Use this pin in conjunction with the FB pin to compensate the voltage-control feedback loop. Pull this pin low for disable.
8	FB	This pin is the inverting input to the error amplifier. Use this pin in conjunction with the COMP pin to compensate the voltage-control feedback loop. Connect this pin to the output resistor divider (if used) or directly to $V_{out}$ .
9	VOS	Offset voltage pin from $V_{out}$ .
10	PGOOD	Power Good output. Open drain type output that is flagged low if $\pm 10\%$ of $V_{out}$ .

## ABSOLUTE MAXIMUM RATINGS

Pin Name	Symbol	$V_{MAX}$	$V_{MIN}$
Main Supply Voltage Input	$V_{CC}$	15 V	-0.3 V
Bootstrap Supply Voltage Input	BOOT	30 V wrt/GND 38-40 V < 100 ns 15 V wrt/LX	-0.3 V
Switching Node (Bootstrap Supply Return)	LX	25 V 30 V for < 100 ns	-5 V
High-Side Driver Output (Top Gate)	UG	30 V wrt/GND 15 V wrt/LX 40 V for < 100 ns	-0.3 V wrt/LX
Low-Side Driver Output (Bottom Gate)	LG	$V_{CC} + 0.3$ V	-0.3 V -2 V < 100 ns
Feedback, VOS	FB, VOS	3.6 V	-0.3 V
COMP/ $\overline{EN}$	COMP/ $\overline{EN}$	3.6 V	-0.3 V
PGOOD	PGOOD	7 V	-0.3 V

## MAXIMUM RATINGS

Rating	Symbol	Value	Unit
Thermal Resistance, Junction-to-Ambient	$R_{\theta JA}$	165	$^{\circ}$ C/W
Thermal Resistance, Junction-to-Case	$R_{\theta JC}$	45	$^{\circ}$ C/W
NCP1588 Operating Junction Temperature Range	$T_J$	0 to 150	$^{\circ}$ C
NCP1588 Operating Ambient Temperature Range	$T_A$	0 to 70	$^{\circ}$ C
Storage Temperature Range	$T_{stg}$	-55 to +150	$^{\circ}$ C
Moisture Sensitivity Level	MSL	1	260

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

# NCP1588

**ELECTRICAL CHARACTERISTICS** (0°C < T<sub>A</sub> < 70°C, 0°C < T<sub>J</sub> < 125°C (NCP1588); 4.5 V < V<sub>CC</sub> < 13.2 V, 4.5 V < BOOT < 26.4 V, C<sub>UG</sub> = C<sub>LG</sub> = 1.0 nF (REF:NTD30N02), for min/max values unless otherwise noted.)

Characteristic	Conditions	Min	Typ	Max	Unit
Input Voltage Range		4.5		13.2	V
Boost Voltage Range	13.2 V wrt LX	4.5		26.4	V

## Supply Current

Quiescent Supply Current	V <sub>FB</sub> = 1.0 V, No Switching, V <sub>CC</sub> = 13.2 V		1.0	1.75	mA
Boost Quiescent Current	V <sub>FB</sub> = 1.0 V, No Switching		140		μA

## Undervoltage Lockout

UVLO threshold	V <sub>CC</sub> Rising Edge	3.8		4.0	V
UVLO hysteresis			0.37		V

## Switching Regulator

VFB Feedback Voltage, control loop in regulation	T <sub>A</sub> = 0 to 70°C	0.792	0.8	0.808	V
Oscillator Frequency	T <sub>A</sub> = 0 to 70°C	270	300	330	KHz
Ramp-Amplitude Voltage			1.1		V
Minimum Duty Cycle			0		%
Maximum Duty Cycle		70	75	80	%
LG minimum on time			500		ns

## Error Amplifier

Open loop dc gain		70	80		DB
Output source current	V <sub>fb</sub> < 0.8 V	2.0			mA
Output sink current	V <sub>fb</sub> > 0.8 V	2.0			mA
Input Offset Voltage		-2.0	0	2.0	mV
Input Bias Current			0.1	1.0	μA
Unity Gain Bandwidth		15			Mhz
Disable Threshold		0.3		0.5	V
Output Sink current during disable				100	μA

## Gate Drivers

Upper Gate source	V <sub>CC</sub> = 5 V, V <sub>UG</sub> - V <sub>LX</sub> = 2.5 V	1.5			A
Upper Gate sink			1.4		Ω
Lower Gate source		1.5			A
Lower Gate sink	V <sub>CC</sub> = 12 V		1.0		Ω
UG falling to LG rising delay	V <sub>CC</sub> = 12 V, UG-LX < 2.0 V, LG > 2.0 V		30	90	ns
LG falling to UG rising delay	V <sub>CC</sub> = 12 V, LG < 2.0 V, UG > 2.0 V		30	60	ns

## Soft-Start

Soft-Start time		3.0		7.0	ms
-----------------	--	-----	--	-----	----

## Power Good

Output Saturation Voltage	IPG = 4 mA, V <sub>CC</sub> = 12 Vdc			0.4	V
OVP threshold to part disable			1.0		V
UVP threshold to part disable			0.6		V
OVP threshold to PGOOD output low			0.88		V
UVP threshold to PGOOD output low			0.72		V

## Overcurrent Protection

OC Current source	Sourced from LG pin, before SS		10		μA
-------------------	--------------------------------	--	----	--	----

[查询"NCP1588MTR2G"供应商](#)

TYPICAL CHARACTERISTICS

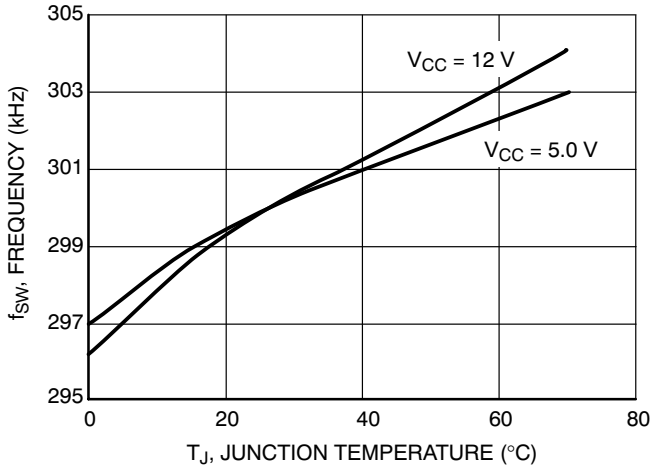


Figure 3. Oscillator Frequency ( $f_{sw}$ ) vs. Temperature

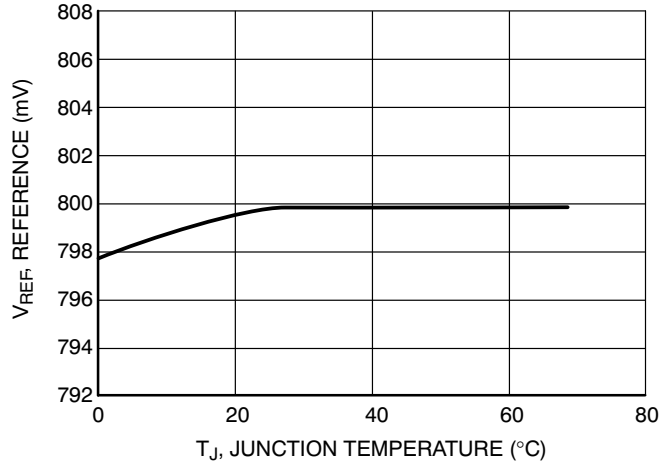


Figure 4. Reference Voltage ( $V_{REF}$ ) vs. Temperature

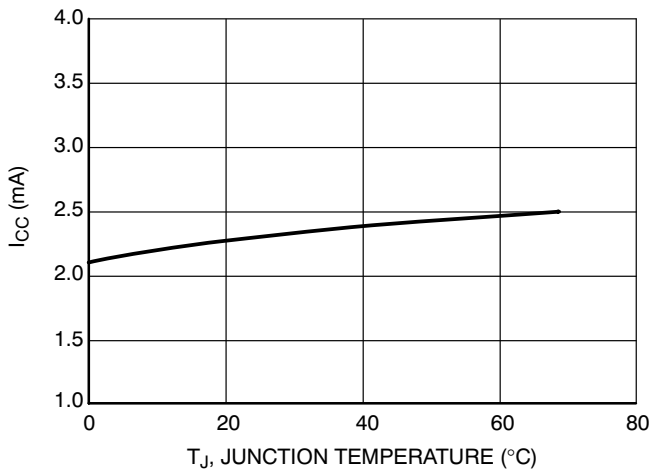


Figure 5.  $I_{CC}$  vs. Temperature

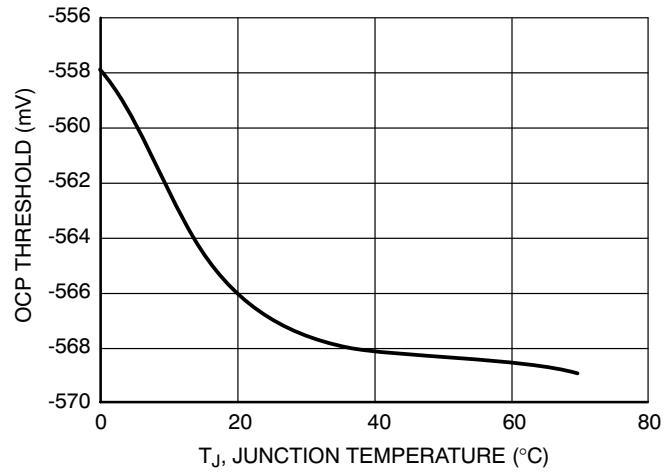


Figure 6. OCP Threshold with 55k Rset vs. Temperature

[查询"NCP1588MTR2G"供应商](#)**Overcurrent Protection (OCP)**

The low-side  $R_{DS(on)}$  sense is implemented by comparing the voltage at the LX, at the end of LG on time to an internally generated fixed voltage. If the phase voltage is lower than OCP trip voltage, an overcurrent condition occurs and a counter is initiated.

When the counter completes after two clock cycles, the PWM logic and both HS-FET and LS-FET are turned off. Power has to be recycled to exit out of the overcurrent fault. The minimum turn-on time of the LS-FET is set to be 500 ns.

NCP1588 allows to easily program an Overcurrent Threshold ranging from 50 mV to 550 mV, simply by adding a resistor (ROCSET) between LG and GND. During a short period of time following  $V_{CC}$  rising over UVLO threshold, an internal 10  $\mu$ A current (IOCSET) is sourced from LG pin, determining a voltage drop across ROCSET. This voltage drop will be sampled and internally held by the device as OverCurrent Threshold. The OC setting procedure overall time length is about 4.2 ms. Connecting a ROCSET resistor between LG and GND, the programmed threshold will be:

$$I_{OCth} = \frac{I_{OCSET} \cdot R_{OCSET}}{R_{DS(on)}}$$

RSET values range from 5 k $\Omega$  to 55 k $\Omega$ . In case ROCSET is not connected, the device switches the OCP threshold to a fixed 640 mV value: an internal safety clamp on BG is triggered as soon as LG voltage reaches 700 mV, enabling the 640 mV fixed threshold and ending OC setting phase. The current trip threshold tolerance is  $\pm 25$  mV. The accuracy of the set point is best at the highest set point. The accuracy will decrease as the set point decreases.

**Internal Soft –Start**

The NCP1588 features an internal soft-start function, which reduces the inrush current and overshoot of the output voltage. Figure 7. shows a typical soft-start sequence. Soft-Start is achieved by ramping the internal reference using the oscillator clock (64 steps from 0 V to 0.8 V of  $V_{REF}$ ). The order of startup sequence is as follows: UVLO  $\rightarrow$  OCP programming  $\rightarrow$  Comp voltage reach the lower end of the Ramp voltage (1.1 V). The typical soft-start time is 4.2 ms. The internal soft-start is held low when the part is in UVLO or Disable mode.

**Power Good**

Power Good is an open drain and active high output. This output can be pulled up high to the appropriate level with an external resistor. It monitors the output voltage through the VOS pin. The PGOOD is flagged low for  $\pm 10\%$  of  $V_{out}$  for OV/UV trip points respectively. The separate VOS input is not slowed down by the compensation on the VFB pin. The PGOOD output can deliver a max of 4 mA sink current at 0.4 V when de-asserted. The PGOOD pin is held low during soft-start. Once soft-start is complete PGOOD goes high if there are no faults without any delays associated to it.

**Undervoltage Protection**

If the voltage at VOS pin drops below UV threshold, the device turns off both HS and LS MOSFETs, latching the condition. This requires a POR to recover.

**Overvoltage Protection**

If the voltage at VOS pin rises over OV threshold (1V typ), overvoltage protection turns off UG MOSFET and turns on LG MOSFET. The LG MOSFET will be turned off as soon as VOS goes below  $V_{ref}/2$  (0.4 V). The condition is latched, and requires POR to recover. The device still controls the LG MOSFET and can switch it on whenever VOS rises above 0.4 V.

# NCP1588

[查询"NCP1588MTR2G"供应商](#)

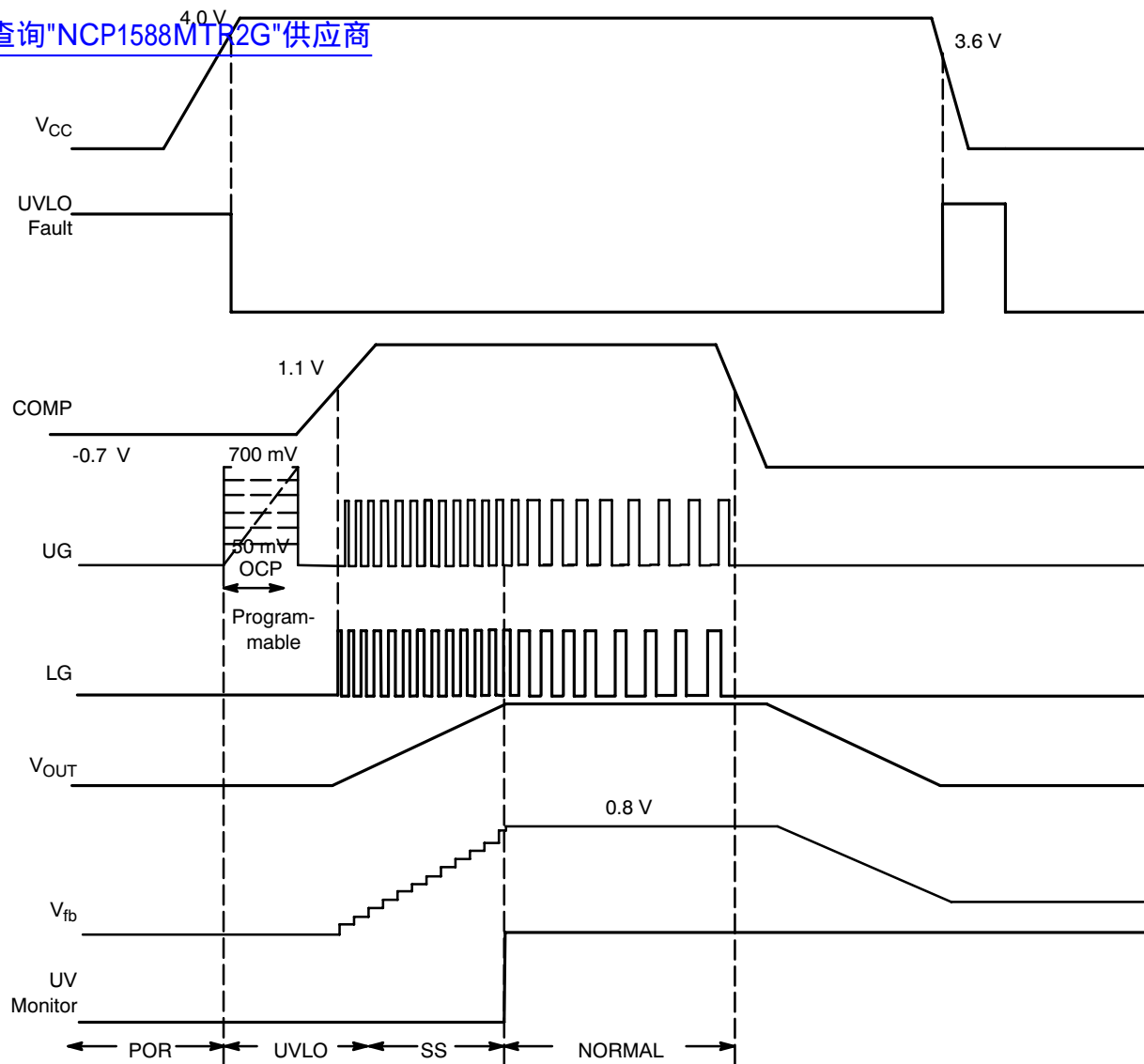


Figure 7. Typical Startup Sequence

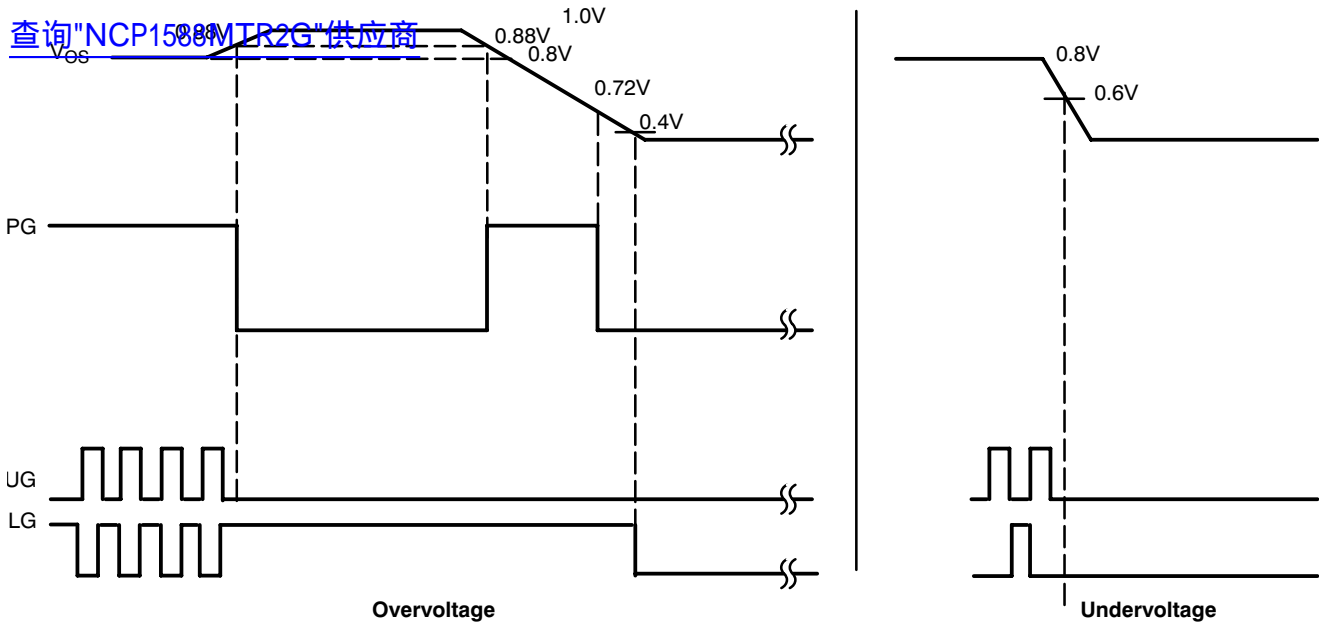


Figure 8. Typical Power Good Function

**Feedback and Compensation**

The NCP1588 allows the output voltage to be adjusted from 0.8 V to 5.0 V via an external resistor divider network. The controller will try to maintain 0.8 V at feedback pin. Thus, if a resistor divider circuit was placed across the feedback pin to  $V_{OUT}$ , the controller will regulate the output voltage proportional to the resistor divider network in order to maintain 0.8 V at the FB pin. The same formula applies to the VOS pin and the controller will maintain 0.8 V at the VOS pin.

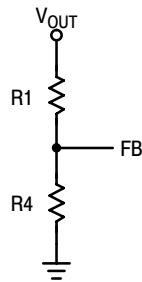


Figure 9.

The relationship between the resistor divider network above and the output voltage is shown in the following equation:

$$R_4 = R_1 \times \left( \frac{V_{REF}}{V_{OUT} - V_{REF}} \right)$$

The same formula can be applied to the feedback resistors at VOS.

$$R_9 = R_{10} \times \left( \frac{V_{REF}}{V_{OUT} - V_{REF}} \right)$$

**Design Example:**

**Voltage Mode Control Loop with TYPE III Compensation**

**Converter Parameters:**

- Input Voltage:  $V_{IN} = 5 \text{ V}$
- Output Voltage:  $V_{OUT} = 1.65 \text{ V}$
- Switching Frequency: 300 kHz
- Total Output Capacitance:  $C_{OUT} = 3600 \mu\text{F}$
- Total ESR:  $\text{ESR} = 6 \text{ m}\Omega$
- Output Inductance:  $L_{OUT} = 1 \mu\text{H}$
- Ramp Amplitude:  $V_{RAMP} = 1 \text{ V}$

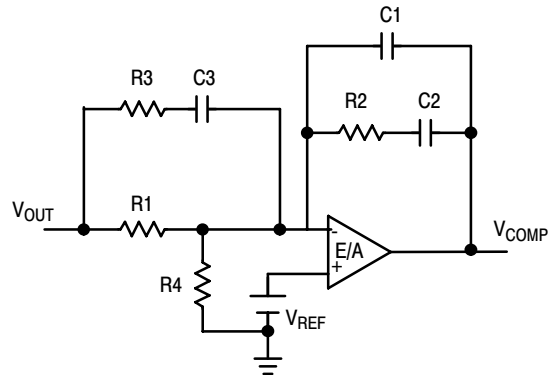


Figure 10.

- a.. Set a target for the close loop bandwidth at 1/6<sup>th</sup> of the switching frequency.

$$F_{\text{cross\_over}} := 50 \text{ kHz}$$

b. Output Filter Double Pole Frequency  
[查询 NCP1588MTR2G 供应商](#)

$$F_{lc} := \frac{1}{2 \cdot \pi \cdot \sqrt{L_{OUT} \cdot C_{OUT}}}$$

$$F_{lc} = 2.653 \text{ kHz}$$

c.. ESR Zero Frequency:

$$F_{ESR} := \frac{1}{2 \cdot \pi \cdot C_{OUT} \cdot C_{ESR}}$$

$$F_{ESR} = 7.368 \text{ kHz}$$

Step 1: Set a value for R1 between 2 kΩ and 5 kΩ

$$R1 := 4.12 \text{ k}\Omega$$

Step 2: Pick compensation DC gain (R2/R1) for desired close loop bandwidth.

$$V_{RAMP} := 1.1 \text{ V}$$

$$R2 := R1 \cdot \left( \frac{V_{RAMP}}{V_{IN}} \right) \cdot \left( \frac{F_{cross\_over}}{F_{lc}} \right)$$

$$R2 = 17.085 \text{ k}\Omega$$

Step 3: Place 1st zero at half the output filter double pole frequency.

$$C2 := \frac{2 \cdot \sqrt{L_{OUT} \cdot C_{OUT}}}{R2}$$

$$C2 = 7.024 \times 10^{-3} \mu\text{F}$$

Step 4: Place 1st pole at ESR zero frequency.

$$C1 := \frac{C2}{C2 \cdot R2 \cdot 2 \cdot \pi \cdot F_{ESR} - 1}$$

$$C1 = 1.542 \times 10^{-3} \mu\text{F}$$

Step 5: Place 2<sup>nd</sup> zero at the output filter double pole frequency.

$$R3 := \frac{R1}{\frac{F_{SW}}{2 \cdot F_{lc}} - 1}$$

$$R3 = 74.169 \Omega$$

Step 6: Place 2<sup>nd</sup> pole at half the switching frequency.

$$C3 := \frac{1}{(\pi \cdot R3 \cdot F_{SW})}$$

$$C3 = 0.014 \mu\text{F}$$

Step 7: R4 is sized to maintain the feedback voltage to  $V_{REF} = 0.8 \text{ V}$ .

$$R4 := \frac{V_{REF} \cdot R1}{V_{OUT} - V_{REF}}$$

$$R4 = 3.878 \text{ k}\Omega$$

**The Component values for Type III Compensation are:**

$$R1 = 4.12 \text{ k}\Omega$$

$$R2 = 17.085 \text{ k}\Omega$$

$$R3 = 74.169 \Omega$$

$$R4 = 3.878 \text{ k}\Omega$$

$$C1 = 0.0015 \mu\text{F}$$

$$C2 = 0.007 \mu\text{F}$$

$$C3 = 0.014 \mu\text{F}$$

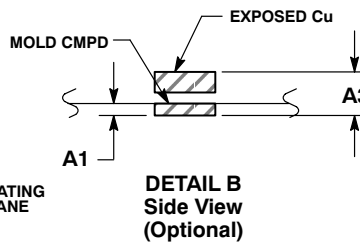
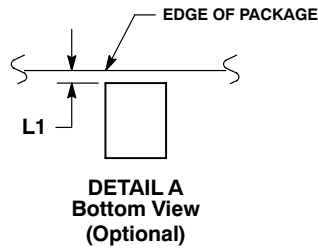
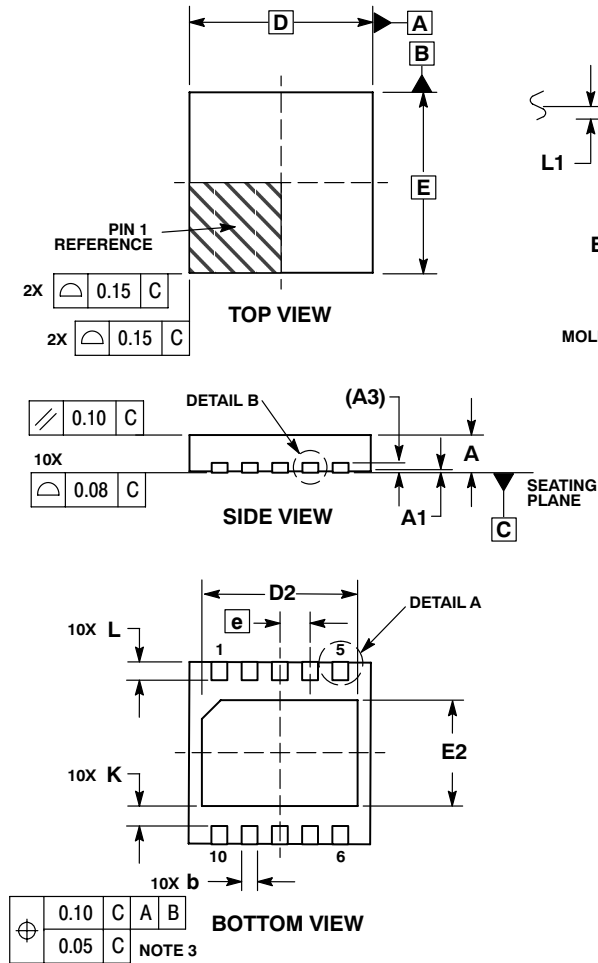
NOTE: Recommend to change values to industry standard component values.

# NCP1588

查询"NCP1588MTR2G"供应商

## PACKAGE DIMENSIONS

DFN10, 3x3, 0.5P  
CASE 485C-01  
ISSUE A

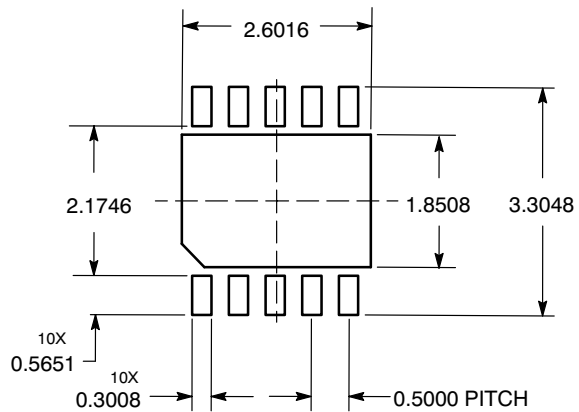


**NOTES:**

1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
2. CONTROLLING DIMENSION: MILLIMETERS.
3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.
5. TERMINAL b MAY HAVE MOLD COMPOUND MATERIAL ALONG SIDE EDGE. MOLD FLASHING MAY NOT EXCEED 30 MICRONS ONTO BOTTOM SURFACE OF TERMINAL b.
6. DETAILS A AND B SHOW OPTIONAL VIEWS FOR END OF TERMINAL LEAD AT EDGE OF PACKAGE.

MILLIMETERS		
DIM	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A3	0.20	REF
b	0.18	0.30
D	3.00	BSC
D2	2.45	2.55
E	3.00	BSC
E2	1.75	1.85
e	0.50	BSC
K	0.19	TYP
L	0.35	0.45
L1	0.00	0.03

### SOLDERING FOOTPRINT\*



DIMENSIONS: MILLIMETERS

\*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

ON Semiconductor and are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

### PUBLICATION ORDERING INFORMATION

**LITERATURE FULFILLMENT:**  
Literature Distribution Center for ON Semiconductor  
P.O. Box 5163, Denver, Colorado 80217 USA  
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada  
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada  
Email: orderlit@onsemi.com

**N. American Technical Support:** 800-282-9855 Toll Free USA/Canada  
**Europe, Middle East and Africa Technical Support:** Phone: 421 33 790 2910  
**Japan Customer Focus Center** Phone: 81-3-5773-3850

**ON Semiconductor Website:** [www.onsemi.com](http://www.onsemi.com)  
**Order Literature:** <http://www.onsemi.com/orderlit>  
For additional information, please contact your local Sales Representative