



March 2002
Revised March 2002

74LCXZ16240

Low Voltage 16-Bit Inverting Buffer/Line Driver with 5V Tolerant Inputs/Outputs

General Description

The LCXZ16240 contains sixteen inverting buffers with 3-STATE outputs designed to be employed as a memory and address driver, clock driver, or bus-oriented transmitter/receiver. The device is nibble controlled. Each nibble has separate 3-STATE control inputs which can be shorted together for full 16-bit operation.

When V_{CC} is between 0 and 1.5V, the LCXZ16240 is in the high impedance state during power up or power down. This places the outputs in the high impedance (Z) state preventing intermittent low impedance loading or glitching in bus oriented applications.

The LCXZ16240 is designed for low voltage (2.7V or 3.3V) V_{CC} applications with capacity of interfacing to a 5V signal environment.

The LCXZ16240 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

Features

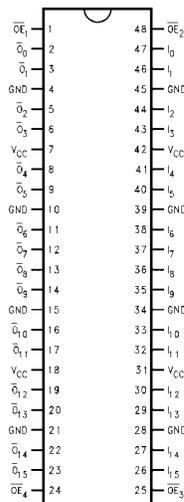
- 5V tolerant inputs and outputs
- Guaranteed power up/down high impedance
- Supports live insertion/withdrawal
- 2.7V–3.6V V_{CC} specifications provided
- 4.5 ns t_{PD} max ($V_{CC} = 3.3V$), 20 μA I_{CC} max
- ± 24 mA output drive ($V_{CC} = 3.0V$)
- Implements patented noise/EMI reduction circuitry
- Latch-up performance exceeds 500 mA
- ESD performance:
 - Human body model > 2000V
 - Machine model > 200V

Ordering Code:

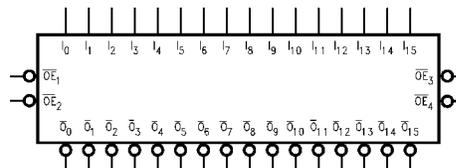
Order Number	Package Number	Package Description
74LCXZ16240MEA	MS48A	48-Lead Small Shrink Outline Package (SSOP), JEDEC MO-118, 0.300" Wide
74LCXZ16240MTD	MTD48	48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Connection Diagram



Logic Symbol



Pin Descriptions

Pin Names	Description
\overline{OE}_n	Output Enable Inputs (Active LOW)
I_0 – I_{15}	Inputs
O_0 – O_{15}	Outputs

74LCXZ16240 Low Voltage 16-Bit Inverting Buffer/Line Driver with 5V Tolerant Inputs/Outputs

74LCXZ16240

Truth Tables

Inputs		Outputs
\overline{OE}_1	I_0-I_3	$\overline{O}_0-\overline{O}_3$
L	L	H
L	H	L
H	X	Z

Inputs		Outputs
\overline{OE}_3	I_8-I_{11}	$\overline{O}_8-\overline{O}_{11}$
L	L	H
L	H	L
H	X	Z

Inputs		Outputs
\overline{OE}_2	I_4-I_7	$\overline{O}_4-\overline{O}_7$
L	L	H
L	H	L
H	X	Z

Inputs		Outputs
\overline{OE}_4	$I_{12}-I_{15}$	$\overline{O}_{12}-\overline{O}_{15}$
L	L	H
L	H	L
H	X	Z

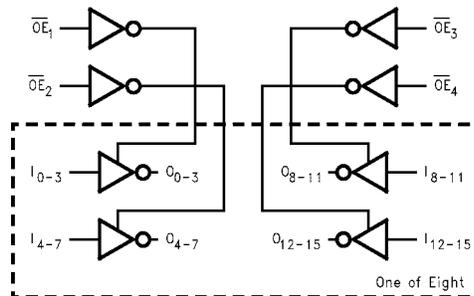
H = HIGH Voltage Level
 L = LOW Voltage Level
 X = Immaterial
 Z = High Impedance

Functional Description

The LCXZ16240 contains sixteen inverting buffers with 3-STATE standard outputs. The device is nibble (4 bits) controlled with each nibble functioning identically, but independent of the other. The control pins may be shorted together to obtain full 16-bit operation. The 3-STATE outputs are

controlled by an Output Enable (\overline{OE}_n) input for each nibble. When \overline{OE}_n is LOW, the outputs are in 2-state mode. When \overline{OE}_n is HIGH, the outputs are in the high impedance mode, but this does not interfere with entering new data into the inputs.

Logic Diagram



Absolute Maximum Ratings (Note 1)					
Symbol	Parameter	Value	Conditions	Units	
V _{CC}	Supply Voltage	-0.5 to +7.0		V	
V _I	DC Input Voltage	-0.5 to +7.0		V	
V _O	DC Output Voltage	-0.5 to +7.0 -0.5 to V _{CC} + 0.5	Output in 3-STATE or V _{CC} = 0-1.5V Output in HIGH or LOW State (Note 2)	V	
I _{IK}	DC Input Diode Current	-50	V _I < GND	mA	
I _{OK}	DC Output Diode Current	-50 +50	V _O < GND V _O > V _{CC}	mA	
I _O	DC Output Source/Sink Current	±50		mA	
I _{CC}	DC Supply Current per Supply Pin	±100		mA	
I _{GND}	DC Ground Current per Ground Pin	±100		mA	
T _{STG}	Storage Temperature	-65 to +150		°C	

Recommended Operating Conditions (Note 3)						
Symbol	Parameter	Min	Max	Units		
V _{CC}	Supply Voltage	Operating		2.7	3.6	V
V _I	Input Voltage	0	5.5	V		
V _O	Output Voltage	0	V _{CC}	V		
I _{OH} /I _{OL}	Output Current	0	5.5	V		
		HIGH or LOW State 3-STATE or V _{CC} = OFF		0	5.5	V
		V _{CC} = 3.0V - 3.6V V _{CC} = 2.7V - 3.0V		±24 ±12		mA
T _A	Free-Air Operating Temperature	-40	85	°C		
Δt/ΔV	Input Edge Rate, V _{IN} = 0.8V-2.0V, V _{CC} = 3.0V	0	10	ns/V		

Note 1: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 2: I_O Absolute Maximum Rating must be observed.

Note 3: Unused inputs must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

Symbol	Parameter	Conditions	V _{CC} (V)	T _A = -40°C to +85°C		Units
				Min	Max	
V _{IH}	HIGH Level Input Voltage		2.7 - 3.6	2.0		V
V _{IL}	LOW Level Input Voltage		2.7 - 3.6		0.8	V
V _{OH}	HIGH Level Output Voltage	I _{OH} = -100 μA	2.7 - 3.6	V _{CC} - 0.2		V
		I _{OH} = -12 mA	2.7	2.2		
		I _{OH} = -18 mA	3.0	2.4		
		I _{OH} = -24 mA	3.0	2.2		
V _{OL}	LOW Level Output Voltage	I _{OL} = 100 μA	2.7 - 3.6		0.2	V
		I _{OL} = 12 mA	2.7		0.4	
		I _{OL} = 16 mA	3.0		0.4	
		I _{OL} = 24 mA	3.0		0.55	
I _I	Input Leakage Current	0 ≤ V _I ≤ 5.5V	2.7 - 3.6		±5.0	μA
I _{OZ}	3-STATE Output Leakage	0 ≤ V _O ≤ 5.5V V _I = V _{IH} or V _{IL}	2.7 - 3.6		±5.0	μA
I _{OFF}	Power-Off Leakage Current	V _I or V _O = 5.5V	0		10	μA
I _{PU/PD}	Power Up/Down 3-STATE Output Current	V _O = 0.5V to V _{CC} V _I = GND or V _{CC}	0 - 1.5		±5.0	μA
I _{CC}	Quiescent Supply Current	V _I = V _{CC} or GND	2.7 - 3.6		225	μA
		3.6V ≤ V _I , V _O ≤ 5.5V (Note 4)	2.7 - 3.6		±225	
ΔI _{CC}	Increase in I _{CC} per Input	V _{IH} = V _{CC} - 0.6V	2.7 - 3.6		500	μA

Note 4: Outputs disabled or 3-STATE only.

74LCXZ16240

AC Electrical Characteristics						
Symbol	Parameter	$T_A = -40^\circ\text{C to } +85^\circ\text{C}, R_L = 500 \Omega$				Units
		$V_{CC} = 3.3V \pm 0.3V$		$V_{CC} = 2.7V$		
		$C_L = 50 \text{ pF}$		$C_L = 50 \text{ pF}$		
		Min	Max	Min	Max	
t_{PHL}	Propagation Delay	1.0	4.5	1.0	5.3	ns
t_{PLH}	Data to Output	1.0	4.5	1.0	5.3	
t_{PZL}	Output Enable Time	1.0	5.4	1.0	6.0	ns
t_{PZH}	Output Disable Time	1.0	5.4	1.0	6.0	
t_{PLZ}	Output Disable Time	1.0	5.3	1.0	5.4	ns
t_{PHZ}	Output Enable Time	1.0	5.3	1.0	5.4	
t_{OSHL}	Output to Output Skew (Note 5)		1.0			ns
t_{OSLH}	Output to Output Skew (Note 5)		1.0			

Note 5: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t_{OSHL}) or LOW-to-HIGH (t_{OSLH}).

Dynamic Switching Characteristics					
Symbol	Parameter	Conditions	V_{CC} (V)	$T_A = 25^\circ\text{C}$	Unit
				Typical	
V_{OLP}	Quiet Output Dynamic Peak V_{OL}	$C_L = 50 \text{ pF}, V_{IH} = 3.3V, V_{IL} = 0V$	3.3	0.8	V
V_{OLV}	Quiet Output Dynamic Valley V_{OL}	$C_L = 50 \text{ pF}, V_{IH} = 3.3V, V_{IL} = 0V$	3.3	-0.8	V

Capacitance				
Symbol	Parameter	Conditions	Typical	Units
C_{IN}	Input Capacitance	$V_{CC} = \text{Open}, V_I = 0V \text{ or } V_{CC}$	7	pF
C_{OUT}	Output Capacitance	$V_{CC} = 3.3V, V_I = 0V \text{ or } V_{CC}$	8	pF
C_{PD}	Power Dissipation Capacitance	$V_{CC} = 3.3V, V_I = 0V \text{ or } V_{CC}, f = 10 \text{ MHz}$	20	pF

AC LOADING and WAVEFORMS Generic for LCX Family

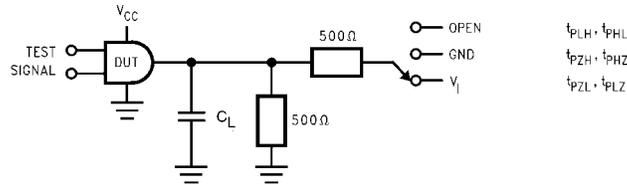
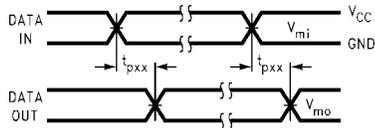
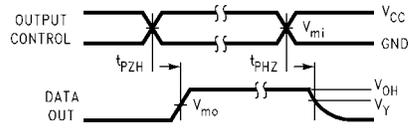


FIGURE 1. AC Test Circuit (C_L includes probe and jig capacitance)

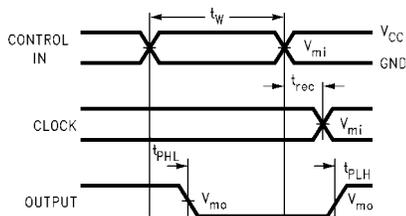
V_I	C_L
6V for $V_{CC} = 3.3V, 2.7V$	50 pF
$V_{CC} * 2$ for $V_{CC} = 2.5V$	30 pF



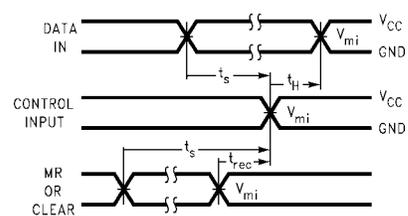
Waveform for Inverting and Non-Inverting Functions



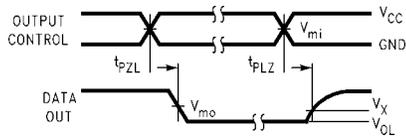
3-STATE Output High Enable and Disable Times for Logic



Propagation Delay, Pulse Width and t_{rec} Waveforms



Setup Time, Hold Time and Recovery Time for Logic



3-STATE Output Low Enable and Disable Times for Logic

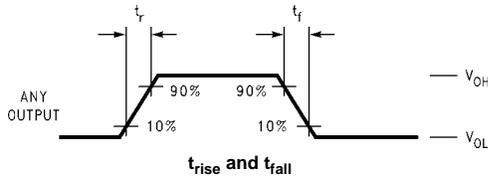
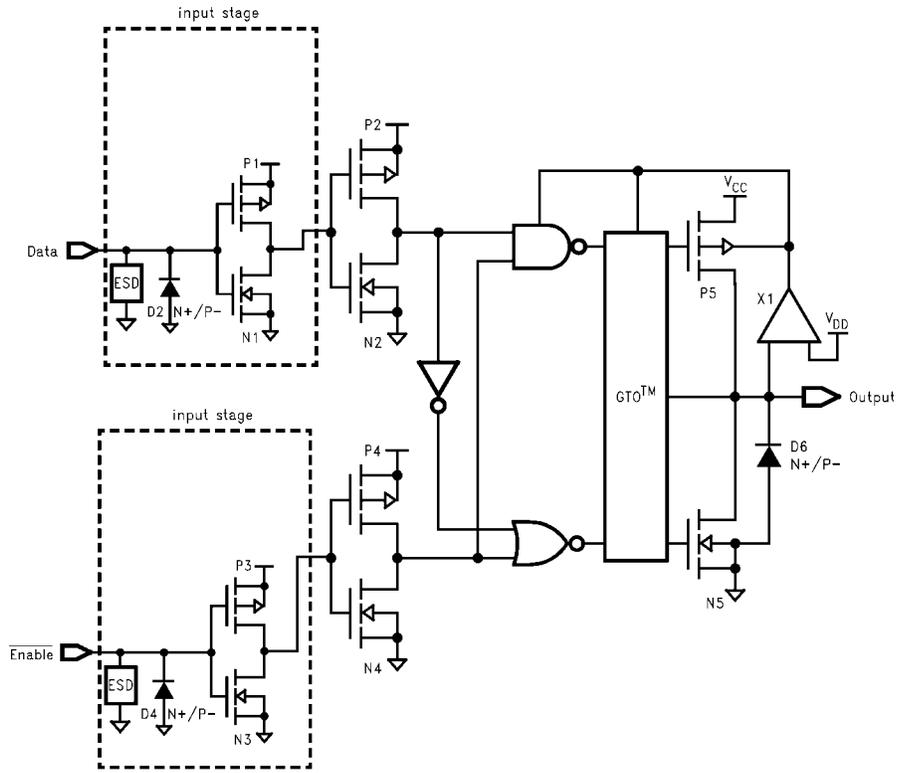


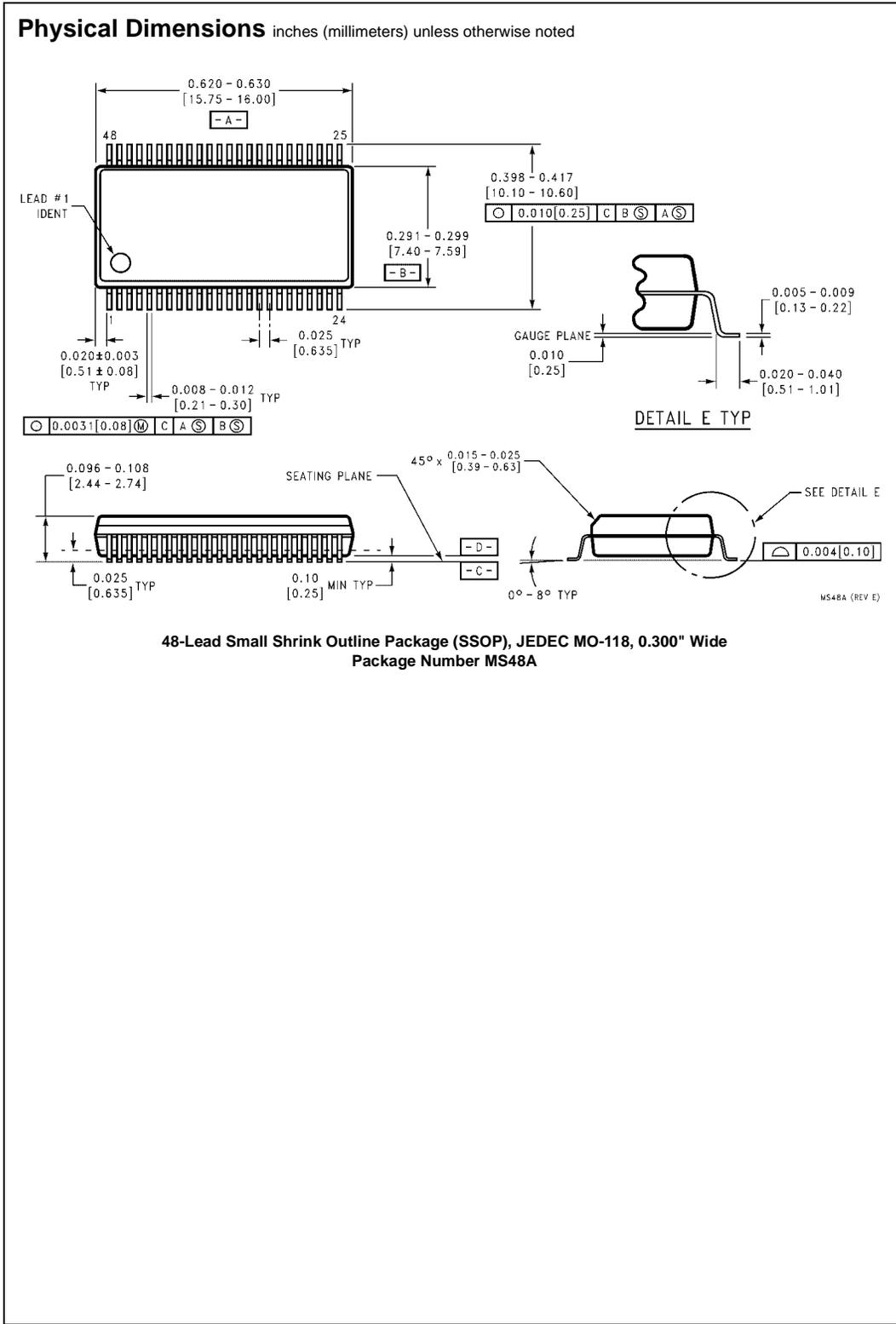
FIGURE 2. Waveforms (Input Characteristics; $f = 1MHz, t_R = t_F = 3ns$)

Symbol	V_{CC}	
	3.3V ± 0.3V	2.7V
V_{mi}	1.5V	1.5V
V_{mo}	1.5V	1.5V
V_x	$V_{OL} + 0.3V$	$V_{OL} + 0.3V$
V_y	$V_{OH} - 0.3V$	$V_{OH} - 0.3V$

74LCXZ16240

Schematic Diagram Generic for LCX Family





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Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

DIMENSIONS ARE IN MILLIMETERS

NOTES:

- A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AB, REF NOTE 6, DATE 7/93.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
- D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

MTD48RevB1

**48-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide
Package Number MTD48**

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