M24M01-R

1 Mbit serial I²C bus EEPROM

Features

■ Compatible with I²C extended addressing

■ Two-wire I²C serial interface supports 1 MHz protocol

■ Single supply voltage:
  – 1.8 V to 5.5 V

■ Hardware write control

■ Byte and Page Write (up to 256 bytes)

■ Random and Sequential Read modes

■ Self-timed programming cycle

■ Automatic address incrementing

■ Enhanced ESD/Latch-Up protection

■ More than 1 million Write cycles

■ More than 40-year data retention

■ Packages
  – ECOPACK® (RoHS compliant)

SO8 (MN)
150 mils width

SO8 (MW)
208 mils width

Contents

Contents

List of tables

List of figures

1 Description

The M24M01-R is an I^{2}C-compatible electrically erasable programmable memory (EEPROM) device organized as 128 Kb × 8 bits.

The I^{2}C bus is a two-wire serial interface, comprising a bidirectional data line and a clock line. The devices carry a built-in 4-bit device type identifier code (1010) in accordance with the I^{2}C bus definition.

The M24M01-R behaves as a slave in the I^{2}C protocol, with all memory operations synchronized by the serial clock. Read and Write operations are generated by the bus master and initiated by a Start condition, followed by the device select code, address bytes and data bytes. Data transfers are terminated by a Stop condition after an Ack for Write, and after a NoAck for Read.

When writing data to the memory, the device inserts an acknowledge bit during the 9th bit time, following the bus master's 8-bit transmission. When data is read by the bus master, the bus master acknowledges the receipt of the data byte in the same way.

In order to meet environmental requirements, ST offers the M24M01-R in ECOPACK® packages. ECOPACK® packages are Lead-free and RoHS compliant.

ECOPACK is an ST trademark. ECOPACK specifications are available at: *www.st.com*.

Figure 1. Logic diagram
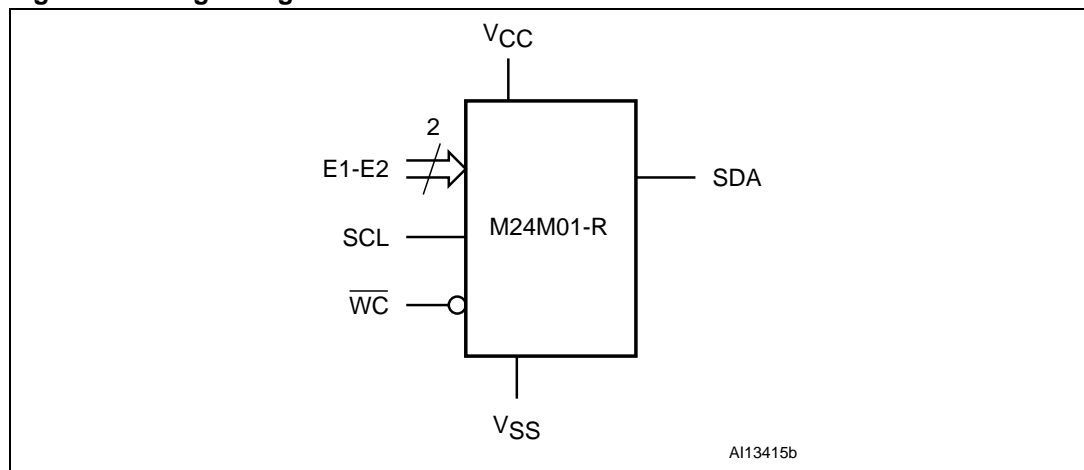
Table 1. Signal names

Signal name	Function	Direction
E1, E2	Chip Enable	Input
SDA	Serial Data	I/O
SCL	Serial Clock	Input
$\overline{WC}$	Write Control	Input
V$_{CC}$	Supply voltage	
V$_{SS}$	Ground	

Figure 2.   SO connections

M24M01-R

```
        ┌──────────┐
  NC ⌷ │1        8│ ⌷ V_CC
  E1 ⌷ │2        7│ ⌷ WC
  E2 ⌷ │3        6│ ⌷ SCL
 V_SS ⌷ │4        5│ ⌷ SDA
        └──────────┘
```

AI13416b
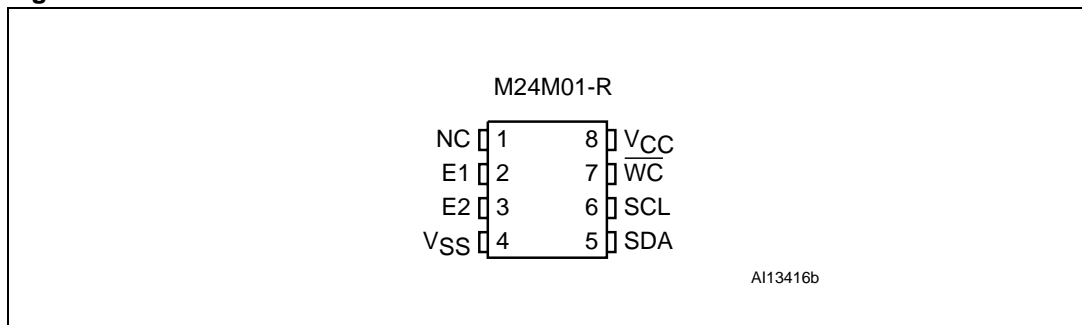
1. See *Section 7: Package mechanical* for package dimensions, and how to identify pin-1.

2. NC = Not Connected internally.

2 Signal description

2.1 Serial Clock (SCL)

This input signal is used to strobe all data in and out of the device. In applications where this signal is used by slave devices to synchronize the bus to a slower clock, the bus master must have an open drain output, and a pull-up resistor must be connected from Serial Clock (SCL) to V_{CC}. (*Figure 5* indicates how the value of the pull-up resistor can be calculated). In most applications, though, this method of synchronization is not employed, and so the pull-up resistor is not necessary, provided that the bus master has a push-pull (rather than open drain) output.

2.2 Serial Data (SDA)

This bidirectional signal is used to transfer data in or out of the device. It is an open drain output that may be wire-OR'ed with other open drain or open collector signals on the bus. A pull up resistor must be connected from Serial Data (SDA) to V_{CC}. (*Figure 5* indicates how the value of the pull-up resistor can be calculated).

2.3 Chip Enable (E1, E2)

These input signals are used to set the value that is to be looked for on the two bits (b2, b1) of the 7-bit device select code. These inputs must be tied to V_{CC} or V_{SS}, to establish the device select code as shown in *Figure 3*. When not connected (left floating), these inputs are read as low (0,0).

Figure 3.   Device select code
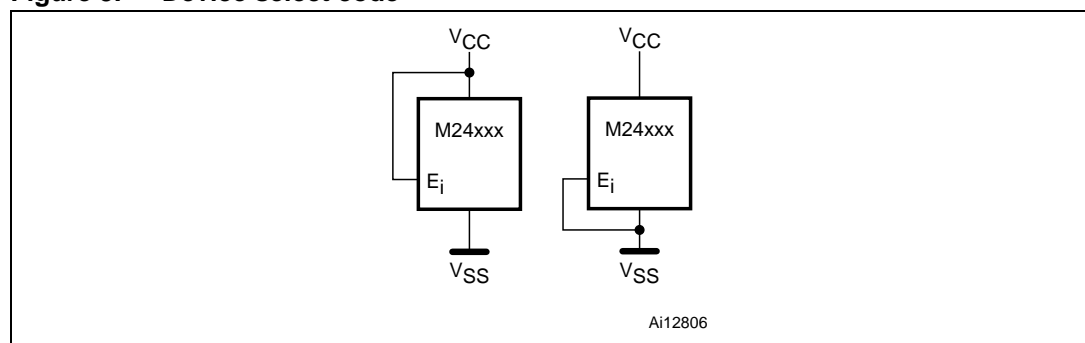
2.4 Write Control ($\overline{WC}$)

This input signal is useful for protecting the entire contents of the memory from inadvertent write operations. Write operations are disabled to the entire memory array when Write Control ($\overline{WC}$) is driven high. When unconnected, the signal is internally read as V_{IL}, and Write operations are allowed.

When Write Control ($\overline{WC}$) is driven high, device select and address bytes are acknowledged, Data bytes are not acknowledged.

2.5 V_{SS} ground

V_{SS} is the reference for the V_{CC} supply voltage.

2.6   Supply voltage (V_{CC})

2.6.1   Operating supply voltage V_{CC}

Prior to selecting the memory and issuing instructions to it, a valid and stable V_{CC} voltage within the specified [V_{CC}(min), V_{CC}(max)] range must be applied (see *Table 7*). In order to secure a stable DC supply voltage, it is recommended to decouple the V_{CC} line with a suitable capacitor (usually of the order of 10 nF to 100 nF) close to the V_{CC}/V_{SS} package pins.

This voltage must remain stable and valid until the end of the transmission of the instruction and, for a Write instruction, until the completion of the internal write cycle (t_W).

2.6.2   Power-up conditions

When the power supply is turned on, V_{CC} rises from V_{SS} to V_{CC}. The V_{CC} rise time must not vary faster than 1 V/µs.

2.6.3   Device reset

In order to prevent inadvertent Write operations during power-up, a power on reset (POR) circuit is included. At power-up (continuous rise of V_{CC}), the device does not respond to any instruction until V_{CC} has reached the power on reset threshold voltage (this threshold is lower than the minimum V_{CC} operating voltage defined in *Table 7*). When V_{CC} passes over the POR threshold, the device is reset and is in Standby Power mode.

In a similar way, during power-down (continuous decrease in V_{CC}), as soon as V_{CC} drops below the Power On Reset threshold voltage, the device stops responding to any instruction sent to it.

2.6.4   Power-down conditions

During power-down (continuous decrease in V_{CC}), the device must be in the Standby Power mode (mode reached after decoding a Stop condition, assuming that is there is no internal Write cycle in progress).

Figure 4.   Maximum R$_{bus}$ value versus bus parasitic capacitance (C$_{bus}$) for an I^{2}C bus at maximum frequency f$_C$ = 400 kHz

ai14796

Figure 5.   Maximum R$_{bus}$ value versus bus parasitic capacitance (C$_{bus}$) for an I^{2}C bus at maximum frequency f$_C$ = 1MHz

ai14795
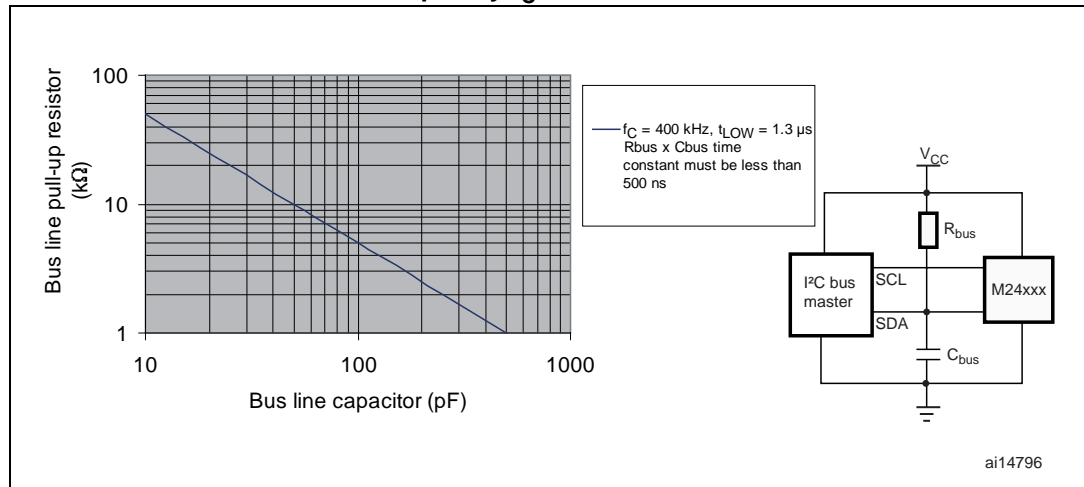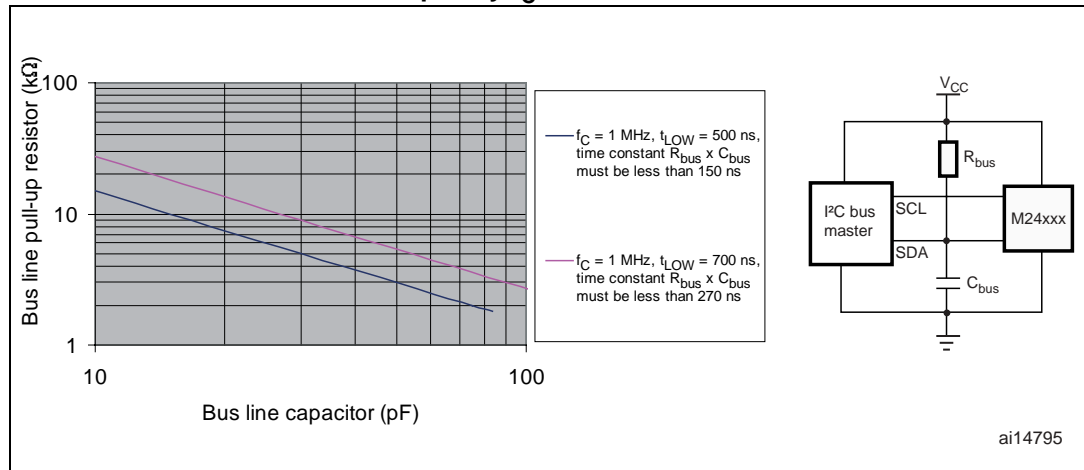
Figure 6. I²C bus protocol
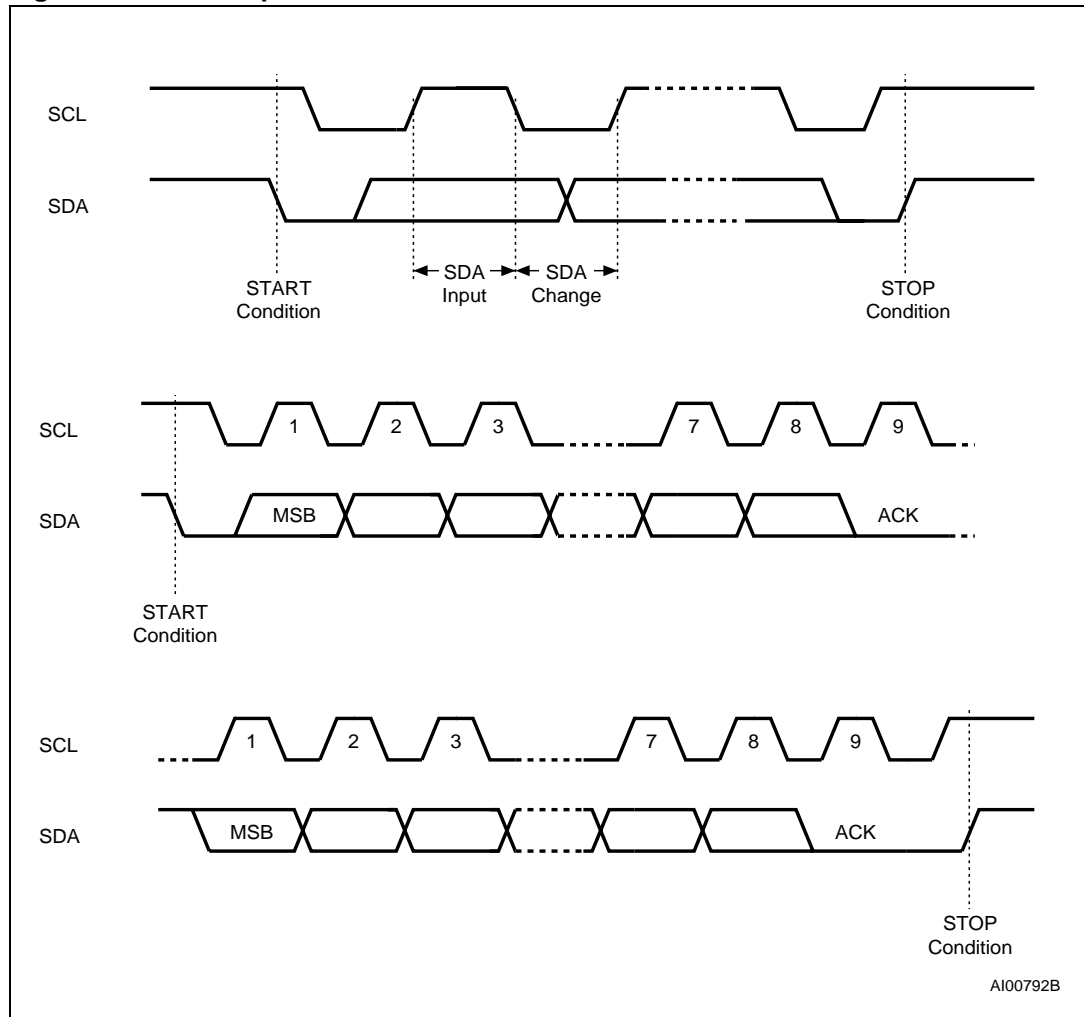
Table 2. Device select code

	Device type identifier[1]				Chip Enable address[2]		A16	R$\overline{\text{W}}$
	b7	b6	b5	b4	b3	b2	b1	b0
Device select code	1	0	1	0	E2	E1	A16	R$\overline{\text{W}}$

1. The most significant bit, b7, is sent first.

2. E1 and E2 are compared against the respective external pins on the memory device.

Table 3. Most significant address byte

b15	b14	b13	b12	b11	b10	b9	b8

Table 4. Least significant address byte

b7	b6	b5	b4	b3	b2	b1	b0

3 Device operation

The device supports the I^{2}C protocol. This is summarized in *Figure 6*. Any device that sends data on to the bus is defined to be a transmitter, and any device that reads the data to be a receiver. The device that controls the data transfer is known as the bus master, and the other as the slave device. A data transfer can only be initiated by the bus master, which will also provide the serial clock for synchronization. The M24M01-R device is always a slave in all communication.

3.1 Start condition

Start is identified by a falling edge of Serial Data (SDA) while Serial Clock (SCL) is stable in the high state. A Start condition must precede any data transfer command. The device continuously monitors (except during a Write cycle) Serial Data (SDA) and Serial Clock (SCL) for a Start condition, and will not respond unless one is given.

3.2 Stop condition

Stop is identified by a rising edge of Serial Data (SDA) while Serial Clock (SCL) is stable and driven high. A Stop condition terminates communication between the device and the bus master. A Read command that is followed by NoAck can be followed by a Stop condition to force the device into the Standby mode. A Stop condition at the end of a Write command triggers the internal EEPROM Write cycle.

3.3 Acknowledge bit (ACK)

The acknowledge bit is used to indicate a successful byte transfer. The bus transmitter, whether it be bus master or slave device, releases Serial Data (SDA) after sending eight bits of data. During the 9th clock pulse period, the receiver pulls Serial Data (SDA) low to acknowledge the receipt of the eight data bits.

3.4 Data input

During data input, the device samples Serial Data (SDA) on the rising edge of Serial Clock (SCL). For correct device operation, Serial Data (SDA) must be stable during the rising edge of Serial Clock (SCL), and the Serial Data (SDA) signal must change *only* when Serial Clock (SCL) is driven low.

3.5 Memory addressing

To start communication between the bus master and the slave device, the bus master must initiate a Start condition. Following this, the bus master sends the device select code, shown in *Table 2* (on Serial Data (SDA), most significant bit first).

The device select code consists of a 4-bit device type identifier, and a 2-bit Chip Enable "Address" (E2, E1). To address the memory array, the 4-bit device type identifier is 1010b.

Up to four memory devices can be connected on a single I^2C bus. Each one is given a unique 2-bit code on the Chip Enable (E1, E2) inputs. When the device select code is received, the device only responds if the Chip Enable Address is the same as the value on the Chip Enable (E1, E2) inputs.

The 8th bit is the Read/$\overline{Write}$ bit (R$\overline{W}$). This bit is set to 1 for Read and 0 for Write operations.

If a match occurs on the device select code, the corresponding device gives an acknowledgment on Serial Data (SDA) during the 9th bit time. If the device does not match the device select code, it deselects itself from the bus, and goes into Standby mode.

Table 5.   Operating modes

Mode	R$\overline{W}$ bit	$\overline{WC}$[1]	Bytes	Initial sequence
Current Address Read	1	X	1	Start, device select, R$\overline{W}$ = 1
Random Address Read	0	X	1	Start, device select, R$\overline{W}$ = 0, Address
	1	X		reStart, device select, R$\overline{W}$ = 1
Sequential Read	1	X	≥ 1	Similar to Current or Random Address Read
Byte Write	0	V_{IL}	1	Start, device select, R$\overline{W}$ = 0
Page Write	0	V_{IL}	≤256	Start, device select, R$\overline{W}$ = 0

1.   X = V_{IH} or V_{IL}.

Figure 7.   Write mode sequences with $\overline{WC}$ = 1 (data write inhibited)
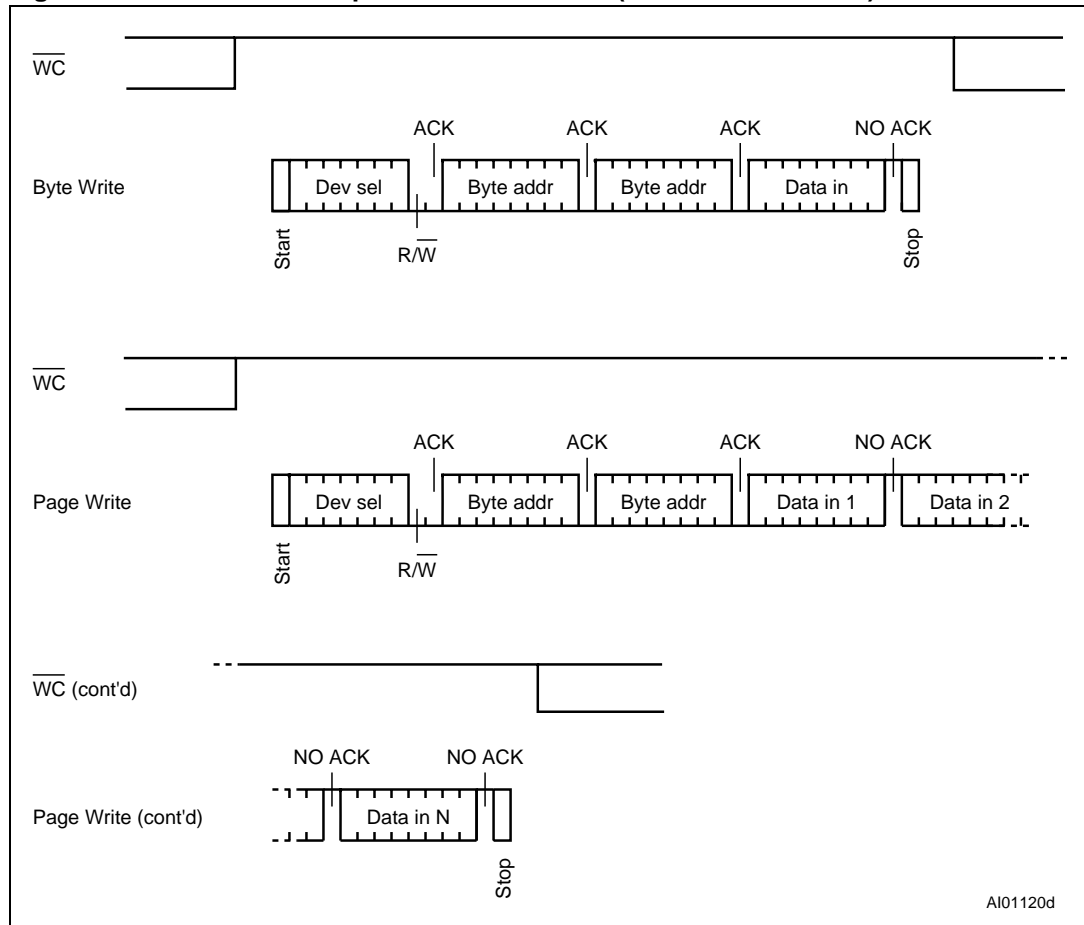
3.6 Write operations

Following a Start condition the bus master sends a device select code with the R/$\overline{W}$ bit (R$\overline{W}$) reset to 0. The device acknowledges this, as shown in *Figure 8*, and waits for two address bytes. The device responds to each address byte with an acknowledge bit, and then waits for the data byte.

Writing to the memory may be inhibited if Write Control ($\overline{WC}$) is driven high. Any Write instruction with Write Control ($\overline{WC}$) driven high (during a period of time from the Start condition until the end of the two address bytes) will not modify the memory contents, and the accompanying data bytes are *not* acknowledged, as shown in *Figure 7*.

Each data byte in the memory has a 17-bit address (the most significant bit b16 is in the device select code and the Least Significant Bits b15-b0 are defined in two address bytes). The most significant byte (*Table 3*) is sent first, followed by the least significant byte (*Table 4*).

When the bus master generates a Stop condition immediately after the Ack bit (in the "10th bit" time slot), either at the end of a Byte Write or a Page Write, the internal memory Write cycle is triggered. A Stop condition at any other time slot does not trigger the internal Write cycle.

After the Stop condition, the delay t_W, and the successful completion of a Write operation, the device's internal address counter is incremented automatically, to point to the next byte address after the last one that was modified.

During the internal Write cycle, Serial Data (SDA) is disabled internally, and the device does not respond to any requests.

3.7 Byte Write

After the device select code and the address bytes, the bus master sends one data byte. If the addressed location is Write-protected, by Write Control ($\overline{WC}$) being driven high, the device replies with NoAck, and the location is not modified. If, instead, the addressed location is not Write-protected, the device replies with Ack. The bus master terminates the transfer by generating a Stop condition, as shown in *Figure 8*.

3.8 Page Write

The Page Write mode allows up to 256 bytes to be written in a single Write cycle, provided that they are all located in the same 'row' in the memory: that is, the most significant memory address bits, b15-b6, are the same. If more bytes are sent than will fit up to the end of the row, a condition known as 'roll-over' occurs. This should be avoided, as data starts to become overwritten in an implementation dependent way.

The bus master sends from 1 to 256 bytes of data, each of which is acknowledged by the device if Write Control ($\overline{WC}$) is low. If Write Control ($\overline{WC}$) is high, the contents of the addressed memory location are not modified, and each data byte is followed by a NoAck. After each byte is transferred, the internal byte address counter (the 6 least significant address bits only) is incremented. The transfer is terminated by the bus master generating a Stop condition.

Figure 8. Write mode sequences with $\overline{WC}$ = 0 (data write enabled)
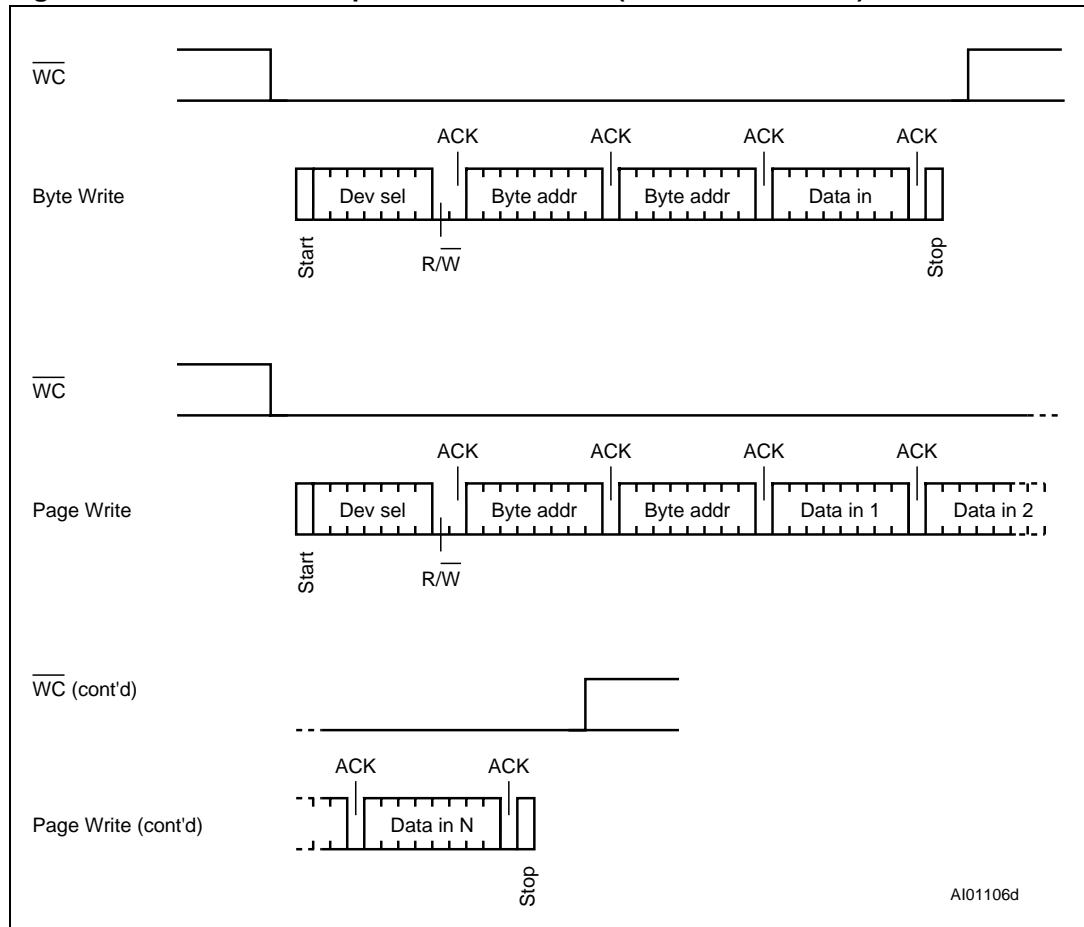

3.9 ECC (error correction code) and Write cycling

The M24M01-R device offers an ECC (error correction code) logic which compares each 4-byte word with its six associated EEPROM ECC bits. As a result, if a single bit out of 4 bytes of data happens to be erroneous during a Read operation, the ECC detects it and replaces it by the correct value. The read reliability is therefore much improved by the use of this feature.

Note however that even if a single byte has to be written, 4 bytes are internally modified (plus the ECC word), that is, the addressed byte is cycled together with the three other bytes making up the word. It is therefore recommended to write by packets of 4 bytes in order to benefit from the larger amount of Write cycles.

The M24M01-R device is qualified at 1 million (1 000 000) Write cycles, using a cycling routine that writes to the device by multiples of 4-byte words.

**Figure 9.**   **Write cycle polling flowchart using ACK**
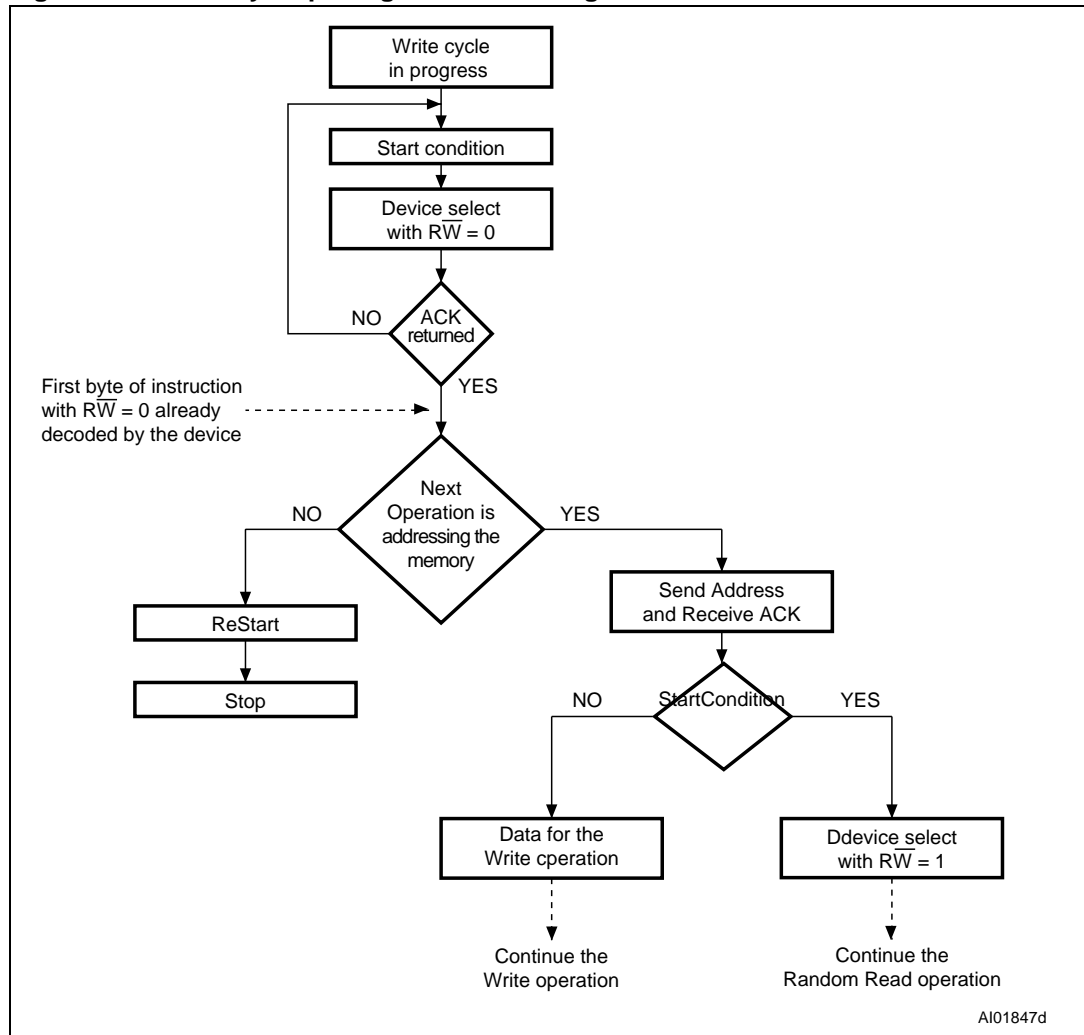
3.10 Minimizing system delays by polling on ACK

During the internal Write cycle, the device disconnects itself from the bus, and writes a copy of the data from its internal latches to the memory cells. The maximum Write time (t_w) is shown in *Table 11*, but the typical time is shorter. To make use of this, a polling sequence can be used by the bus master.

The sequence, as shown in *Figure 9*, is:

● Initial condition: a Write cycle is in progress.

● Step 1: the bus master issues a Start condition followed by a device select code (the first byte of the new instruction).

● Step 2: if the device is busy with the internal Write cycle, no Ack will be returned and the bus master goes back to Step 1. If the device has terminated the internal Write cycle, it responds with an Ack, indicating that the device is ready to receive the second part of the instruction (the first byte of this instruction having been sent during Step 1).

Figure 10. Read mode sequences
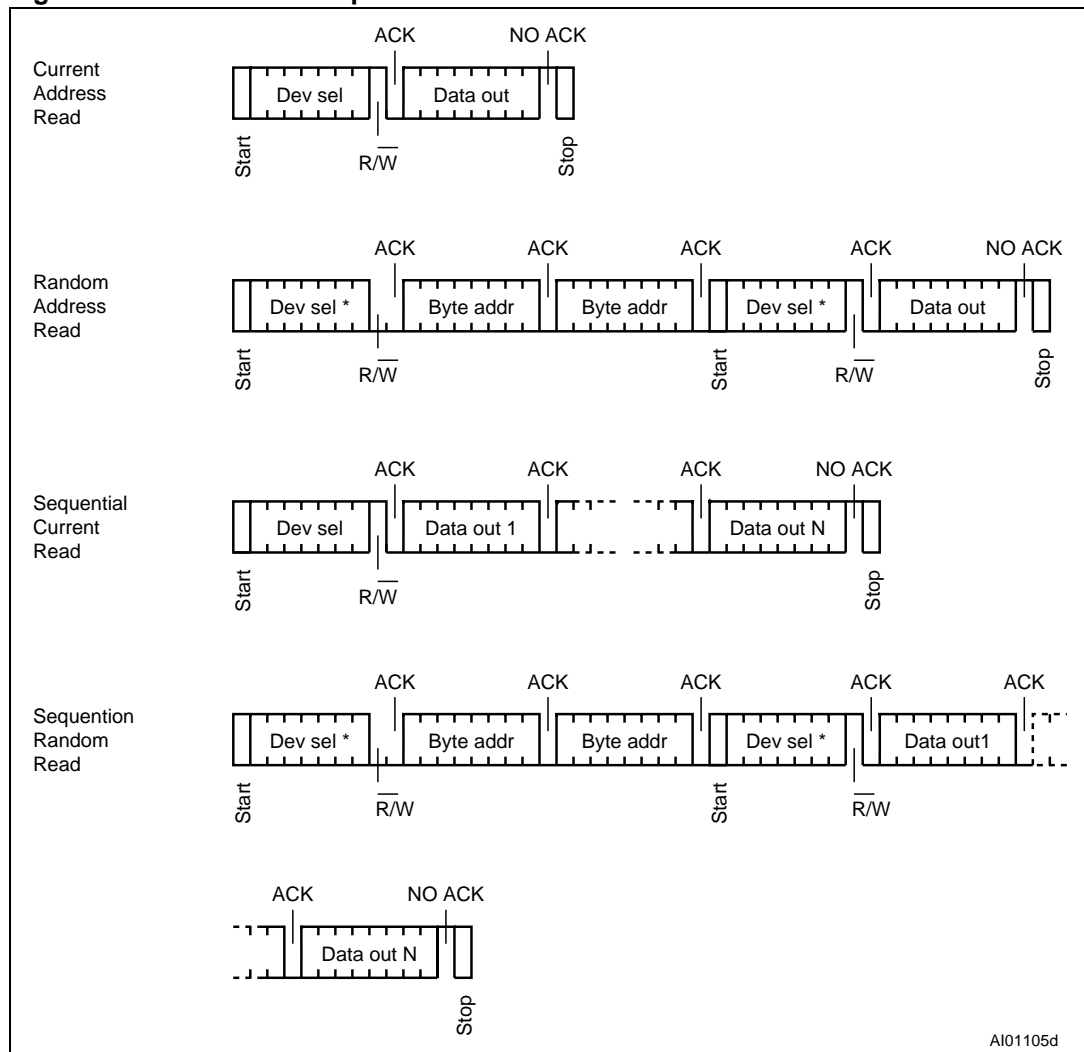
1. The seven most significant bits of the device select code of a Random Read (in the 1st and 4th bytes) must be identical.

3.11 Read operations

Read operations are performed independently of the state of the Write Control ($\overline{WC}$) signal.

After the successful completion of a Read operation, the device's internal address counter is incremented by one, to point to the next byte address.

3.12 Random Address Read

A dummy Write is first performed to load the address into this address counter (as shown in *Figure 10*) but *without* sending a Stop condition. Then, the bus master sends another Start condition, and repeats the device select code, with the R$\overline{W}$ bit set to 1. The device acknowledges this, and outputs the contents of the addressed byte. The bus master must *not* acknowledge the byte, and terminates the transfer with a Stop condition.

3.13 Current Address Read

For the Current Address Read operation, following a Start condition, the bus master only sends a device select code with the R/$\overline{W}$ bit set to 1. The device acknowledges this, and outputs the byte addressed by the internal address counter. The counter is then incremented. The bus master terminates the transfer with a Stop condition, as shown in *Figure 10*, *without* acknowledging the byte.

3.14 Sequential Read

This operation can be used after a Current Address Read or a Random Address Read. The bus master *does* acknowledge the data byte output, and sends additional clock pulses so that the device continues to output the next byte in sequence. To terminate the stream of bytes, the bus master must *not* acknowledge the last byte, and *must* generate a Stop condition, as shown in *Figure 10*.

The output data comes from consecutive addresses, with the internal address counter automatically incremented after each byte output. After the last memory address, the address counter 'rolls-over', and the device continues to output data from memory address 00h.

3.15 Acknowledge in Read mode

For all Read commands, the device waits, after each byte read, for an acknowledgment during the 9th bit time. If the bus master does not drive Serial Data (SDA) low during this time, the device terminates the data transfer and switches to its Standby mode.

4   Initial delivery state

The device is delivered with all the memory array bits set to 1 (each byte contains FFh).

5   Maximum rating

Stressing the device outside the ratings listed in *Table 6* may cause permanent damage to the device. These are stress ratings only, and operation of the device at these, or any other conditions outside those indicated in the operating sections of this specification, is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Refer also to the STMicroelectronics SURE Program and other relevant quality documents.

Table 6.   Absolute maximum ratings

Symbol	Parameter	Min.	Max.	Unit
T_A	Ambient operating temperature	−40	130	°C
T_{STG}	Storage temperature	−65	150	°C
T_{LEAD}	Lead temperature during soldering	see note [1]		°C
V_{IO}	Input or output range	−0.50	V_{CC} + 0.6	V
V_{CC}	Supply voltage	−0.50	6.5	V
V_{ESD}	Electrostatic discharge voltage (Human Body model)[2]	−3000	3000	V

1. Compliant with JEDEC Std J-STD-020D (for small body, Sn-Pb or Pb assembly), the ST ECOPACK® 7191395 specification, and the European directive on Restrictions on Hazardous Substances (RoHS) 2002/95/EU.

2. AEC-Q100-002 (compliant with JEDEC Std JESD22-A114A, C1=100pF, R1=1500Ω, R2=500Ω)

6   DC and AC parameters

This section summarizes the operating and measurement conditions, and the DC and AC characteristics of the device. The parameters in the DC and AC characteristic tables that follow are derived from tests performed under the measurement conditions summarized in the relevant tables. Designers should check that the operating conditions in their circuit match the measurement conditions when relying on the quoted parameters.

Table 7.   Operating conditions

Symbol	Parameter	Min.	Max.	Unit
V_{CC}	Supply voltage	1.8	5.5	V
T_A	Ambient operating temperature	–40	85	°C

Table 8.   AC measurement conditions

Symbol	Parameter	Min.	Max.	Unit
C_L	Load capacitance	100		pF
	Input rise and fall times		50	ns
	Input levels	$0.2V_{CC}$ to $0.8V_{CC}$		V
	Input and output timing reference levels	$0.3V_{CC}$ to $0.7V_{CC}$		V

Figure 11.   AC measurement I/O waveform
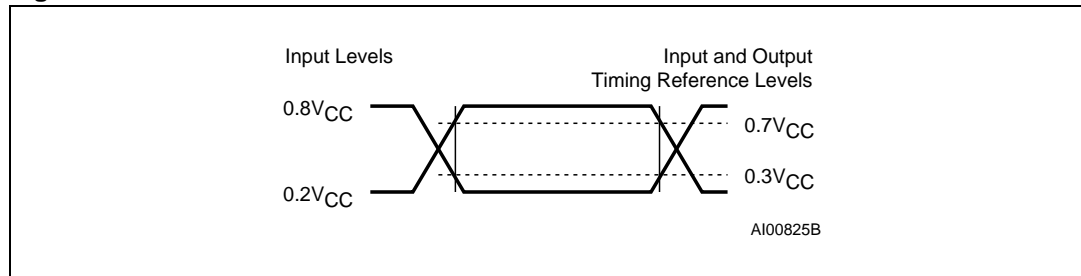
Table 9.   Input parameters

Symbol	Parameter[1]	Test condition	Min.	Max.	Unit
C_{IN}	Input capacitance (SDA)			8	pF
C_{IN}	Input capacitance (other pins)			6	pF
Z_L	Input impedance ($\overline{WC}$)	$V_{IN} < 0.3\ V_{CC}$	30		kΩ
Z_H		$V_{IN} > 0.7V_{CC}$	400		kΩ

1. Sampled only, not 100% tested.

Table 10.   DC characteristics

Symbol	Parameter	Test condition (in addition to those in *Table 7*)	Min.	Max.	Unit
I_{LI}	Input leakage current (E1, E2, SCL, SDA)	$V_{IN} = V_{SS}$ or V_{CC} device in Standby mode		± 2	µA
I_{LO}	Output leakage current	$V_{OUT} = V_{SS}$ or V_{CC}, SDA in Hi-Z		± 2	µA
I_{CC}	Supply current (Read)	V_{CC} = 1.8 V, f_c= 400 kHz (rise/fall time < 50 ns)		0.8	mA
		V_{CC} = 2.5 V, f_c= 400 kHz (rise/fall time < 50 ns)		1	mA
		V_{CC} = 5.0 V, f_c= 400 kHz (rise/fall time < 50 ns)		2	mA
		1.8 V < V_{CC} < 5.5 V, f_c= 1 MHz (rise/fall time < 50 ns)		2.5	mA
I_{CC0}	Supply current (Write)	During t_W, 1.8V < V_{CC} < 5.5V		5[1]	mA
I_{CC1}	Standby supply current	$V_{IN} = V_{SS}$ or V_{CC}, V_{CC} = 1.8 V		1	µA
		$V_{IN} = V_{SS}$ or V_{CC}, V_{CC} = 2.5 V		2	µA
		$V_{IN} = V_{SS}$ or V_{CC}, V_{CC} = 5.5 V		3	µA
V_{IL}	Input low voltage (SCL, SDA, $\overline{WC}$)	1.8 V ≤V_{CC} < 2.5 V	−0.45	0.25 V_{CC}	V
		2.5 V ≤V_{CC} ≤5.5 V	−0.45	0.3 V_{CC}	
V_{IH}	Input high voltage (SCL, SDA, $\overline{WC}$)	1.8 V ≤V_{CC} < 2.5 V	0.75V_{CC}	V_{CC}+1	V
		2.5 V ≤V_{CC} ≤5.5 V	0.7V_{CC}	V_{CC}+1	
V_{OL}	Output low voltage	I_{OL} = 0.7 mA, V_{CC} = 1.8 V		0.2	V
		I_{OL} = 2.1 mA, V_{CC} = 2.5 V		0.4	V
		I_{OL} = 3.0 mA, V_{CC} = 5.5 V		0.4	V

1. Characterized value, not tested in production.

Table 11.   **AC characteristics at 400 kHz**

| Symbol	Alt.	Parameter	Min.	Max.	Unit
		Test conditions specified in *Table 7*			
f_C	f_{SCL}	Clock frequency		400	kHz
t_{CHCL}	t_{HIGH}	Clock pulse width high	600		ns
t_{CLCH}	t_{LOW}	Clock pulse width low	1300		ns
t_{XH1XH2}[1]	t_R	Input signal rise time	20	300	ns
t_{XL1XL2}[1]	t_F	Input signal fall time	20	300	ns
t_{DL1DL2}	t_F	SDA (out) fall time	20	100	ns
t_{DXCX}	$t_{SU:DAT}$	Data in set up time	100		ns
t_{CLDX}	$t_{HD:DAT}$	Data in hold time	0		ns
t_{CLQX}	t_{DH}	Data out hold time	200		ns
t_{CLQV}[2][3]	t_{AA}	Clock low to next data valid (access time)	200	900	ns
t_{CHDX}[4]	$t_{SU:STA}$	Start condition set up time	600		ns
t_{DLCL}	$t_{HD:STA}$	Start condition hold time	600		ns
t_{CHDH}	$t_{SU:STO}$	Stop condition set up time	600		ns
t_{DHDL}	t_{BUF}	Time between Stop condition and next Start condition	1300		ns
t_W		Pulse width ignored (input filter on SCL and SDA)		100	ns
t_{NS}[5]	t_{WR}	Write time 1.8 V < V_{CC} < 5.5 V		5	ms

1. Values recommended by the I²C-bus Fast-Mode specification.

2. To avoid spurious Start and Stop conditions, a minimum delay is placed between SCL=1 and the falling or rising edge of SDA.

3. t_{CLQV} is the time (from the falling edge of SCL) required by the SDA bus line to reach $0.8V_{CC}$ in a compatible way with the I²C specification (which specifies $t_{SU:DAT}$ (min) = 100 ns), assuming that the R_{bus} × C_{bus} time constant is less than 500 ns (as specified in *Figure 4*).

4. For a reStart condition, or following a Write cycle.

5. Characterized only, not tested in production.

Table 12. AC characteristics at 1 MHz (preliminary data)

Symbol	Alt.	Parameter	Min.	Max.	Unit
		**Test conditions specified in Table 7**			
f_C	f_{SCL}	Clock frequency	0	1	MHz
t_{CHCL}	t_{HIGH}	Clock pulse width high	300	-	ns
t_{CLCH}	t_{LOW}	Clock pulse width low	400	-	ns
t_{XH1XH2}[1]	t_R	Input signal rise time	20	300	ns
t_{XL1XL2}[1]	t_F	Input signal fall time	20	300	ns
t_{DL1DL2}[2]	t_F	SDA (out) fall time	20	100	ns
t_{DXCX}	$t_{SU:DAT}$	Data in setup time	80	-	ns
t_{CLDX}	$t_{HD:DAT}$	Data in hold time	0	-	ns
t_{CLQX}	t_{DH}	Data out hold time	50	-	ns
t_{CLQV}[3][4]	t_{AA}	Clock low to next data valid (access time)	50	500	ns
t_{CHDX}[5]	$t_{SU:STA}$	Start condition setup time	250	-	ns
t_{DLCL}	$t_{HD:STA}$	Start condition hold time	250	-	ns
t_{CHDH}	$t_{SU:STO}$	Stop condition setup time	250	-	ns
t_{DHDL}	t_{BUF}	Time between Stop condition and next Start condition	500	-	ns
t_W	t_{WR}	Write time	-	5	ms
t_{NS}[2]		Pulse width ignored (input filter on SCL and SDA)	-	50	ns

1. Values recommended by the I²C-bus Fast-Mode specification.

2. Characterized only, not tested in production.

3. To avoid spurious Start and Stop conditions, a minimum delay is placed between SCL=1 and the falling or rising edge of SDA.

4. t_{CLQV} is the time (from the falling edge of SCL) required by the SDA bus line to reach $0.8V_{CC}$, assuming that the $R_{bus} \times C_{bus}$ time constant is less than 150 ns (as specified in Figure 4).

5. For a reStart condition, or following a Write cycle.

Figure 12. AC waveforms

AI00795e
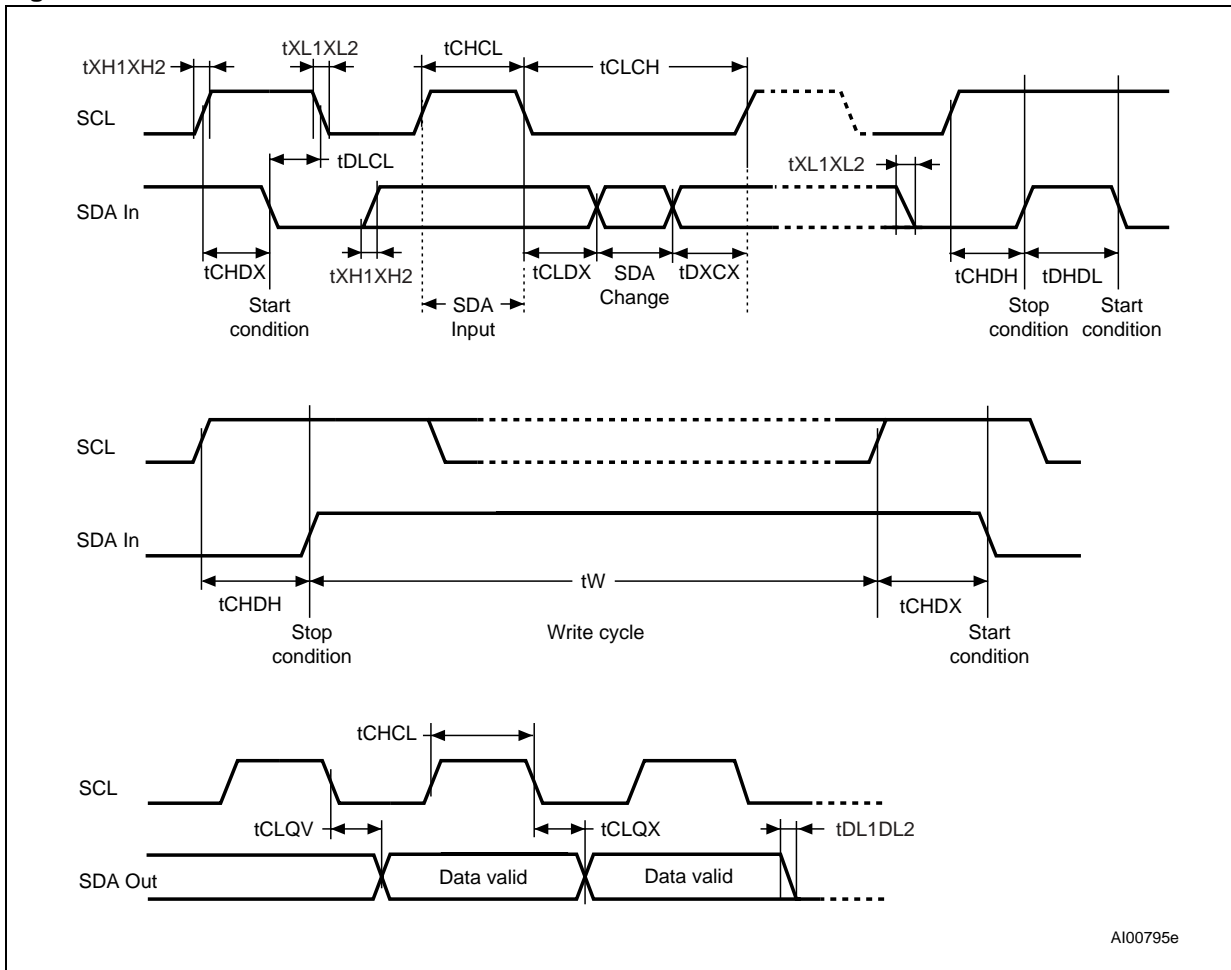
7 Package mechanical

Figure 13. SO8 narrow – 8 lead plastic small outline, 150 mils body width, package outline
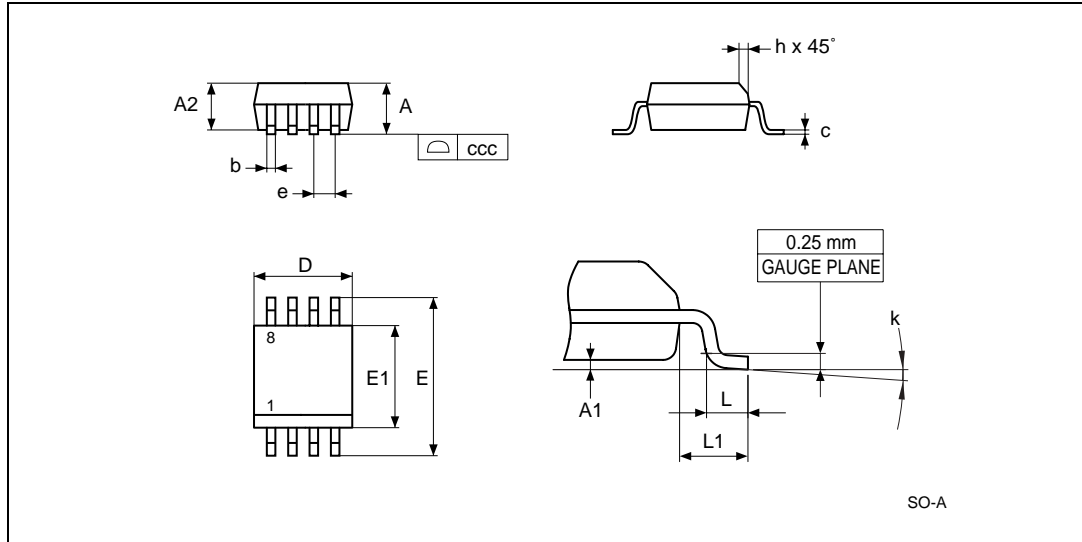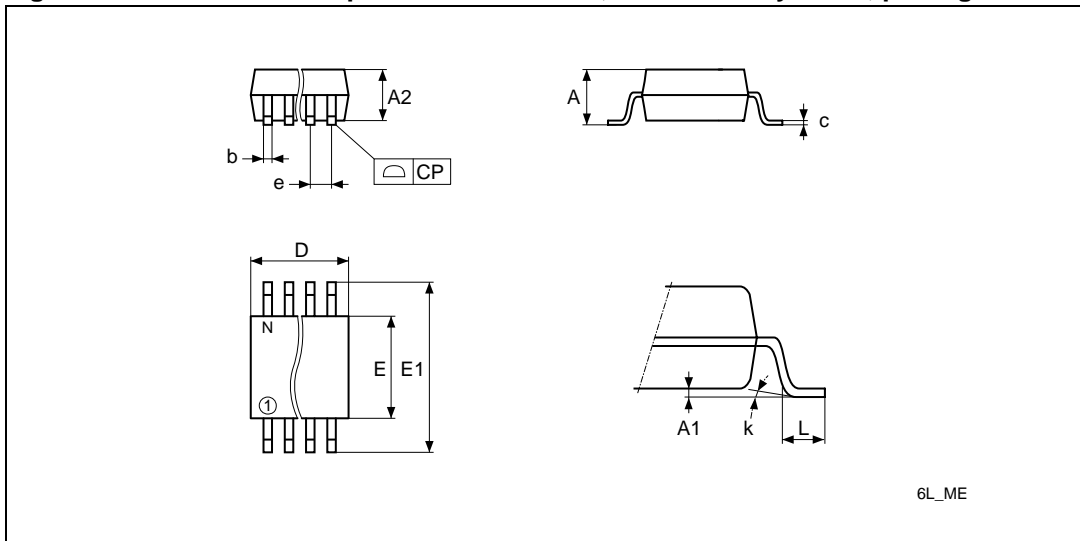

1. Drawing is not to scale.

Table 13. SO8 narrow – 8 lead plastic small outline, 150 mils body width, package mechanical data

Symbol	millimeters			inches[1]		
	Typ	Min	Max	Typ	Min	Max
A			1.75			0.0689
A1		0.1	0.25		0.0039	0.0098
A2		1.25			0.0492	
b		0.28	0.48		0.011	0.0189
c		0.17	0.23		0.0067	0.0091
ccc			0.1			0.0039
D	4.9	4.8	5	0.1929	0.189	0.1969
E	6	5.8	6.2	0.2362	0.2283	0.2441
E1	3.9	3.8	4	0.1535	0.1496	0.1575
e	1.27	-	-	0.05	-	-
h		0.25	0.5		0.0098	0.0197
k		0°	8°		0°	8°
L		0.4	1.27		0.0157	0.05
L1	1.04			0.0409		

1. Values in inches are converted from mm and rounded to 4 decimal digits.

Figure 14.   SO8W – 8 lead plastic small outline, 208 mils body width, package outline

1.   Drawing is not to scale.

2.   The '1' that appears in the top view of the package shows the position of pin 1 and the 'N' indicates the total number of pins.

Table 14.   SO8W – 8 lead plastic small outline, 208 mils body width, package mechanical data

Symbol	millimeters			inches[1]		
	Typ	Min	Max	Typ	Min	Max
A			2.5			0.0984
A1		0	0.25		0	0.0098
A2		1.51	2		0.0594	0.0787
b	0.4	0.35	0.51	0.0157	0.0138	0.0201
c	0.2	0.1	0.35	0.0079	0.0039	0.0138
CP			0.1			0.0039
D			6.05			0.2382
E		5.02	6.22		0.1976	0.2449
E1		7.62	8.89		0.3	0.35
e	1.27	-	-	0.05	-	-
k		0°	10°		0°	10°
L		0.5	0.8		0.0197	0.0315
N	8			8		

1.   Values in inches are converted from mm and rounded to 4 decimal digits.

8 Part numbering

Table 15. Ordering information scheme

Example: M24M01   –   H R MN 6   T   P

Device type

M24 = I^2C serial access EEPROM

Device function

M01 = 1 Mbit (256 Kb × 8 bits)

Clock frequency

Blank: f_C max = 400 kHz

H: f_C max = 1 MHz

Operating voltage

R = V_{CC} = 1.8 V to 5.5 V

Package

MN = SO8 (150 mils width)

MW = SO8 (208 mils width)

Device grade

6 = Industrial temperature range, –40 to 85 °C.
   Device tested with standard test flow

Option

blank = Standard Packing

T = Tape and Reel Packing

Plating technology

P or G = ECOPACK® (RoHS compliant)

For a list of available options (speed, package, etc.) or for further information on any aspect of this device, please contact your nearest ST sales office.

The category of second-level interconnect is marked on the package and on the inner box label, in compliance with JEDEC Standard JESD97. The maximum ratings related to soldering conditions are also marked on the inner box label.

9 Revision history

Table 16.   Document revision history

Date	Revision	Changes
07-Dec-2006	1	Initial release.
02-Oct-2007	2	Document status promoted from Preliminary Data to full Datasheet. *Section 2.6: Supply voltage (VCC)* updated. *Note 1* updated to latest standard revision below *Table 6: Absolute maximum ratings*. V_{IL}, V_{IH} modified and, rise/fall time corrected in Test conditions in *Table 10: DC characteristics*. Package values in inches calculated from mm and rounded to 4 decimal digits (note added below package mechanical data tables in *Section 7: Package mechanical*.
26-Nov-2007	3	1 MHz maximum clock frequency added: – *Figure 5: Maximum Rbus value versus bus parasitic capacitance (Cbus) for an I2C bus at maximum frequency fC = 1MHz* – *Table 12: AC characteristics at 1 MHz (preliminary data)* added. t_{NS} moved from *Table 9: Input parameters* to *Table 11: AC characteristics at 400 kHz*. Note removed below *Table 9*. In *Table 11*, t_{CH1CH2}, t_{CL1CL2} and t_{DL1DL2} removed, t_{XH1XH2}, t_{XL1XL2} added, t_{DL1DL2} max modified, notes modified. *Figure 4: Maximum Rbus value versus bus parasitic capacitance (Cbus) for an I2C bus at maximum frequency fC = 400 kHz* modified. *Figure 12: AC waveforms* modified. Small text changes.

Please Read Carefully: