

Automotive ProASIC3 Family FPGAs

Features and Benefits

High-Temperature AEC-Q100-Qualified Devices

- Grade 2 105°C T_A (115°C T_J)
- Grade 1 125°C T_A (135°C T_J)
- PPAP Documentation

Firm-Error Immune

- Only Automotive FPGAs to Offer Firm-Error Immunity
- Can Be Used without Configuration Upset Risk

High Capacity

- 60 k to 1 M System Gates
- Up to 144 kbits of SRAM
- Up to 300 User I/Os

Reprogrammable Flash Technology

- 130-nm, 7-Layer Metal (6 Copper), Flash-Based CMOS Automotive Process
- Live-at-Power-Up (LAPU) Level 0 Support
- Single-Chip Solution
- Retains Programmed Design when Powered Off

On-Chip User Nonvolatile Memory

- 1 kbit of FlashROM with Synchronous Interface

High Performance

- 350 MHz System Performance
- 3.3 V, 66 MHz 64-Bit PCI

In-System Programming (ISP) and Security

- Secure ISP Using On-Chip 128-Bit Advanced Encryption Standard (AES) Decryption via JTAG (IEEE 1532-compliant)
- FlashLock[®] to Secure FPGA Contents (anti-tampering)

Low Power

- 1.5 V Core Voltage
- Support for 1.5-V-Only Systems
- Low-Impedance Flash Switches

High-Performance Routing Hierarchy

- Segmented, Hierarchical Routing and Clock Structure
- High-Performance, Low-Skew Global Network
- Architecture Supports Ultra-High Utilization

Advanced I/O

- 700 Mbps DDR, LVDS-Capable I/Os
- 1.5 V, 1.8 V, 2.5 V, and 3.3 V Mixed-Voltage Operation
- Bank-Selectable I/O Voltages—up to 4 Banks per Chip
- Single-Ended I/O Standards: LVTTTL, LVCMOS 3.3 V / 2.5 V / 1.8 V / 1.5 V, 3.3 V PCI / 3.3 V PCI-X, and LVCMOS 2.5 V / 5.0 V Input
- Differential I/O Standards: LVPECL, LVDS, B-LVDS, and M-LVDS (A3P250 and A3P1000)
- I/O Registers on Input, Output, and Enable Paths
- Hot-Swappable and Cold-Sparing I/Os
- Programmable Output Slew Rate and Drive Strength
- Weak Pull-Up/Down
- IEEE 1149.1 (JTAG) Boundary Scan Test
- Pin-Compatible Packages across the Automotive ProASIC[®]3 Family

Clock Conditioning Circuit (CCC) and PLL

- Six CCC Blocks, One with an Integrated PLL
- Configurable Phase Shift, Multiply/Divide, Delay Capabilities, and External Feedback
- Wide Input Frequency Range (1.5 MHz up to 350 MHz)

SRAMs

- Variable-Aspect-Ratio 4,608-Bit RAM Blocks (×1, ×2, ×4, ×9, and ×18 organizations available)

Automotive ProASIC3 Product Family

ProASIC3 Devices	A3P060	A3P125	A3P250	A3P1000
System Gates	60 k	125 k	250 k	1 M
VersaTiles (D-flip-flops)	1,536	3,072	6,144	24,576
RAM kbits (1,024 bits)	18	36	36	144
4,608-Bit Blocks	4	8	8	32
FlashROM Bits	1 k	1 k	1 k	1 k
Secure (AES) ISP	Yes	Yes	Yes	Yes
Integrated PLL in CCCs	1	1	1	1
VersaNet Globals*	18	18	18	18
I/O Banks	2	2	4	4
Maximum User I/Os	96	133	157	300
Package Pins				
VQFP	VQ100	VQ100	VQ100	
FBGA	FG144	FG144	FG144, FG256	FG144, FG256, FG484

Note: *Six chip-wide (main) globals and three additional global networks in each quadrant are available.

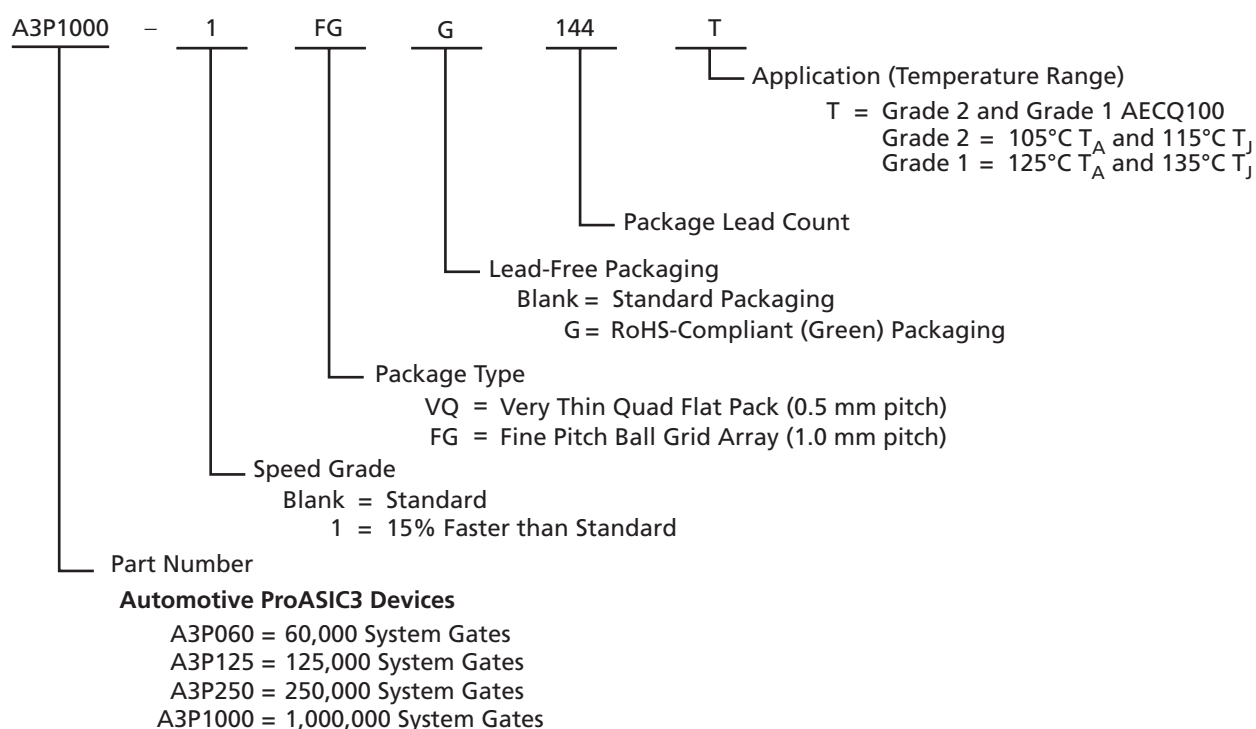
I/Os Per Package

ProASIC3 Devices	A3P060	A3P125	A3P250		A3P1000	
Package	I/O Type					
	Single-Ended I/O	Single-Ended I/O	Single-Ended I/O ²	Differential I/O Pairs	Single-Ended I/O ²	Differential I/O Pairs
VQ100	71	71	68	13	–	–
FG144	96	97	97	24	97	25
FG256	–	–	157	38	177	44
FG484	–	–	–	–	300	74

Notes:

1. When considering migrating your design to a lower- or higher-density device, refer to the [ProASIC3 Flash Family FPGAs handbook](#) to ensure complying with design and board migration requirements.
2. Each used differential I/O pair reduces the number of available single-ended I/Os by two.
3. FG256 and FG484 are footprint-compatible packages.

Automotive ProASIC3 Ordering Information



Note: Minimum order quantities apply. Contact your local Actel sales office for details.

Temperature Grade Offerings

Package	A3P060	A3P125	A3P250	A3P1000
VQ100	C, I, T	C, I, T	C, I, T	–
FG144	C, I, T	C, I, T	C, I, T	C, I, T
FG256	–	–	C, I, T	C, I, T
FG484	–	–	–	C, I, T

Notes:

1. C = Commercial temperature range: 0°C to 70°C
2. I = Industrial temperature range: –40°C to 85°C
3. T = Automotive temperature range: Grade 2 and Grade 1 AEC-Q100
Grade 2 = 105°C T_A and 115°C T_J
Grade 1 = 125°C T_A and 135°C T_J
4. Specifications for Commercial and Industrial grade devices can be found in the [ProASIC3 Flash Family FPGAs handbook](#).

Speed Grade and Temperature Grade Matrix

Temperature Grade	Std.	–1
T (Grade 1 and Grade 2), Commercial, Industrial	✓	✓

Notes:

1. T = Automotive temperature range: Grade 2 and Grade 1 AEC-Q100
Grade 2 = 105°C T_A and 115°C T_J
Grade 1 = 125°C T_A and 135°C T_J
2. Specifications for Commercial and Industrial grade devices can be found in the [ProASIC3 Flash Family FPGAs handbook](#).

Contact your local Actel representative for device availability:

<http://www.actel.com/contact/default.aspx>.

[查询"A3P060-1FGG144T"供应商](#)

1 – Automotive ProASIC3 Device Family Overview

General Description

Automotive ProASIC3 nonvolatile flash technology gives automotive system designers the advantage of a secure, low-power, single-chip solution that is live at power-up (LAPU). Automotive ProASIC3 is reprogrammable and offers time-to-market benefits at an ASIC-level unit cost. These features enable designers to create high-density systems using existing ASIC or FPGA design flows and tools.

Automotive ProASIC3 devices offer 1 kbit of on-chip, reprogrammable, nonvolatile FlashROM storage as well as clock conditioning circuitry based on an integrated phase-locked loop (PLL). Automotive ProASIC3 devices have up to 1 million system gates, supported with up to 144 kbits of SRAM and up to 300 user I/Os.

Automotive ProASIC3 devices are the only firm-error-immune automotive grade FPGAs. Firm-error immunity makes them ideally suited for demanding applications in powertrain, safety, and telematics-based subsystems, where firm-error failure is not an option.

Firm errors in SRAM-based FPGAs can result in high defect levels in field-deployed systems. These unavoidable defects must be considered separately from standard defects and failure mechanisms when looking at overall system quality and reliability.

Flash Advantages

Reduced Cost of Ownership

Advantages to the designer extend beyond low unit cost, performance, and ease of use. Unlike SRAM-based FPGAs, flash-based Automotive ProASIC3 devices allow all functionality to be live at power-up; no external boot PROM is required. On-board security mechanisms prevent access to all the programming information and enable secure remote updates of the FPGA logic. Flash-based FPGAs are LAPU Class 0 devices, offering the lowest available power in a single-chip device and providing firm-error immunity. The Automotive ProASIC3 family device architecture mitigates the need for ASIC migration at high user volumes. This makes the Automotive ProASIC3 family a cost-effective ASIC replacement solution, especially for automotive applications.

Security

The nonvolatile, flash-based Automotive ProASIC3 devices do not require a boot PROM, so there is no vulnerable external bitstream that can be easily copied. Automotive ProASIC3 devices incorporate FlashLock, which provides a unique combination of reprogrammability and design security without external overhead, advantages that only an FPGA with nonvolatile flash programming can offer.

Automotive ProASIC3 devices utilize a 128-bit flash-based lock and a separate AES key to secure programmed intellectual property and configuration data. In addition, all FlashROM data in Automotive ProASIC3 devices can be encrypted prior to loading, using the industry-leading AES-128 (FIPS192) bit block cipher encryption standard. The AES was adopted by the National Institute of Standards and Technology (NIST) in 2000 and replaces the 1977 DES standard. Automotive ProASIC3 devices have a built-in AES decryption engine and a flash-based AES key that make them the most comprehensive programmable logic device security solution available today. Automotive ProASIC3 devices with AES-based security allow for secure, remote field updates over public networks such as the Internet, and ensure that valuable IP remains out of the hands of system overbuilders, system cloners, and IP thieves. The contents of a programmed Automotive ProASIC3 device cannot be read back, although secure design verification is possible. Additionally, security features of Automotive ProASIC3 devices provide anti-tampering protection.

Security, built into the FPGA fabric, is an inherent component of the Automotive ProASIC3 family. The flash cells are located beneath seven metal layers, and many device design and layout

techniques have been used to make invasive attacks extremely difficult. The Automotive ProASIC3 family, with FlashLock and AES security, is unique in being highly resistant to both invasive and noninvasive attacks. Your valuable IP is protected and secure. An Automotive ProASIC3 device provides the most impenetrable security for programmable logic designs.

Single Chip

Flash-based FPGAs store their configuration information in on-chip flash cells. Once programmed, the configuration data is an inherent part of the FPGA structure, and no external configuration data needs to be loaded at system power-up (unlike SRAM-based FPGAs). Therefore, flash-based Automotive ProASIC3 FPGAs do not require system configuration components such as EEPROMs or microcontrollers to load device configuration data. This reduces bill-of-materials costs and PCB area, and increases security and system reliability.

Live at Power-Up

The Actel flash-based Automotive ProASIC3 devices support Level 0 of the LAPU classification standard. This feature helps in system component initialization, execution of critical tasks before the processor wakes up, setup and configuration of memory blocks, clock generation, and bus activity management. The LAPU feature of flash-based Automotive ProASIC3 devices greatly simplifies total system design and reduces total system cost, often eliminating the need for CPLDs and external clock generation PLLs. In addition, glitches and brownouts in system power will not corrupt the Automotive ProASIC3 device's flash configuration, and unlike SRAM-based FPGAs, the device will not have to be reloaded when system power is restored. This enables the reduction or complete removal of the configuration PROM, expensive voltage monitor, brownout detection, and clock generator devices from the PCB design. Flash-based Automotive ProASIC3 devices simplify total system design and reduce cost and design risk while increasing system reliability and improving system initialization time.

Firm-Error Immunity

Firm errors occur most commonly when high-energy neutrons, generated in the upper atmosphere, strike a configuration cell of an SRAM FPGA. The energy of the collision can change the state of the configuration cell and thus change the logic, routing, or I/O behavior in an unpredictable way. These errors are impossible to prevent in SRAM FPGAs. The consequence of this type of error can be a complete system failure. Firm errors do not exist in the configuration memory of Automotive ProASIC3 flash-based FPGAs. Once it is programmed, the flash cell configuration element of Automotive ProASIC3 FPGAs cannot be altered by high-energy neutrons and is therefore immune to them. Recoverable (or soft) errors occur in the user data SRAM of all FPGA devices. These can easily be mitigated by using error detection and correction (EDAC) circuitry built into the FPGA fabric.

Low Power

Flash-based Automotive ProASIC3 devices exhibit very low power characteristics, similar to those of an ASIC, making them an ideal choice for power-sensitive applications. Automotive ProASIC3 devices have only a very limited power-on current surge and no high-current transition period, both of which occur on many FPGAs.

Automotive ProASIC3 devices also have low dynamic power consumption to further maximize power savings.

Advanced Flash Technology

The Automotive ProASIC3 family offers many benefits, including nonvolatility and reprogrammability, through an advanced flash-based, 130-nm LVC MOS process with seven layers of metal. Standard CMOS design techniques are used to implement logic and control functions. The combination of fine granularity, enhanced flexible routing resources, and abundant flash switches allows for very high logic utilization without compromising device routability or performance. Logic functions within the device are interconnected through a four-level routing hierarchy.

Advanced Architecture

The proprietary Automotive ProASIC3 architecture provides granularity comparable to standard-cell ASICs. The Automotive ProASIC3 device consists of five distinct and programmable architectural features ([Figure 1-1 on page 1-4](#) and [Figure 1-2 on page 1-4](#)):

- FPGA VersaTiles
- Dedicated FlashROM
- Dedicated SRAM memory
- Extensive CCCs and PLLs
- Advanced I/O structure

The FPGA core consists of a sea of VersaTiles. Each VersaTile can be configured as a three-input logic function, a D-flip-flop (with or without enable), or a latch by programming the appropriate flash switch interconnections. The versatility of the Automotive ProASIC3 core tile as either a three-input lookup table (LUT) equivalent or a D-flip-flop/latch with enable allows for efficient use of the FPGA fabric. The VersaTile capability is unique to the Actel ProASIC family of third-generation-architecture flash FPGAs. VersaTiles are connected with any of the four levels of routing hierarchy. Flash switches are distributed throughout the device to provide nonvolatile, reconfigurable interconnect programming. Maximum core utilization is possible for virtually any design.

In addition, extensive on-chip programming circuitry allows for rapid, single-voltage (3.3 V) programming of Automotive ProASIC3 devices via an IEEE 1532 JTAG interface.

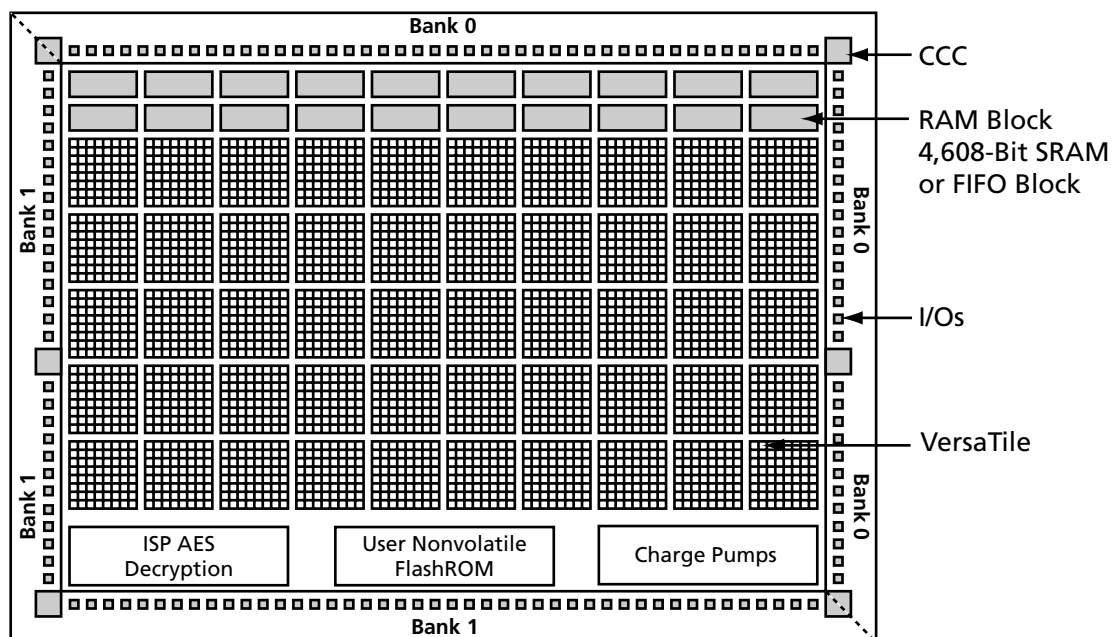


Figure 1-1 • Automotive ProASIC3 Device Architecture Overview with Two I/O Banks (A3P060 and A3P125)

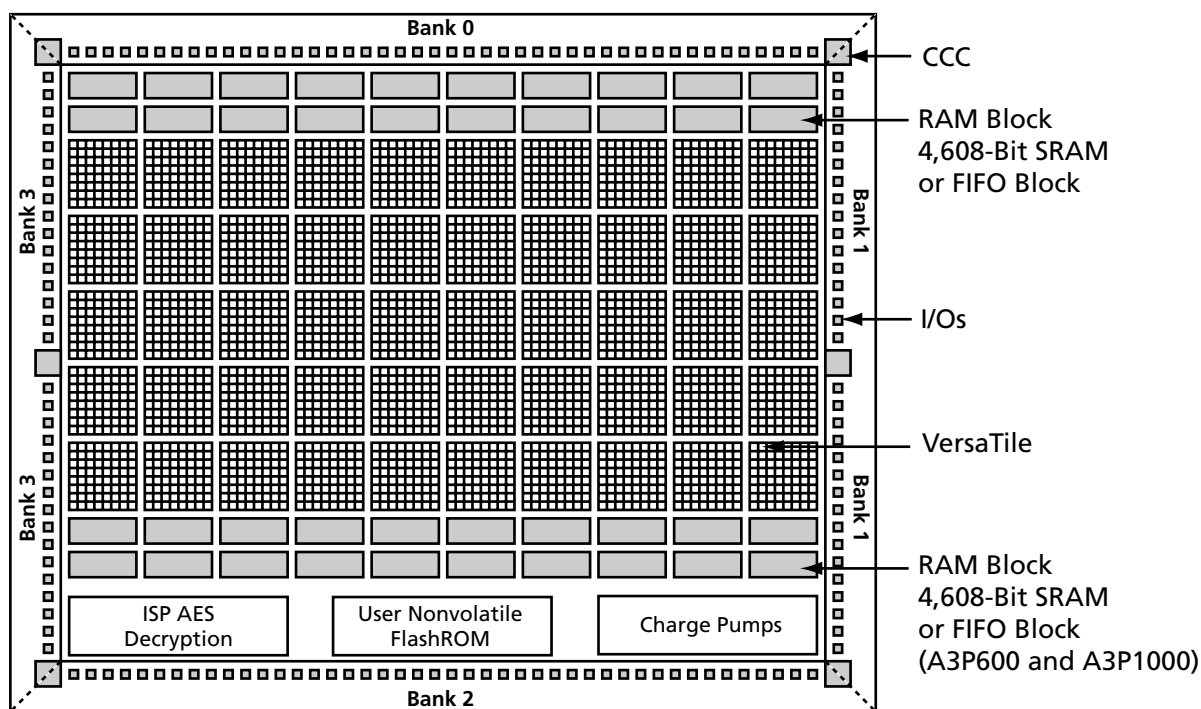


Figure 1-2 • Automotive ProASIC3 Device Architecture Overview with Four I/O Banks (A3P600 and A3P1000)

VersaTiles

The Automotive ProASIC3 core consists of VersaTiles, which have been enhanced beyond the ProASIC^{PLUS}® core tiles. The Automotive ProASIC3 VersaTile supports the following:

- All 3-input logic functions—LUT-3 equivalent
- Latch with clear or set
- D-flip-flop with clear or set
- Enable D-flip-flop with clear or set

Refer to [Figure 1-3](#) for VersaTile configurations.

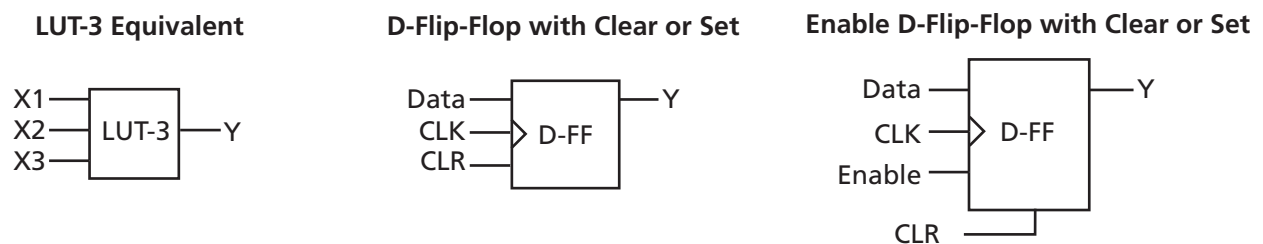


Figure 1-3 • VersaTile Configurations

User Nonvolatile FlashROM

Actel Automotive ProASIC3 devices have 1 kbit of on-chip, user-accessible, nonvolatile FlashROM. The FlashROM can be used in diverse system applications:

- Unique protocol addressing (wireless or fixed)
- System calibration settings
- Device serialization and/or inventory control
- Subscription-based business models (for example, infotainment systems)
- Secure key storage for secure communications algorithms
- Asset management/tracking
- Date stamping
- Version management

The FlashROM is written using the standard Automotive ProASIC3 IEEE 1532 JTAG programming interface.

The FlashROM can be programmed via the JTAG programming interface, and its contents can be read back either through the JTAG programming interface or via direct FPGA core addressing. Note that the FlashROM can only be programmed from the JTAG interface and cannot be programmed from the internal logic array.

The FlashROM is programmed as 8 banks of 128 bits; however, reading is performed on a byte-by-byte basis using a synchronous interface. A 7-bit address from the FPGA core defines which of the 8 banks and which of the 16 bytes within that bank are being read. The three most significant bits (MSBs) of the FlashROM address determine the bank, and the four least significant bits (LSBs) of the FlashROM address define the byte.

The Actel Automotive ProASIC3 development software solutions, Libero® Integrated Design Environment (IDE) and Designer, have extensive support for the FlashROM. One such feature is auto-generation of sequential programming files for applications requiring a unique serial number in each part. Another feature allows the inclusion of static data for system version control. Data for the FlashROM can be generated quickly and easily using Actel Libero IDE and Designer software tools. Comprehensive programming file support is also included to allow for easy programming of large numbers of parts with differing FlashROM contents.

SRAM

Automotive ProASIC3 devices have embedded SRAM blocks along their north and south sides. Each variable-aspect-ratio SRAM block is 4,608 bits in size. Available memory configurations are 256×18, 512×9, 1k×4, 2k×2, and 4k×1 bits. The individual blocks have independent read and write ports that can be configured with different bit widths on each port. For example, data can be sent through a 4-bit port and read as a single bitstream. The embedded SRAM blocks can be initialized via the device JTAG port (ROM emulation mode) using the UJTAG macro.

PLL and CCC

Automotive ProASIC3 devices provide designers with very flexible clock conditioning circuit (CCC) capabilities. Each member of the Automotive ProASIC3 family contains six CCCs. One CCC (center west side) has a PLL.

The six CCC blocks are located at the four corners and the centers of the east and west sides. One CCC (center west side) has a PLL.

All six CCC blocks are usable; the four corner CCCs and the east CCC allow simple clock delay operations as well as clock spine access.

The inputs of the six CCC blocks are accessible from the FPGA core or from one of several inputs located near the CCC that have dedicated connections to the CCC block.

The CCC block has these key features:

- Wide input frequency range (f_{IN_CCC}) = 1.5 MHz to 350 MHz
- Output frequency range (f_{OUT_CCC}) = 0.75 MHz to 350 MHz
- Clock delay adjustment via programmable and fixed delays from –7.56 ns to +11.12 ns
- 2 programmable delay types for clock skew minimization
- Clock frequency synthesis (for PLL only)

Additional CCC specifications:

- Internal phase shift = 0°, 90°, 180°, and 270°. Output phase shift depends on the output divider configuration (for PLL only).
- Output duty cycle = 50% ± 1.5% or better (for PLL only)
- Low output jitter: worst case < 2.5% × clock period peak-to-peak period jitter when single global network used (for PLL only)
- Maximum acquisition time is 300 μs (for PLL only)
- Low power consumption of 5 mW
- Exceptional tolerance to input period jitter— allowable input jitter is up to 1.5 ns (for PLL only)
- Four precise phases; maximum misalignment between adjacent phases of 40 ps × 350 MHz / f_{OUT_CCC} (for PLL only)

Global Clocking

Automotive ProASIC3 devices have extensive support for multiple clocking domains. In addition to the CCC and PLL support described above, there is a comprehensive global clock distribution network.

Each VersaTile input and output port has access to nine VersaNets: six chip (main) and three quadrant global networks. The VersaNets can be driven by the CCC or directly accessed from the core via multiplexers (MUXes). The VersaNets can be used to distribute low-skew clock signals or for rapid distribution of high-fanout nets.

I/Os with Advanced I/O Standards

The Automotive ProASIC3 family of FPGAs features a flexible I/O structure, supporting a range of voltages (1.5 V, 1.8 V, 2.5 V, and 3.3 V). Automotive ProASIC3 FPGAs support many different I/O standards—single-ended and differential.

The I/Os are organized into banks, with two or four banks per device. The configuration of these banks determines the I/O standards supported.

Each I/O module contains several input, output, and enable registers. These registers allow the implementation of the following:

- Single-Data-Rate applications
- Double-Data-Rate applications—DDR LVDS, B-LVDS, and M-LVDS I/Os for point-to-point communications

Automotive ProASIC3 banks for the A3P250 and A3P1000 devices support LVPECL, LVDS, B-LVDS, and M-LVDS. B-LVDS and M-LVDS can support up to 20 loads.

Part Number and Revision Date

Part Number 51700099-001-0

Revised January 2008

Datasheet Categories

Categories

In order to provide the latest information to designers, some datasheets are published before data has been fully characterized. Datasheets are designated as "Product Brief," "Advance," "Preliminary," and "Production." The definition of these categories are as follows:

Product Brief

The product brief is a summarized version of a datasheet (advance or production) and contains general product information. This document gives an overview of specific device and family information.

Advance

This version contains initial estimated information based on simulation, other products, devices, or speed grades. This information can be used as estimates, but not for production. This label only applies to the DC and Switching Characteristics chapter of the datasheet and will only be used when the data has not been fully characterized.

Preliminary

The datasheet contains information based on simulation and/or initial characterization. The information is believed to be correct, but changes are possible.

Unmarked (production)

This version contains information that is considered to be final.

Export Administration Regulations (EAR)

The products described in this document are subject to the Export Administration Regulations (EAR). They could require an approved export license prior to export from the United States. An export includes release of product or disclosure of technology to a foreign national inside or outside the United States.

Actel Safety Critical, Life Support, and High-Reliability Applications Policy

The Actel products described in this advance status document may not have completed Actel's qualification process. Actel may amend or enhance products during the product introduction and qualification process, resulting in changes in device functionality or performance. It is the responsibility of each customer to ensure the fitness of any Actel product (but especially a new product) for a particular purpose, including appropriateness for safety-critical, life-support, and other high-reliability applications. Consult Actel's Terms and Conditions for specific liability exclusions relating to life-support applications. A reliability report covering all of Actel's products is available on the Actel website at http://www.actel.com/documents/ORT_Report.pdf. Actel also offers a variety of enhanced qualification and lot acceptance screening procedures. Contact your local Actel sales office for additional reliability information.



2 – Automotive ProASIC3 DC and Switching Characteristics

General Specifications

Operating Conditions

Stresses beyond those listed in [Table 2-1](#) may cause permanent damage to the device.

Exposure to absolute maximum rating conditions for extended periods may affect device reliability. Absolute Maximums are stress ratings only; functional operation of the device at these or any other conditions beyond those listed under the Recommended Operating Conditions specified in [Table 2-2 on page 2-2](#) is not implied.

Table 2-1 • Absolute Maximum Ratings

Symbol	Parameter	Limits	Units
V _{CC}	DC core supply voltage	–0.3 to 1.65	V
V _{JTAG}	JTAG DC voltage	–0.3 to 3.75	V
V _{PUMP}	Programming voltage	–0.3 to 3.75	V
V _{CCPLL}	Analog power supply (PLL)	–0.3 to 1.65	V
V _{CCI}	DC I/O output buffer supply voltage	–0.3 to 3.75	V
VMV	DC I/O input buffer supply voltage	–0.3 to 3.75	V
VI	I/O input voltage	–0.3 V to 3.6 V (when I/O hot insertion mode is enabled) –0.3 V to (V _{CCI} + 1 V) or 3.6 V, whichever voltage is lower (when I/O hot-insertion mode is disabled)	V
T _{STG} ²	Storage temperature	–65 to +150	°C
T _J ²	Junction temperature	+150	°C

Notes:

1. The device should be operated within the limits specified by the datasheet. During transitions, the input signal may undershoot or overshoot according to the limits shown in [Table 2-3 on page 2-3](#).
2. For flash programming and retention maximum limits, refer to [Figure 2-1 on page 2-2](#). For recommended operating limits, refer to [Table 2-2 on page 2-2](#).

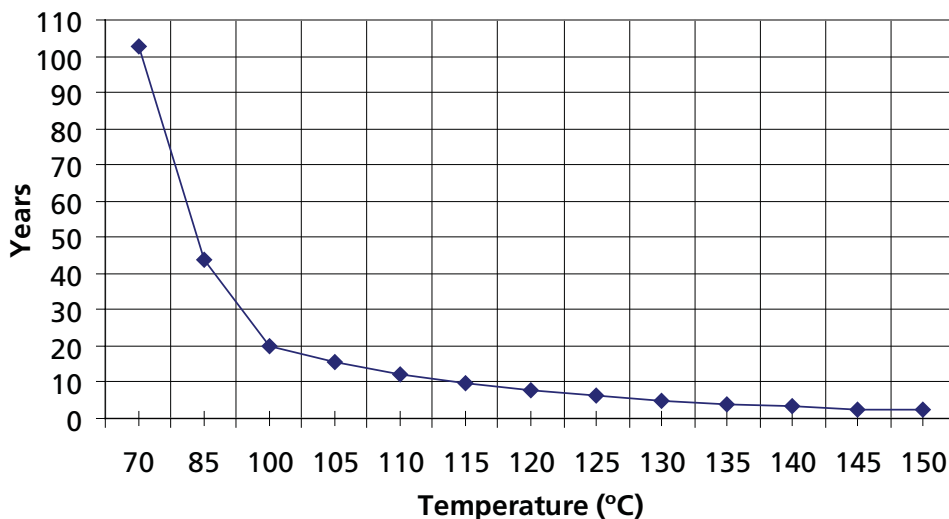
Table 2-2 • Recommended Operating Conditions

Symbol	Parameter	Automotive Grade 1	Automotive Grade 2	Units
T_J	Junction temperature	–40 to +135	–40 to +115	°C
V_{CC}	1.5 V DC core supply voltage	1.425 to 1.575	1.425 to 1.575	V
V_{JTAG}	JTAG DC voltage	1.4 to 3.6	1.4 to 3.6	V
V_{PUMP}	Programming voltage	3.0 to 3.6	3.0 to 3.6	V
	Operation ³	0 to 3.6	0 to 3.6	V
V_{CCPLL}	Analog power supply (PLL)	1.4 to 1.6	1.4 to 1.6	V
V_{CCI} and VMV	1.5 V DC supply voltage	1.425 to 1.575	1.425 to 1.575	V
	1.8 V DC supply voltage	1.7 to 1.9	1.7 to 1.9	V
	2.5 V DC supply voltage	2.3 to 2.7	2.3 to 2.7	V
	3.3 V DC supply voltage	3.0 to 3.6	3.0 to 3.6	V
	LVDS/B-LVDS/M-LVDS differential I/O	2.375 to 2.625	2.375 to 2.625	V
	LVPECL differential I/O	3.0 to 3.6	3.0 to 3.6	V

Notes:

1. The ranges given here are for power supplies only. The recommended input voltage ranges specific to each I/O standard are given in Table 2-14 on page 2-16. VMV and V_{CCI} should be at the same voltage within a given I/O bank.
2. All parameters representing voltages are measured with respect to GND unless otherwise specified.
3. V_{PUMP} can be left floating during operation (not programming mode).

T_J (°C)	HTR Lifetime (yrs)
70	102.7
85	43.8
100	20.0
105	15.6
110	12.3
115	9.7
120	7.7
125	6.2
130	5.0
135	4.0
140	3.3
145	2.7
150	2.2



Note: HTR time is the period during which you would not expect a verify failure due to flash cell leakage.

Figure 2-1 • High-Temperature Data Retention (HTR)

Table 2-3 • Overshoot and Undershoot Limits (as measured on quiet I/Os)

V _{CCI} and VMV	Average V _{CCI} -GND Overshoot or Undershoot Duration as a Percentage of Clock Cycle	Maximum Overshoot/Undershoot (115°C)	Maximum Overshoot/Undershoot (135°C)
2.7 V or less	10%	0.81 V	0.72 V
	5%	0.90 V	0.82 V
3 V	10%	0.80 V	0.72 V
	5%	0.90 V	0.81 V
3.3 V	10%	0.79 V	0.69 V
	5%	0.88 V	0.79 V
3.6 V	10%	N/A	N/A
	5%	N/A	N/A

Notes:

1. The duration is allowed at one out of six clock cycles (estimated SSO density over cycles). If the overshoot/undershoot occurs at one out of two cycles, the maximum overshoot/undershoot has to be reduced by 0.15 V.
2. This table refers only to overshoot/undershoot limits for simultaneously switching I/Os and does not provide PCI overshoot/undershoot limits.

I/O Power-Up and Supply Voltage Thresholds for Power-On Reset (Commercial and Industrial)

Sophisticated power-up management circuitry is designed into every ProASIC®3 device. These circuits ensure easy transition from the powered-off state to the powered-up state of the device. The many different supplies can power up in any sequence with minimized current spikes or surges. In addition, the I/O will be in a known state through the power-up sequence. The basic principle is shown in [Figure 2-2 on page 2-4](#).

There are five regions to consider during power-up.

ProASIC3 I/Os are activated only if ALL of the following three conditions are met:

1. V_{CC} and V_{CCI} are above the minimum specified trip points ([Figure 2-2 on page 2-4](#)).
2. V_{CCI} > V_{CC} – 0.75 V (typical)
3. Chip is in the operating mode.

V_{CCI} Trip Point:

Ramping up: 0.6 V < trip_point_up < 1.2 V

Ramping down: 0.5 V < trip_point_down < 1.1 V

V_{CC} Trip Point:

Ramping up: 0.6 V < trip_point_up < 1.1 V

Ramping down: 0.5 V < trip_point_down < 1 V

V_{CC} and V_{CCI} ramp-up trip points are about 100 mV higher than ramp-down trip points. This specifically built-in hysteresis prevents undesirable power-up oscillations and current surges. Note the following:

- During programming, I/Os become tristated and weakly pulled up to V_{CCI}.
- JTAG supply, PLL power supplies, and charge pump V_{PUMP} supply have no influence on I/O behavior.

Internal Power-Up Activation Sequence

1. Core
2. Input buffers
3. Output buffers, after 200 ns delay from input buffer activation

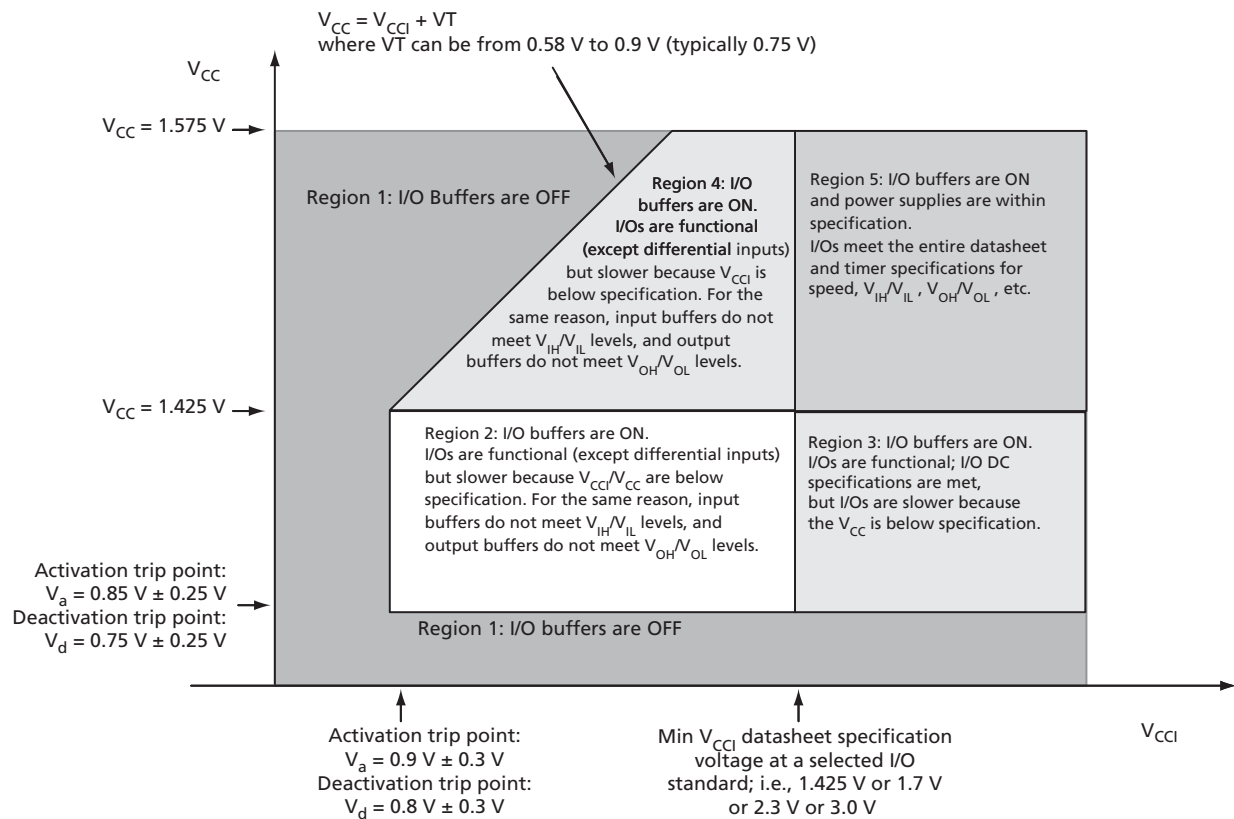


Figure 2-2 • I/O State as a Function of V_{CCI} and V_{CC} Voltage Levels

Thermal Characteristics

Introduction

The temperature variable in the Actel Designer software refers to the junction temperature, not the ambient temperature. This is an important distinction because dynamic and static power consumption cause the chip junction to be higher than the ambient temperature.

EQ 2-1 can be used to calculate junction temperature.

$$T_J = \text{Junction Temperature} = \Delta T + T_A$$

EQ 2-1

where:

T_A = Ambient Temperature

ΔT = Temperature gradient between junction (silicon) and ambient $\Delta T = \theta_{ja} * P$

θ_{ja} = Junction-to-ambient of the package. θ_{ja} numbers are located in Table 2-4 on page 2-5.

P = Power dissipation

Package Thermal Characteristics

The device junction-to-case thermal resistivity is θ_{jc} and the junction-to-ambient air thermal resistivity is θ_{ja} . The thermal characteristics for θ_{ja} are shown for two air flow rates. The absolute maximum junction temperature is 110°C. EQ 2-2 shows a sample calculation of the absolute maximum power dissipation allowed for a 484-pin FBGA package at commercial temperature and in still air.

$$\text{Maximum Power Allowed} = \frac{\text{Max. junction temp. (°C)} - \text{Max. ambient temp. (°C)}}{\theta_{ja}(\text{°C/W})} = \frac{110^{\circ}\text{C} - 70^{\circ}\text{C}}{20.5^{\circ}\text{C/W}} = 1.951 \text{ W}$$

EQ 2-2

Table 2-4 • Package Thermal Resistivities

Package Type	Device	Pin Count	θ_{jc}	θ_{ja}			Units
				Still Air	200 ft./min.	500 ft./min.	
Very Thin Quad Flat Pack (VQFP)	All devices	100	10.0	35.3	29.4	27.1	°C/W
Fine Pitch Ball Grid Array (FBGA)	See note*	144	3.8	26.9	22.9	21.5	°C/W
	See note*	256	3.8	26.6	22.8	21.5	°C/W
	See note*	484	3.2	20.5	17.0	15.9	°C/W
	A3P1000	144	6.3	31.6	26.2	24.2	°C/W
	A3P1000	256	6.6	28.1	24.4	22.7	°C/W
	A3P1000	484	8.0	23.3	19.0	16.7	°C/W

* This information applies to all ProASIC3 devices except the A3P1000. Detailed device/package thermal information will be available in future revisions of the datasheet.

Temperature and Voltage Derating Factors

Table 2-5 • Temperature and Voltage Derating Factors for Timing Delays
(normalized to $T_J = 115^{\circ}\text{C}$, $V_{CC} = 1.425 \text{ V}$)

Array Voltage V_{CC} (V)	−40°C	0°C	25°C	70°C	85°C	115°C	125°C	135°C
1.425	0.83	0.88	0.90	0.95	0.97	1.00	1.01	1.02
1.5	0.79	0.83	0.85	0.90	0.92	0.95	0.96	0.97
1.575	0.76	0.80	0.82	0.87	0.88	0.91	0.93	0.94

Calculating Power Dissipation

Quiescent Supply Current

Table 2-6 • Quiescent Supply Current Characteristics

	A3P060	A3P125	A3P250	A3P1000
Typical (25°C)	2 mA	2 mA	3 mA	8 mA
Maximum (Automotive Grade 1) – 135°C	53 mA	53 mA	106 mA	265 mA
Maximum (Automotive Grade 2) – 115°C	26 mA	26 mA	53 mA	131 mA

Note: I_{DD} includes V_{CC} , V_{PUMP} , V_{CC1} , and VMV currents. Values do not include I/O static contribution, which is shown in Table 2-7 and Table 2-10 on page 2-8.

Power per I/O Pin

Table 2-7 • Summary of I/O Input Buffer Power (per pin) – Default I/O Software Settings¹
Applicable to Advanced I/O Banks

	VMV (V)	Static Power P_{DC2} (mW) ¹	Dynamic Power P_{AC9} (μW/MHz) ²
Single-Ended			
3.3 V LVTTTL / 3.3 V LVCMOS	3.3	–	16.69
2.5 V LVCMOS	2.5	–	5.12
1.8 V LVCMOS	1.8	–	2.13
1.5 V LVCMOS (JESD8-11)	1.5	–	1.45
3.3 V PCI	3.3	–	18.11
3.3 V PCI-X	3.3	–	18.11
Differential			
LVDS	2.5	2.26	1.20
LVPECL	3.3	5.72	1.87

Notes:

1. P_{DC2} is the static power (where applicable) measured on VMV.
2. P_{AC9} is the total dynamic power measured on V_{CC} and VMV.

Table 2-8 • Summary of I/O Input Buffer Power (per pin) – Default I/O Software Settings¹
Applicable to Standard Plus I/O Banks

	VMV (V)	Static Power P_{DC2} (mW) ¹	Dynamic Power P_{AC9} (μW/MHz) ²
Single-Ended			
3.3 V LVTTTL / 3.3 V LVCMOS	3.3	–	16.72
2.5 V LVCMOS	2.5	–	5.14
1.8 V LVCMOS	1.8	–	2.13
1.5 V LVCMOS (JESD8-11)	1.5	–	1.48
3.3 V PCI	3.3	–	18.13
3.3 V PCI-X	3.3	–	18.13

Notes:

1. P_{DC2} is the static power (where applicable) measured on VMV.
2. P_{AC9} is the total dynamic power measured on V_{CC} and VMV.

Table 2-9 • Summary of I/O Output Buffer Power (per pin) – Default I/O Software Settings¹
Applicable to Advanced I/O Banks

	C_{LOAD} (pF)	V_{CCI} (V)	Static Power P_{DC3} (mW) ²	Dynamic Power P_{AC10} (μW/MHz) ³
Single-Ended				
3.3 V LVTTTL / 3.3 V LVCMOS	35	3.3	–	468.67
2.5 V LVCMOS	35	2.5	–	267.48
1.8 V LVCMOS	35	1.8	–	149.46
1.5 V LVCMOS (JESD8-11)	35	1.5	–	103.12
3.3 V PCI	10	3.3	–	201.02
3.3 V PCI-X	10	3.3	–	201.02
Differential				
LVDS	–	2.5	7.74	88.92
LVPECL	–	3.3	19.54	166.52

Notes:

1. Dynamic power consumption is given for standard load and software default drive strength and output slew.
2. P_{DC3} is the static power (where applicable) measured on VMV.
3. P_{AC10} is the total dynamic power measured on V_{CCI} and VMV.

Table 2-10 • Summary of I/O Output Buffer Power (per pin) – Default I/O Software Settings¹
Applicable to Standard Plus I/O Banks

	C_{LOAD} (pF)	V_{CCI} (V)	Static Power P_{DC3} (mW) ²	Dynamic Power P_{AC10} (μW/MHz) ³
Single-Ended				
3.3 V LVTTTL / 3.3 V LVCMOS	35	3.3	–	452.67
2.5 V LVCMOS	35	2.5	–	258.32
1.8 V LVCMOS	35	1.8	–	133.59
1.5 V LVCMOS (JESD8-11)	35	1.5	–	92.84
3.3 V PCI	10	3.3	–	184.92
3.3 V PCI-X	10	3.3	–	184.92

Notes:

1. Dynamic power consumption is given for standard load and software default drive strength and output slew.
2. P_{DC3} is the static power (where applicable) measured on VMV.
3. P_{AC10} is the total dynamic power measured on V_{CCI} and VMV.

Power Consumption of Various Internal Resources

Table 2-11 • Different Components Contributing to Dynamic Power Consumption in ProASIC3 Devices

Parameter	Definition	Device Specific Dynamic Power (μW/MHz)			
		A3P1000	A3P250	A3P125	A3P060
P _{AC1}	Clock contribution of a Global Rib	14.50	11.00	11.00	9.30
P _{AC2}	Clock contribution of a Global Spine	2.48	1.58	0.81	0.81
P _{AC3}	Clock contribution of a VersaTile row	0.81			
P _{AC4}	Clock contribution of a VersaTile used as a sequential module	0.12			
P _{AC5}	First contribution of a VersaTile used as a sequential module	0.07			
P _{AC6}	Second contribution of a VersaTile used as a sequential module	0.29			
P _{AC7}	Contribution of a VersaTile used as a combinatorial module	0.29			
P _{AC8}	Average contribution of a routing net	0.70			
P _{AC9}	Contribution of an I/O input pin (standard-dependent)	See Table 2-7 on page 2-6 .			
P _{AC10}	Contribution of an I/O output pin (standard-dependent)	See Table 2-7 and Table 2-10 on page 2-8 .			
P _{AC11}	Average contribution of a RAM block during a read operation	25.00			
P _{AC12}	Average contribution of a RAM block during a write operation	30.00			
P _{AC13}	Static PLL contribution	2.55 mW			
P _{AC14}	Dynamic contribution for PLL	2.60			

* For a different output load, drive strength, or slew rate, Actel recommends using the Actel power spreadsheet calculator or SmartPower tool in Actel Libero® Integrated Design Environment (IDE).

Power Calculation Methodology

This section describes a simplified method to estimate power consumption of an application. For more accurate and detailed power estimations, use the SmartPower tool in Actel Libero IDE software.

The power calculation methodology described below uses the following variables:

- The number of PLLs as well as the number and the frequency of each output clock generated
- The number of combinatorial and sequential cells used in the design
- The internal clock frequencies
- The number and the standard of I/O pins used in the design
- The number of RAM blocks used in the design
- Toggle rates of I/O pins as well as VersaTiles—guidelines are provided in [Table 2-12 on page 2-11](#).
- Enable rates of output buffers—guidelines are provided for typical applications in [Table 2-13 on page 2-12](#).
- Read rate and write rate to the memory—guidelines are provided for typical applications in [Table 2-13 on page 2-12](#). The calculation should be repeated for each clock domain defined in the design.

Methodology

Total Power Consumption— P_{TOTAL}

$$P_{TOTAL} = P_{STAT} + P_{DYN}$$

P_{STAT} is the total static power consumption.

P_{DYN} is the total dynamic power consumption.

Total Static Power Consumption— P_{STAT}

$$P_{STAT} = P_{DC1} + N_{INPUTS} * P_{DC2} + N_{OUTPUTS} * P_{DC3}$$

N_{INPUTS} is the number of I/O input buffers used in the design.

$N_{OUTPUTS}$ is the number of I/O output buffers used in the design.

Total Dynamic Power Consumption— P_{DYN}

$$P_{DYN} = P_{CLOCK} + P_{S-CELL} + P_{C-CELL} + P_{NET} + P_{INPUTS} + P_{OUTPUTS} + P_{MEMORY} + P_{PLL}$$

Global Clock Contribution— P_{CLOCK}

$$P_{CLOCK} = (P_{AC1} + N_{SPINE} * P_{AC2} + N_{ROW} * P_{AC3} + N_{S-CELL} * P_{AC4}) * F_{CLK}$$

N_{SPINE} is the number of global spines used in the user design—guidelines are provided in [Table 2-12 on page 2-11](#).

N_{ROW} is the number of VersaTile rows used in the design—guidelines are provided in [Table 2-12 on page 2-11](#).

F_{CLK} is the global clock signal frequency.

N_{S-CELL} is the number of VersaTiles used as sequential modules in the design.

P_{AC1} , P_{AC2} , P_{AC3} , and P_{AC4} are device-dependent.

Sequential Cells Contribution— P_{S-CELL}

$$P_{S-CELL} = N_{S-CELL} * (P_{AC5} + \alpha_1 / 2 * P_{AC6}) * F_{CLK}$$

N_{S-CELL} is the number of VersaTiles used as sequential modules in the design. When a multi-tile sequential cell is used, it should be accounted for as 1.

α_1 is the toggle rate of VersaTile outputs—guidelines are provided in [Table 2-12 on page 2-11](#).

F_{CLK} is the global clock signal frequency.

Combinatorial Cells Contribution— P_{C-CELL}

$$P_{C-CELL} = N_{C-CELL} * \alpha_1 / 2 * P_{AC7} * F_{CLK}$$

N_{C-CELL} is the number of VersaTiles used as combinatorial modules in the design.

α_1 is the toggle rate of VersaTile outputs—guidelines are provided in [Table 2-12 on page 2-11](#).

F_{CLK} is the global clock signal frequency.

Routing Net Contribution— P_{NET}

$$P_{NET} = (N_{S-CELL} + N_{C-CELL}) * \alpha_1 / 2 * P_{AC8} * F_{CLK}$$

N_{S-CELL} is the number VersaTiles used as sequential modules in the design.

N_{C-CELL} is the number of VersaTiles used as combinatorial modules in the design.

α_1 is the toggle rate of VersaTile outputs—guidelines are provided in [Table 2-12 on page 2-11](#).

F_{CLK} is the global clock signal frequency.

I/O Input Buffer Contribution— P_{INPUTS}

$$P_{INPUTS} = N_{INPUTS} * \alpha_2 / 2 * P_{AC9} * F_{CLK}$$

N_{INPUTS} is the number of I/O input buffers used in the design.

α_2 is the I/O buffer toggle rate—guidelines are provided in [Table 2-12 on page 2-11](#).

F_{CLK} is the global clock signal frequency.

I/O Output Buffer Contribution— P_{OUTPUTS}

$$P_{\text{OUTPUTS}} = N_{\text{OUTPUTS}} * \alpha_2 / 2 * \beta_1 * P_{\text{AC10}} * F_{\text{CLK}}$$

N_{OUTPUTS} is the number of I/O output buffers used in the design.

α_2 is the I/O buffer toggle rate—guidelines are provided in [Table 2-12](#).

β_1 is the I/O buffer enable rate—guidelines are provided in [Table 2-13](#) on page 2-12.

F_{CLK} is the global clock signal frequency.

RAM Contribution— P_{MEMORY}

$$P_{\text{MEMORY}} = P_{\text{AC11}} * N_{\text{BLOCKS}} * F_{\text{READ-CLOCK}} * \beta_2 + P_{\text{AC12}} * N_{\text{BLOCK}} * F_{\text{WRITE-CLOCK}} * \beta_3$$

N_{BLOCKS} is the number of RAM blocks used in the design.

$F_{\text{READ-CLOCK}}$ is the memory read clock frequency.

β_2 is the RAM enable rate for read operations.

$F_{\text{WRITE-CLOCK}}$ is the memory write clock frequency.

β_3 is the RAM enable rate for write operations—guidelines are provided in [Table 2-13](#) on page 2-12.

PLL Contribution— P_{PLL}

$$P_{\text{PLL}} = P_{\text{AC13}} + P_{\text{AC14}} * F_{\text{CLKOUT}}$$

F_{CLKIN} is the input clock frequency.

F_{CLKOUT} is the output clock frequency.¹

Guidelines

Toggle Rate Definition

A toggle rate defines the frequency of a net or logic element relative to a clock. It is a percentage. If the toggle rate of a net is 100%, this means that this net switches at half the clock frequency. Below are some examples:

- The average toggle rate of a shift register is 100% because all flip-flop outputs toggle at half of the clock frequency.
- The average toggle rate of an 8-bit counter is 25%:
 - Bit 0 (LSB) = 100%
 - Bit 1 = 50%
 - Bit 2 = 25%
 - ...
 - Bit 7 (MSB) = 0.78125%
 - Average toggle rate = (100% + 50% + 25% + 12.5% + . . . + 0.78125%) / 8

Enable Rate Definition

Output enable rate is the average percentage of time during which tristate outputs are enabled. When nontristate output buffers are used, the enable rate should be 100%.

Table 2-12 • Toggle Rate Guidelines Recommended for Power Calculation

Component	Definition	Guideline
α_1	Toggle rate of VersaTile outputs	10%
α_2	I/O buffer toggle rate	10%

1. The PLL dynamic contribution depends on the input clock frequency, the number of output clock signals generated by the PLL, and the frequency of each output clock. If a PLL is used to generate more than one output clock, include each output clock in the formula by adding its corresponding contribution ($P_{\text{AC14}} * F_{\text{CLKOUT}}$ product) to the total PLL contribution.

Table 2-13 • Enable Rate Guidelines Recommended for Power Calculation

Component	Definition	Guideline
β_1	I/O output buffer enable rate	100%
β_2	RAM enable rate for read operations	12.5%
β_3	RAM enable rate for write operations	12.5%

User I/O Characteristics

Timing Model

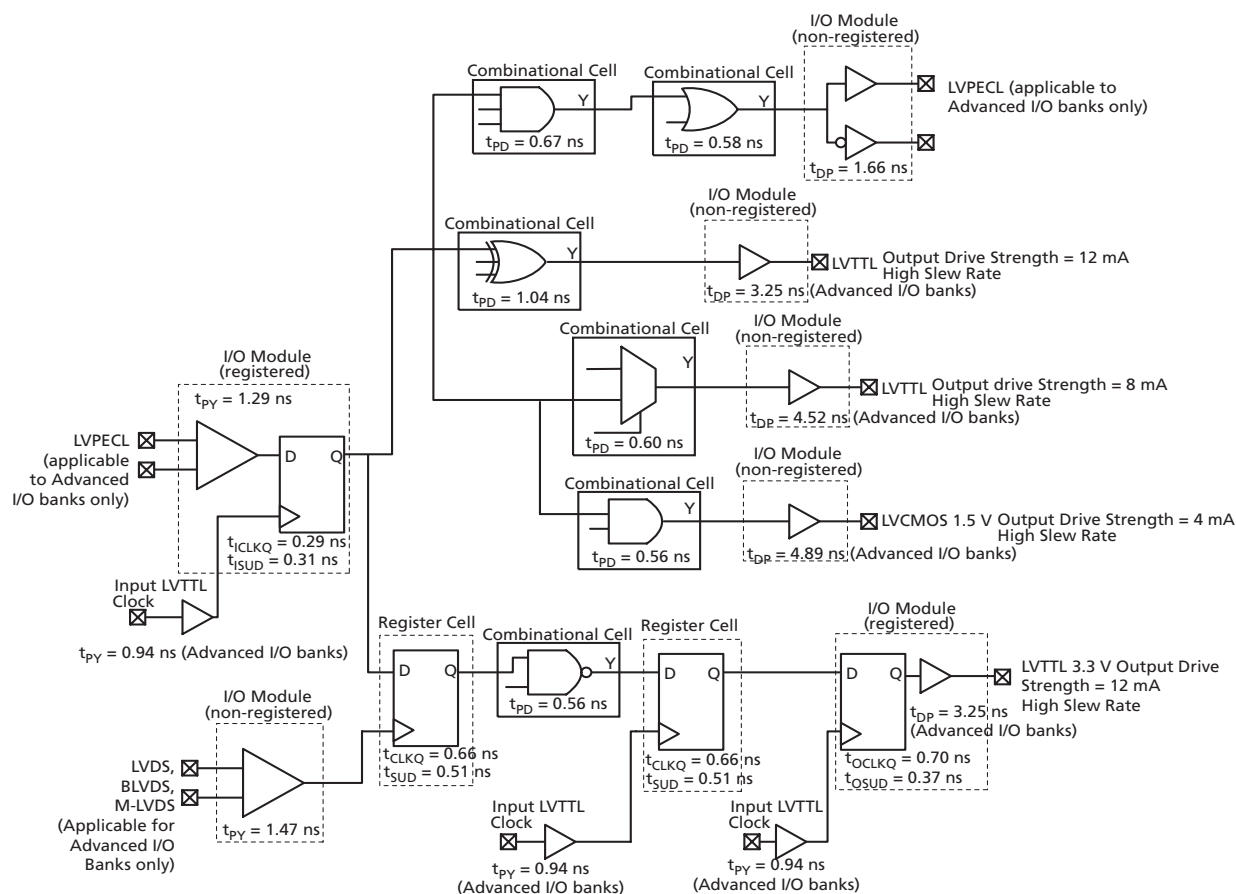


Figure 2-3 • Timing Model

Operating Conditions: -1 Speed, Automotive Grade 2 Temp. Range ($T_J = 115^\circ\text{C}$), Worst Case
 $V_{CC} = 1.425$ V

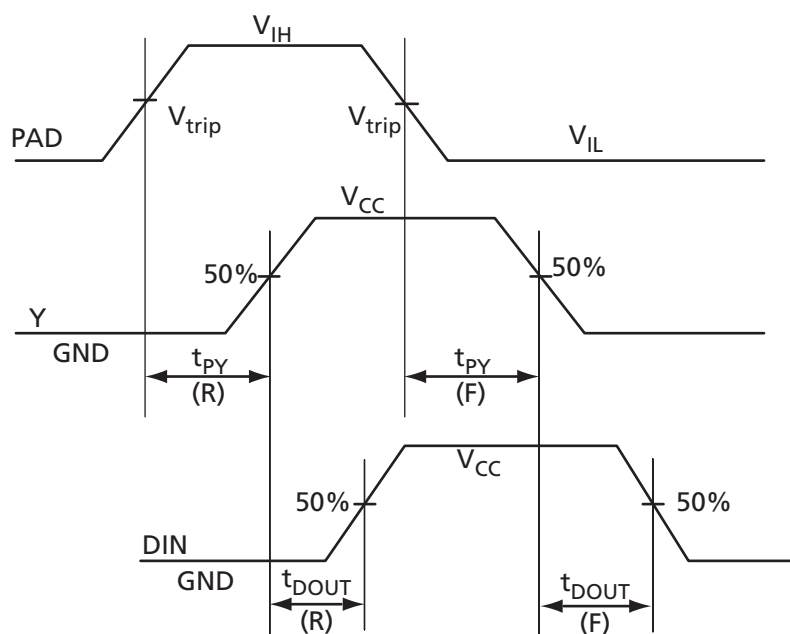
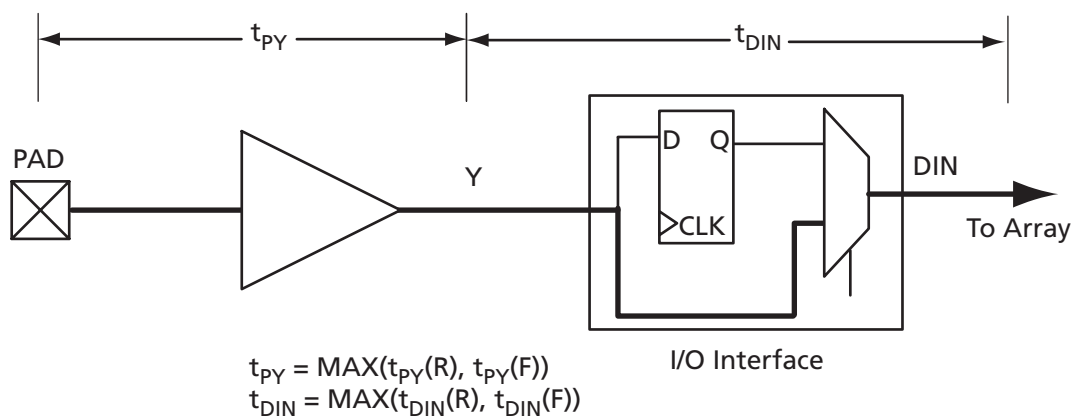


Figure 2-4 • Input Buffer Timing Model and Delays (example)

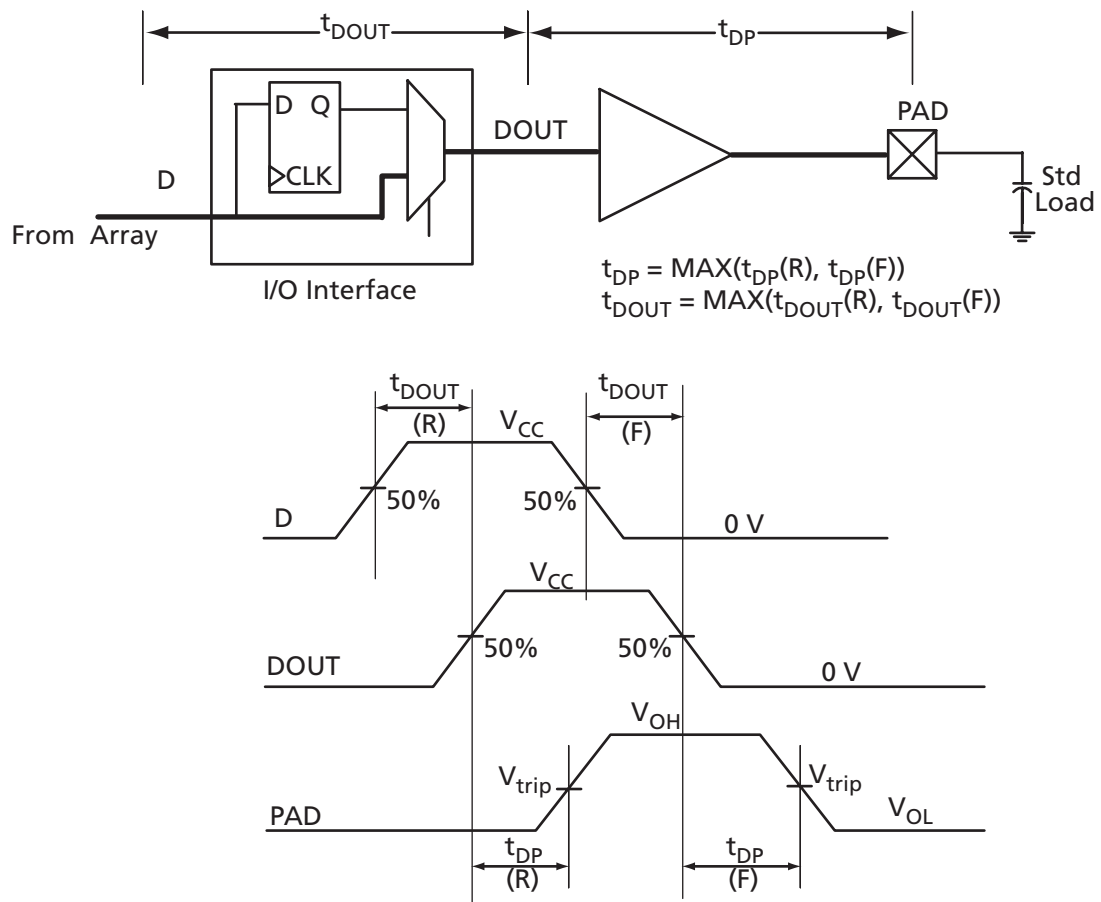
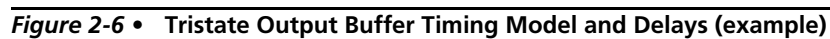


Figure 2-5 • Output Buffer Model and Delays (example)



Overview of I/O Performance

Summary of I/O DC Input and Output Levels – Default I/O Software Settings

Table 2-14 • Summary of Maximum and Minimum DC Input and Output Levels Applicable to Commercial and Industrial Conditions—Software Default Settings
Applicable to Advanced I/O Banks

I/O Standard	Drive Strength	Slew Rate	V _{IL}		V _{IH}		V _{OL}	V _{OH}	I _{OL}	I _{OH}
			Min, V	Max, V	Min, V	Max, V	Max, V	Min, V	mA	mA
3.3 V LVTTTL / 3.3 V LVCMOS	12 mA	High	–0.3	0.8	2	3.6	0.4	2.4	12	12
2.5 V LVCMOS	12 mA	High	–0.3	0.7	1.7	3.6	0.7	1.7	12	12
1.8 V LVCMOS	12 mA	High	–0.3	0.35 * V _{CCl}	0.65 * V _{CCl}	3.6	0.45	V _{CCl} – 0.45	12	12
1.5 V LVCMOS	12 mA	High	–0.3	0.30 * V _{CCl}	0.7 * V _{CCl}	3.6	0.25 * V _{CCl}	0.75 * V _{CCl}	12	12
3.3 V PCI	Per PCI specifications									
3.3 V PCI-X	Per PCI-X specifications									

Note: Currents are measured at 125°C junction temperature.

Table 2-15 • Summary of Maximum and Minimum DC Input and Output Levels Applicable to Commercial and Industrial Conditions—Software Default Settings
Applicable to Standard Plus I/O Banks

I/O Standard	Drive Strength	Slew Rate	V _{IL}		V _{IH}		V _{OL}	V _{OH}	I _{OL}	I _{OH}
			Min, V	Max, V	Min, V	Max, V	Max, V	Min, V	mA	mA
3.3 V LVTTTL / 3.3 V LVCMOS	12 mA	High	–0.3	0.8	2	3.6	0.4	2.4	12	12
2.5 V LVCMOS	12 mA	High	–0.3	0.7	1.7	3.6	0.7	1.7	12	12
1.8 V LVCMOS	8 mA	High	–0.3	0.35 * V _{CCl}	0.65 * V _{CCl}	3.6	0.45	V _{CCl} – 0.45	8	8
1.5 V LVCMOS	4 mA	High	–0.3	0.30 * V _{CCl}	0.7 * V _{CCl}	3.6	0.25 * V _{CCl}	0.75 * V _{CCl}	4	4
3.3 V PCI	Per PCI specifications									
3.3 V PCI-X	Per PCI-X specifications									

Note: Currents are measured at 125°C junction temperature.

Table 2-16 • Summary of Maximum and Minimum DC Input and Output Levels Applicable to Commercial and Industrial Conditions—Software Default Settings
Applicable to Standard I/O Banks

I/O Standard	Drive Strength	Slew Rate	V _{IL}		V _{IH}		V _{OL}	V _{OH}	I _{OL}	I _{OH}
			Min, V	Max, V	Min, V	Max, V	Max, V	Min, V	mA	mA
3.3 V LVTTTL / 3.3 V LVCMOS	8 mA	High	–0.3	0.8	2	3.6	0.4	2.4	8	8
2.5 V LVCMOS	8 mA	High	–0.3	0.7	1.7	3.6	0.7	1.7	8	8
1.8 V LVCMOS	4 mA	High	–0.3	0.35 * V _{CCl}	0.65 * V _{CCl}	3.6	0.45	V _{CCl} – 0.45	4	4
1.5 V LVCMOS	2 mA	High	–0.3	0.30 * V _{CCl}	0.7 * V _{CCl}	3.6	0.25 * V _{CCl}	0.75 * V _{CCl}	2	2

Note: Currents are measured at 125°C junction temperature.

Table 2-17 • Summary of Maximum and Minimum DC Input Levels Applicable to Automotive Grade 1 and Grade 2

DC I/O Standards	Automotive Grade 1 ¹		Automotive Grade 2 ²	
	I _{IL}	I _{IH}	I _{IL}	I _{IH}
	μA	μA	μA	μA
3.3 V LVTTTL / 3.3 V LVCMOS	10	10	15	15
2.5 V LVCMOS	10	10	15	15
1.8 V LVCMOS	10	10	15	15
1.5 V LVCMOS	10	10	15	15
3.3 V PCI	10	10	15	15
3.3 V PCI-X	10	10	15	15

Notes:

1. Automotive range Grade 1 ($-40^{\circ}\text{C} < T_J < 135^{\circ}\text{C}$)

2. Automotive range Grade 2 ($-40^{\circ}\text{C} < T_J < 115^{\circ}\text{C}$)

Summary of I/O Timing Characteristics – Default I/O Software Settings

Table 2-18 • Summary of AC Measuring Points

Standard	Measuring Trip Point (V _{trip})
3.3 V LVTTTL / 3.3 V LVCMOS	1.4 V
2.5 V LVCMOS	1.2 V
1.8 V LVCMOS	0.90 V
1.5 V LVCMOS	0.75 V
3.3 V PCI	0.285 * V _{CCI} (RR)
	0.615 * V _{CCI} (FF)
3.3 V PCI-X	0.285 * V _{CCI} (RR)
	0.615 * V _{CCI} (FF)

Table 2-19 • I/O AC Parameter Definitions

Parameter	Parameter Definition
t _{DP}	Data-to-Pad delay through the Output Buffer
t _{PY}	Pad-to-Data delay through the Input Buffer
t _{DOUT}	Data-to-Output Buffer delay through the I/O interface
t _{EOUT}	Enable-to-Output Buffer Tristate Control delay through the I/O interface
t _{DIN}	Input Buffer-to-Data delay through the I/O interface
t _{HZ}	Enable-to-Pad delay through the Output Buffer—HIGH to Z
t _{ZH}	Enable-to-Pad delay through the Output Buffer—Z to HIGH
t _{LZ}	Enable-to-Pad delay through the Output Buffer—LOW to Z
t _{ZL}	Enable-to-Pad delay through the Output Buffer—Z to LOW
t _{ZHS}	Enable-to-Pad delay through the Output Buffer with delayed enable—Z to HIGH
t _{ZLS}	Enable-to-Pad delay through the Output Buffer with delayed enable—Z to LOW

Table 2-20 • Summary of I/O Timing Characteristics—Software Default Settings
 –1 Speed Grade, Automotive-Case Conditions: $T_J = 115^{\circ}\text{C}$, Worst Case $V_{CC} = 1.425\text{ V}$, Worst Case $V_{CCI} = 3.0\text{ V}$
 Advanced I/O Banks

I/O Standard	Drive Strength (mA)	Slew Rate	Capacitive Load (pF)	External Resistor (Ω)	t_{DOUT} (ns)	t_{DP} (ns)	t_{DIN} (ns)	t_{PY} (ns)	t_{EOUT} (ns)	t_{ZL} (ns)	t_{ZH} (ns)	t_{LZ} (ns)	t_{HZ} (ns)	t_{ZLS} (ns)	t_{ZHS} (ns)	Units
3.3 V LVTTTL / 3.3 V LVCMOS	12 mA	High	35 pF	–	0.53	3.25	0.04	0.94	0.38	3.31	1.51	2.96	1.88	5.37	2.71	ns
2.5 V LVCMOS	12 mA	High	35 pF	–	0.53	3.28	0.04	1.19	0.38	3.34	3.16	1.77	1.80	5.39	5.22	ns
1.8 V LVCMOS	12 mA	High	35 pF	–	0.53	3.25	0.04	1.12	0.38	1.89	1.63	3.41	3.75	3.06	2.82	ns
1.5 V LVCMOS	12 mA	High	35 pF	–	0.53	3.75	0.04	1.32	0.38	2.18	1.91	3.63	3.87	3.35	3.11	ns
3.3 V PCI	Per PCI spec	High	10 pF	25^2	0.53	2.12	0.04	0.78	0.38	1.23	0.91	2.57	2.96	2.41	2.11	ns
3.3 V PCI-X	Per PCI-X spec	High	10 pF	25^2	0.53	2.47	0.04	0.77	0.38	1.23	0.91	2.57	2.96	2.41	2.11	ns
LVDS	24 mA	High	–	–	0.53	1.68	0.04	1.47	–	–	–	–	–	–	–	ns
LVPECL	24 mA	High	–	–	0.53	1.66	0.04	1.29	–	–	–	–	–	–	–	ns

Notes:

1. For specific junction temperature and voltage supply levels, refer to [Table 2-5 on page 2-5](#) for derating values.
2. Resistance is used to measure I/O propagation delays as defined in PCI specifications. See [Figure 2-11 on page 2-47](#) for connectivity. This resistor is not required during normal operation.

Table 2-21 • Summary of I/O Timing Characteristics—Software Default Settings
 –1 Speed Grade, Automotive-Case Conditions: $T_J = 115^{\circ}\text{C}$, Worst Case $V_{CC} = 1.425\text{ V}$, Worst Case $V_{CCI} = 3.0\text{ V}$
 Standard Plus I/O Banks

I/O Standard	Drive Strength (mA)	Slew Rate	Capacitive Load (pF)	External Resistor	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
3.3 V LVTTTL / 3.3 V LVCMOS	12 mA	High	35 pF	–	0.55	3.01	0.04	0.95	0.39	1.74	1.43	2.65	3.06	1.74	1.43	ns
2.5 V LVCMOS	12 mA	High	35 pF	–	0.55	3.05	0.04	1.23	0.39	3.11	2.99	1.56	1.69	5.23	5.11	ns
1.8 V LVCMOS	8 mA	High	35 pF	–	0.55	3.73	0.04	1.16	0.39	3.65	3.86	1.62	1.68	5.78	5.99	ns
1.5 V LVCMOS	4 mA	High	35 pF	–	0.55	4.60	0.04	1.35	0.39	4.61	5.05	2.07	1.85	6.74	7.18	ns
3.3 V PCI	Per PCI spec	High	10 pF	25^2	0.55	2.19	0.04	0.81	0.39	1.27	0.94	2.65	3.06	1.27	0.94	ns
3.3 V PCI-X	Per PCI-X spec	High	10 pF	25^2	0.55	2.19	0.04	0.79	0.39	1.27	0.94	2.65	3.06	1.27	0.94	ns

Notes:

1. For specific junction temperature and voltage supply levels, refer to [Table 2-5 on page 2-5](#) for derating values.
2. Resistance is used to measure I/O propagation delays as defined in PCI specifications. See [Figure 2-11 on page 2-47](#) for connectivity. This resistor is not required during normal operation.

Table 2-22 • Summary of I/O Timing Characteristics—Software Default Settings
 –1 Speed Grade, Automotive-Case Conditions: $T_J = 135^{\circ}\text{C}$, Worst Case $V_{CC} = 1.425\text{ V}$, Worst Case $V_{CCI} = 3.0\text{ V}$
 Advanced I/O Banks

I/O Standard	Drive Strength (mA)	Slew Rate	Capacitive Load (pF)	External Resistor (Ω)	t_{DOUT} (ns)	t_{DP} (ns)	t_{DIN} (ns)	t_{PY} (ns)	t_{EOUT} (ns)	t_{ZL} (ns)	t_{ZH} (ns)	t_{LZ} (ns)	t_{HZ} (ns)	t_{ZLS} (ns)	t_{ZHS} (ns)	Units
3.3 V LVTTTL / 3.3 V LVCMOS	12 mA	High	35 pF	–	0.55	3.36	0.04	0.97	0.39	3.42	1.56	3.05	1.94	5.55	2.80	ns
2.5 V LVCMOS	12 mA	High	35 pF	–	0.55	3.39	0.04	1.23	0.39	3.45	3.27	1.83	1.86	5.58	5.39	ns
1.8 V LVCMOS	12 mA	High	35 pF	–	0.55	3.36	0.04	1.16	0.39	1.95	1.68	3.52	3.88	3.16	2.92	ns
1.5 V LVCMOS	12 mA	High	35 pF	–	0.55	3.88	0.04	1.37	0.39	2.25	1.98	3.75	4.00	3.46	3.21	ns
3.3 V PCI	Per PCI spec	High	10 pF	25^2	0.55	2.19	0.04	0.81	0.39	1.27	0.94	2.65	3.06	2.49	2.18	ns
3.3 V PCI-X	Per PCI-X spec	High	10 pF	25^2	0.55	2.55	0.04	0.79	0.39	1.27	0.94	2.65	3.06	2.49	2.18	ns
LVDS	24 mA	High	–	–	0.55	1.74	0.04	1.52	–	–	–	–	–	–	–	ns
LVPECL	24 mA	High	–	–	0.55	1.71	0.04	1.34	–	–	–	–	–	–	–	ns

Notes:

1. For specific junction temperature and voltage supply levels, refer to [Table 2-5 on page 2-5](#) for derating values.
2. Resistance is used to measure I/O propagation delays as defined in PCI specifications. See [Figure 2-11 on page 2-47](#) for connectivity. This resistor is not required during normal operation.

Table 2-23 • Summary of I/O Timing Characteristics—Software Default Settings
 –1 Speed Grade, Automotive-Case Conditions: $T_J = 115^{\circ}\text{C}$, Worst Case $V_{CC} = 1.425\text{ V}$, Worst Case $V_{CCI} = 3.0\text{ V}$
 Standard Plus I/O Banks

I/O Standard	Drive Strength (mA)	Slew Rate	Capacitive Load (pF)	External Resistor	t_{DOUT} (ns)	t_{DP} (ns)	t_{DIN} (ns)	t_{PY} (ns)	t_{EOUT} (ns)	t_{ZL} (ns)	t_{ZH} (ns)	t_{LZ} (ns)	t_{HZ} (ns)	t_{ZLS} (ns)	t_{ZHS} (ns)	Units
3.3 V LVTTTL / 3.3 V LVCMOS	12 mA	High	35 pF	–	0.55	3.36	0.04	0.97	0.39	3.42	1.56	3.05	1.94	5.55	2.80	ns
2.5 V LVCMOS	12 mA	High	35 pF	–	0.55	3.05	0.04	1.23	0.39	3.11	2.99	1.56	1.69	5.23	5.11	ns
1.8 V LVCMOS	8 mA	High	35 pF	–	0.55	3.73	0.04	1.16	0.39	3.65	3.86	1.62	1.68	5.78	5.99	ns
1.5 V LVCMOS	4 mA	High	35 pF	–	0.55	4.60	0.04	1.35	0.39	4.61	5.05	2.07	1.85	6.74	7.18	ns
3.3 V PCI	Per PCI spec	High	10 pF	25^2	0.55	2.55	0.04	0.82	0.39	1.27	0.94	2.65	3.06	2.49	2.18	ns
3.3 V PCI-X	Per PCI-X spec	High	10 pF	25^2	0.55	2.55	0.04	0.79	0.39	1.27	0.94	2.65	3.06	2.49	2.18	ns

Notes:

1. For specific junction temperature and voltage supply levels, refer to [Table 2-5 on page 2-5](#) for derating values.
2. Resistance is used to measure I/O propagation delays as defined in PCI specifications. See [Figure 2-11 on page 2-47](#) for connectivity. This resistor is not required during normal operation.

Detailed I/O DC Characteristics

Table 2-24 • Input Capacitance

Symbol	Definition	Conditions	Min.	Max.	Units
C_{IN}	Input capacitance	$V_{IN} = 0$, $f = 1.0$ MHz		8	pF
C_{INCLK}	Input capacitance on the clock pin	$V_{IN} = 0$, $f = 1.0$ MHz		8	pF

Table 2-25 • I/O Output Buffer Maximum Resistances¹
Applicable to Advanced I/O Banks

Standard	Drive Strength	$R_{PULL-DOWN}$ (Ω) ²	$R_{PULL-UP}$ (Ω) ³
3.3 V LVTTTL / 3.3 V LVCMOS	2 mA	100	300
	4 mA	100	300
	6 mA	50	150
	8 mA	50	150
	12 mA	25	75
	16 mA	17	50
	24 mA	11	33
2.5 V LVCMOS	2 mA	100	200
	6 mA	50	100
	12 mA	25	50
	16 mA	20	40
	24 mA	11	22
1.8 V LVCMOS	2 mA	200	225
	4 mA	100	112
	6 mA	50	56
	8 mA	50	56
	12 mA	20	22
	16 mA	20	22
1.5 V LVCMOS	2 mA	200	224
	4 mA	100	112
	6 mA	67	75
	8 mA	33	37
	12 mA	33	37
3.3 V PCI/PCI-X	Per PCI/PCI-X specification	25	75

Notes:

1. These maximum values are provided for informational reasons only. Minimum output buffer resistance values depend on V_{CCI} , drive strength selection, temperature, and process. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the Actel website at <http://www.actel.com/download/ibis/default.aspx>.

2. $R_{(PULL-DOWN-MAX)} = (V_{OLspec}) / I_{OLspec}$

3. $R_{(PULL-UP-MAX)} = (V_{CCImax} - V_{OHspec}) / I_{OHspec}$

Table 2-26 • I/O Output Buffer Maximum Resistances¹
Applicable to Standard Plus I/O Banks

Standard	Drive Strength	R _{PULL-DOWN} (Ω) ²	R _{PULL-UP} (Ω) ³
3.3 V LVTTTL / 3.3 V LVCMOS	2 mA	100	300
	4 mA	100	300
	6 mA	50	150
	8 mA	50	150
	12 mA	25	75
	16 mA	25	75
2.5 V LVCMOS	2 mA	100	200
	6 mA	50	100
	12 mA	25	50
1.8 V LVCMOS	2 mA	200	225
	4 mA	100	112
	6 mA	50	56
	8 mA	50	56
1.5 V LVCMOS	2 mA	200	224
	4 mA	100	112
3.3 V PCI/PCI-X	Per PCI/PCI-X specification	0	0

Notes:

1. These maximum values are provided for informational reasons only. Minimum output buffer resistance values depend on V_{CC} , drive strength selection, temperature, and process. For board design considerations and detailed output buffer resistances, use the corresponding IBIS models located on the Actel website at <http://www.actel.com/download/ibis/default.aspx>.
2. $R_{(PULL-DOWN-MAX)} = (V_{OLspec}) / I_{OLspec}$
3. $R_{(PULL-UP-MAX)} = (V_{CCImax} - V_{OHspec}) / I_{OHspec}$

Table 2-27 • I/O Weak Pull-Up/Pull-Down Resistances
Minimum and Maximum Weak Pull-Up/Pull-Down Resistance Values

V _{CCI}	R _(WEAK PULL-UP) ¹ (Ω)		R _(WEAK PULL-DOWN) ² (Ω)	
	Min.	Max.	Min.	Max.
3.3 V	10 k	45 k	10 k	45 k
2.5 V	11 k	55 k	12 k	74 k
1.8 V	18 k	70 k	17 k	110 k
1.5 V	19 k	90 k	19 k	140 k

Notes:

1. $R_{(WEAK PULL-UP-MAX)} = (V_{OLspec}) / I_{(WEAK PULL-UP-MIN)}$
2. $R_{(WEAK PULL-UP-MAX)} = (V_{CCImax} - V_{OHspec}) / I_{(WEAK PULL-UP-MIN)}$

Table 2-28 • I/O Short Currents I_{OSH}/I_{OSL}
Applicable to Advanced I/O Banks

	Drive Strength	I_{OSL} (mA)*	I_{OSH} (mA)*
3.3 V LVTTTL / 3.3 V LVCMOS	2 mA	27	25
	4 mA	27	25
	6 mA	54	51
	8 mA	54	51
	12 mA	109	103
	16 mA	127	132
	24 mA	181	268
3.3 V LVCMOS	2 mA	27	25
	4 mA	27	25
	6 mA	54	51
	8 mA	54	51
	12 mA	109	103
	16 mA	127	132
	24 mA	181	268
2.5 V LVCMOS	2 mA	18	16
	6 mA	37	32
	12 mA	74	65
	16 mA	87	83
	24 mA	124	169
1.8 V LVCMOS	2 mA	11	9
	4 mA	22	17
	6 mA	44	35
	8 mA	51	45
	12 mA	74	91
	16 mA	74	91
1.5 V LVCMOS	2 mA	16	13
	4 mA	33	25
	6 mA	39	32
	8 mA	55	66
	12 mA	55	66
3.3 V PCI/PCI-X	Per PCI/PCI-X specification	109	103

* $T_J = 100^{\circ}\text{C}$

Table 2-29 • I/O Short Currents I_{OSH}/I_{OSL}
Applicable to Standard Plus I/O Banks

	Drive Strength	I_{OSL} (mA)*	I_{OSH} (mA)*
3.3 V LVTTTL / 3.3 V LVCMOS	2 mA	27	25
	4 mA	27	25
	6 mA	54	51
	8 mA	54	51
	12 mA	109	103
	16 mA	109	103
2.5 V LVCMOS	2 mA	18	16
	6 mA	37	32
	12 mA	74	65
1.8 V LVCMOS	2 mA	11	9
	4 mA	22	17
	6 mA	44	35
	8 mA	44	35
1.5 V LVCMOS	2 mA	16	13
	4 mA	33	25
3.3 V PCI/PCI-X	Per PCI/PCI-X specification	109	103

* $T_J = 100^\circ\text{C}$

The length of time an I/O can withstand I_{OSH}/I_{OSL} events depends on the junction temperature. The reliability data below is based on a 3.3 V, 12 mA I/O setting, which is the worst case for this type of analysis.

For example, at 110°C , the short current condition would have to be sustained for more than three months to cause a reliability concern. The I/O design does not contain any short circuit protection, but such protection would only be needed in extremely prolonged stress conditions.

Table 2-30 • Duration of Short Circuit Event before Failure

Temperature	Time before Failure
-40°C	> 20 years
0°C	> 20 years
25°C	> 20 years
70°C	5 years
85°C	2 years
100°C	6 months
110°C	3 months
125°C	25 days
135°	12 days

Table 2-31 • I/O Input Rise Time, Fall Time, and Related I/O Reliability

Input Buffer	Input Rise/Fall Time (min.)	Input Rise/Fall Time (max.)	Reliability
LVTTTL/LVCMOS	No requirement	10 ns *	20 years (110°C)
LVDS/B-LVDS/M-LVDS/LVPECL	No requirement	10 ns *	10 years (100°C)

* The maximum input rise/fall time is related to the noise induced into the input buffer trace. If the noise is low, the rise time and fall time of input buffers can be increased beyond the maximum value. The longer the rise/fall times, the more susceptible the input signal is to the board noise. Actel recommends signal integrity evaluation/characterization of the system to ensure there is no excessive noise coupling into input signals.

Single-Ended I/O Characteristics

3.3 V LVTTTL / 3.3 V LVCMOS

Low-Voltage Transistor–Transistor Logic (LVTTTL) is a general-purpose standard (EIA/JESD) for 3.3 V applications. It uses an LVTTTL input buffer and push-pull output buffer.

Table 2-32 • Minimum and Maximum DC Input and Output Levels
Applicable to Advanced I/O Banks

3.3 V LVTTTL / 3.3 V LVCMOS	V _{IL}		V _{IH}		V _{OL}	V _{OH}	I _{OL}	I _{OH}	I _{OSL}	I _{OSH}	I _{IL}	I _{IH}
Drive Strength	Min., V	Max., V	Min., V	Max., V	Max., V	Min., V	mA	mA	Max., mA ¹	Max., mA ¹	μA ²	μA ²
2 mA	−0.3	0.8	2	3.6	0.4	2.4	2	2	27	25	10	10
4 mA	−0.3	0.8	2	3.6	0.4	2.4	4	4	27	25	10	10
6 mA	−0.3	0.8	2	3.6	0.4	2.4	6	6	54	51	10	10
8 mA	−0.3	0.8	2	3.6	0.4	2.4	8	8	54	51	10	10
12 mA	−0.3	0.8	2	3.6	0.4	2.4	12	12	109	103	10	10
16 mA	−0.3	0.8	2	3.6	0.4	2.4	16	16	127	132	10	10
24 mA	−0.3	0.8	2	3.6	0.4	2.4	24	24	181	268	10	10

Notes:

1. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.
2. Currents are measured at 125°C junction temperature.
3. Software default selection highlighted in gray.

Table 2-33 • Minimum and Maximum DC Input and Output Levels
Applicable to Standard Plus I/O Banks

3.3 V LVTTTL / 3.3 V LVC MOS	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}	I_{OSL}	I_{OSH}	I_{IL}	I_{IH}
Drive Strength	Min., V	Max., V	Min., V	Max., V	Max., V	Min., V	mA	mA	Max., mA ¹	Max., mA ¹	μA^2	μA^2
2 mA	-0.3	0.8	2	3.6	0.4	2.4	2	2	27	25	10	10
4 mA	-0.3	0.8	2	3.6	0.4	2.4	4	4	27	25	10	10
6 mA	-0.3	0.8	2	3.6	0.4	2.4	6	6	54	51	10	10
8 mA	-0.3	0.8	2	3.6	0.4	2.4	8	8	54	51	10	10
12 mA	-0.3	0.8	2	3.6	0.4	2.4	12	12	109	103	10	10
16 mA	-0.3	0.8	2	3.6	0.4	2.4	16	16	109	103	10	10

Notes:

1. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.
2. Currents are measured at 125°C junction temperature.
3. Software default selection highlighted in gray.

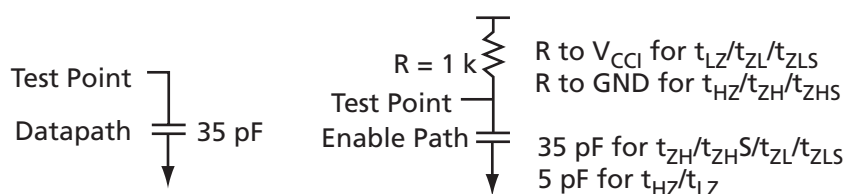


Figure 2-7 • AC Loading

Table 2-34 • AC Waveforms, Measuring Points, and Capacitive Loads

Input LOW (V)	Input HIGH (V)	Measuring Point* (V)	C_{LOAD} (pF)
0	3.3	1.4	35

* Measuring point = V_{trip} . See [Table 2-18 on page 2-17](#) for a complete table of trip points.

Timing Characteristics

Table 2-35 • 3.3 V LVTTTL / 3.3 V LVCMOS High Slew
Automotive-Case Conditions: $T_J = 135^{\circ}\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$, Worst-Case $V_{CCI} = 3.0\text{ V}$
Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	STD	0.64	8.56	0.05	1.14	0.46	8.72	7.37	1.46	1.42	11.22	9.866	ns
	-1	0.55	7.28	0.04	0.97	0.39	7.42	6.27	1.46	1.42	9.54	8.393	ns
6 mA	STD	0.64	5.49	0.05	1.14	0.46	5.59	4.55	1.65	1.74	8.09	7.05	ns
	-1	0.55	4.67	0.04	0.97	0.39	4.75	3.87	1.65	1.74	6.88	5.997	ns
8 mA	STD	0.64	5.49	0.05	1.14	0.46	5.59	4.55	1.65	1.74	8.09	7.05	ns
	-1	0.55	4.67	0.04	0.97	0.39	4.75	3.87	1.65	1.74	6.88	5.997	ns
12 mA	STD	0.64	3.95	0.05	1.14	0.46	4.02	1.56	3.59	1.94	6.52	2.795	ns
	-1	0.55	3.36	0.04	0.97	0.39	3.42	1.56	3.05	1.94	5.55	2.797	ns
16 mA	STD	0.64	3.73	0.05	1.14	0.46	1.84	1.42	3.65	4.11	3.05	2.651	ns
	-1	0.55	3.17	0.04	0.97	0.39	1.84	1.42	3.10	3.50	3.05	2.653	ns
24 mA	STD	0.64	3.44	0.05	1.14	0.46	1.70	1.17	3.72	4.54	2.91	2.405	ns
	-1	0.55	2.92	0.04	0.97	0.39	1.70	1.17	3.16	3.86	2.91	2.407	ns

Notes:

1. Software default selection highlighted in gray.
2. For specific junction temperature and voltage supply levels, refer to [Table 2-5 on page 2-5](#) for derating values.

Table 2-36 • 3.3 V LVTTTL / 3.3 V LVCMOS Low Slew
Automotive-Case Conditions: $T_J = 135^{\circ}\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$, Worst-Case $V_{CCI} = 3.0\text{ V}$
Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	STD	0.64	11.47	0.05	1.14	0.46	11.68	9.95	1.46	1.33	14.18	12.449	ns
	-1	0.55	9.75	0.04	0.97	0.39	9.94	8.46	1.46	1.33	12.06	10.59	ns
6 mA	STD	0.64	8.13	0.05	1.14	0.46	8.28	7.03	1.65	1.65	10.79	9.526	ns
	-1	0.55	6.92	0.04	0.97	0.39	7.05	5.98	1.65	1.65	9.17	8.103	ns
8 mA	STD	0.64	8.13	0.05	1.14	0.46	8.28	7.03	1.65	1.65	10.79	9.526	ns
	-1	0.55	6.92	0.04	0.97	0.39	7.05	5.98	1.65	1.65	9.17	8.103	ns
12 mA	STD	0.64	6.24	0.05	1.14	0.46	6.36	5.45	1.77	1.85	8.86	7.946	ns
	-1	0.55	5.31	0.04	0.97	0.39	5.41	4.63	1.77	1.85	7.53	6.76	ns
16 mA	STD	0.64	5.82	0.05	1.14	0.46	5.93	5.10	1.80	1.90	8.43	7.604	ns
	-1	0.55	4.95	0.04	0.97	0.39	5.04	4.34	1.80	1.90	7.17	6.468	ns
24 mA	STD	0.64	5.42	0.05	1.14	0.46	5.52	5.08	1.83	2.10	8.02	7.581	ns
	-1	0.55	4.61	0.04	0.97	0.39	4.70	4.32	1.83	2.11	6.82	6.449	ns

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-5 on page 2-5](#) for derating values.

Table 2-37 • 3.3 V LVTTTL / 3.3 V LVCMOS High Slew

Automotive-Case Conditions: $T_J = 135^{\circ}\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$, Worst-Case $V_{CCI} = 3.0\text{ V}$
Applicable to Standard Plus I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	STD	0.64	8.06	0.05	1.12	0.46	8.20	7.03	1.26	1.27	8.20	7.027	ns
	-1	0.55	6.85	0.04	.095	0.39	6.98	5.98	1.26	1.27	6.98	5.978	ns
6 mA	STD	0.64	5.03	0.05	1.12	0.46	5.13	4.27	1.42	1.56	5.13	4.267	ns
	-1	0.55	4.28	0.04	0.95	0.39	4.36	3.63	1.42	1.56	4.36	3.63	ns
8 mA	STD	0.64	5.03	0.05	1.12	0.46	5.13	4.27	1.42	1.56	5.13	4.267	ns
	-1	0.55	4.28	0.04	0.95	0.39	4.36	3.63	1.42	1.56	4.36	3.63	ns
12 mA	STD	0.64	3.53	0.05	1.12	0.46	1.74	1.43	3.12	3.60	1.74	1.427	ns
	-1	0.55	3.01	0.04	0.95	0.39	1.74	1.43	2.65	3.06	1.74	1.428	ns
16 mA	STD	0.64	3.53	0.05	1.12	0.46	1.74	1.43	3.12	3.60	1.74	1.427	ns
	-1	0.55	3.01	0.04	0.95	0.39	1.74	1.43	2.65	3.06	1.74	1.428	ns

Notes:

1. Software default selection highlighted in gray.
2. For specific junction temperature and voltage supply levels, refer to [Table 2-5 on page 2-5](#) for derating values.

Table 2-38 • 3.3 V LVTTTL / 3.3 V LVCMOS Low Slew

Automotive-Case Conditions: $T_J = 135^{\circ}\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$, Worst-Case $V_{CCI} = 3.0\text{ V}$
Applicable to Standard Plus I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	STD	0.64	10.82	0.05	1.12	0.46	11.02	9.42	1.26	1.20	11.02	9.419	ns
	-1	0.55	9.21	0.04	0.95	0.39	9.38	8.01	1.26	1.20	9.38	8.012	ns
6 mA	STD	0.64	7.49	0.05	1.12	0.46	7.63	6.58	1.43	1.48	7.63	6.58	ns
	-1	0.55	6.37	0.04	0.95	0.39	6.49	5.60	1.43	1.49	6.49	5.598	ns
8 mA	STD	0.64	7.49	0.05	1.12	0.46	7.63	6.58	1.43	1.48	7.63	6.58	ns
	-1	0.55	6.37	0.04	0.95	0.39	6.49	5.60	1.43	1.49	6.49	5.598	ns
12 mA	STD	0.64	5.64	0.05	1.12	0.46	5.75	5.04	1.54	1.67	5.75	5.042	ns
	-1	0.55	4.80	0.04	0.95	0.39	4.89	4.29	1.54	1.67	4.89	4.289	ns
16 mA	STD	0.64	5.64	0.05	1.12	0.46	5.75	5.04	1.54	1.67	5.75	5.042	ns
	-1	0.55	4.80	0.04	0.95	0.39	4.89	4.29	1.54	1.67	4.89	4.289	ns

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-5 on page 2-5](#) for derating values.

Table 2-39 • 3.3 V LVTTL / 3.3 V LVCMOS High Slew

Automotive-Case Conditions: $T_J = 115^{\circ}\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$, Worst-Case $V_{CCI} = 3.0\text{ V}$
Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	STD	0.63	8.28	0.05	1.10	0.45	8.44	7.13	1.42	1.37	10.85	9.55	ns
	-1	0.53	7.05	0.04	0.94	0.38	7.18	6.06	1.42	1.37	9.23	8.12	ns
6 mA	STD	0.63	5.31	0.05	1.10	0.45	5.41	4.40	1.60	1.68	7.83	6.82	ns
	-1	0.53	4.52	0.04	0.94	0.38	4.60	3.74	1.60	1.68	6.66	5.80	ns
8 mA	STD	0.63	5.31	0.05	1.10	0.45	5.41	4.40	1.60	1.68	7.83	6.82	ns
	-1	0.53	4.52	0.04	0.94	0.38	4.60	3.74	1.60	1.68	6.66	5.80	ns
12 mA	STD	0.63	3.82	0.05	1.10	0.45	3.89	1.51	3.47	1.88	6.31	2.70	ns
	-1	0.53	3.25	0.04	0.94	0.38	3.31	1.51	2.96	1.88	5.37	2.71	ns
16 mA	STD	0.63	3.60	0.05	1.10	0.45	1.78	1.37	3.53	3.98	2.95	2.57	ns
	-1	0.53	3.07	0.04	0.94	0.38	1.78	1.37	3.00	3.38	2.95	2.57	ns
24 mA	STD	0.63	3.33	0.05	1.10	0.45	1.64	1.13	3.60	4.39	2.81	2.33	ns
	-1	0.53	2.83	0.04	0.94	0.38	1.64	1.13	3.06	3.74	2.82	2.33	ns

Notes:

1. Software default selection highlighted in gray.
2. For specific junction temperature and voltage supply levels, refer to [Table 2-5 on page 2-5](#) for derating values.

Table 2-40 • 3.3 V LVTTL / 3.3 V LVCMOS Low Slew

Automotive-Case Conditions: $T_J = 115^{\circ}\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$, Worst-Case $V_{CCI} = 3.0\text{ V}$
Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	STD	0.63	11.09	0.05	1.10	0.45	11.30	9.63	1.41	1.29	13.72	12.04	ns
	-1	0.53	9.44	0.04	0.94	0.38	9.61	8.19	1.41	1.29	11.67	10.25	ns
6 mA	STD	0.63	7.87	0.05	1.10	0.45	8.02	6.80	1.59	1.59	10.43	9.22	ns
	-1	0.53	6.69	0.04	0.94	0.38	6.82	5.78	1.59	1.60	8.88	7.84	ns
8 mA	STD	0.63	7.87	0.05	1.10	0.45	8.02	6.80	1.59	1.59	10.43	9.22	ns
	-1	0.53	6.69	0.04	0.94	0.38	6.82	5.78	1.59	1.60	8.88	7.84	ns
12 mA	STD	0.63	6.04	0.05	1.10	0.45	6.15	5.27	1.71	1.79	8.57	7.69	ns
	-1	0.53	5.14	0.04	0.94	0.38	5.23	4.48	1.71	1.79	7.29	6.54	ns
16 mA	STD	0.63	5.63	0.05	1.10	0.45	5.74	4.94	1.74	1.84	8.16	7.36	ns
	-1	0.53	4.79	0.04	0.94	0.38	4.88	4.20	1.74	1.84	6.94	6.26	ns
24 mA	STD	0.63	5.25	0.05	1.10	0.45	5.34	4.92	1.77	2.04	7.76	7.34	ns
	-1	0.53	4.46	0.04	0.94	0.38	4.55	4.18	1.77	2.04	6.60	6.24	ns

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-5 on page 2-5](#) for derating values.

Table 2-41 • 3.3 V LVTTTL / 3.3 V LVCMOS High Slew

Automotive-Case Conditions: $T_J = 115^{\circ}\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$, Worst-Case $V_{CCI} = 3.0\text{ V}$
Applicable to Standard Plus I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	STD	0.63	7.79	0.05	1.08	0.45	7.94	6.80	1.22	1.23	7.94	6.80	ns
	-1	0.55	6.85	0.04	0.95	0.39	6.98	5.98	1.26	1.27	6.98	5.98	ns
6 mA	STD	0.63	4.87	0.05	1.08	0.45	4.96	4.13	1.38	1.51	4.96	4.13	ns
	-1	0.55	4.28	0.04	0.95	0.39	4.36	3.63	1.42	1.56	4.36	3.63	ns
8 mA	STD	0.63	4.87	0.05	1.08	0.45	4.96	4.13	1.38	1.51	4.96	4.13	ns
	-1	0.55	4.28	0.04	0.95	0.39	4.36	3.63	1.42	1.56	4.36	3.63	ns
12 mA	STD	0.63	3.42	0.05	1.08	0.45	1.69	1.38	3.02	3.48	1.69	1.38	ns
	-1	0.55	3.01	0.04	0.95	0.39	1.74	1.43	2.65	3.06	1.74	1.43	ns
16 mA	STD	0.63	3.42	0.05	1.08	0.45	1.69	1.38	3.02	3.48	1.69	1.38	ns
	-1	0.55	3.01	0.04	0.95	0.39	1.74	1.43	2.65	3.06	1.74	1.43	ns

Notes:

1. Software default selection highlighted in gray.
2. For specific junction temperature and voltage supply levels, refer to [Table 2-5 on page 2-5](#) for derating values.

Table 2-42 • 3.3 V LVTTTL / 3.3 V LVCMOS Low Slew

Automotive-Case Conditions: $T_J = 115^{\circ}\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$, Worst-Case $V_{CCI} = 3.0\text{ V}$
Applicable to Standard Plus I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
4 mA	STD	0.63	10.47	0.05	1.08	0.45	10.66	9.11	1.22	1.16	10.66	9.11	ns
	-1	0.55	9.21	0.04	0.95	0.39	9.38	8.01	1.26	1.20	9.38	8.01	ns
6 mA	STD	0.63	7.25	0.05	1.08	0.45	7.38	6.37	1.38	1.44	7.38	6.37	ns
	-1	0.55	6.37	0.04	0.95	0.39	6.49	5.60	1.43	1.49	6.49	5.60	ns
8 mA	STD	0.63	7.25	0.05	1.08	0.45	7.38	6.37	1.38	1.44	7.38	6.37	ns
	-1	0.55	6.37	0.04	0.95	0.39	6.49	5.60	1.43	1.49	6.49	5.60	ns
12 mA	STD	0.63	5.46	0.05	1.08	0.45	5.56	4.88	1.49	1.61	5.56	4.88	ns
	-1	0.55	4.80	0.04	0.95	0.39	4.89	4.29	1.54	1.67	4.89	4.29	ns
16 mA	STD	0.63	5.46	0.05	1.08	0.45	5.56	4.88	1.49	1.61	5.56	4.88	ns
	-1	0.55	4.80	0.04	0.95	0.39	4.89	4.29	1.54	1.67	4.89	4.29	ns

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-5 on page 2-5](#) for derating values.

2.5 V LVCMOS

Low-Voltage CMOS for 2.5 V is an extension of the LVCMOS standard (JESD8-5) used for general-purpose 2.5 V applications. It uses a 5 V-tolerant input buffer and push-pull output buffer.

Table 2-43 • Minimum and Maximum DC Input and Output Levels
Applicable to Advanced I/O Banks

2.5 V LVCMOS	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}	I_{OSL}	I_{OSH}	I_{IL}	I_{IH}
Drive Strength	Min., V	Max., V	Min., V	Max., V	Max., V	Min., V	mA	mA	Max., mA ¹	Max., mA ¹	μA^2	μA^2
2 mA	-0.3	0.7	1.7	3.6	0.7	1.7	2	2	18	16	10	10
6 mA	-0.3	0.7	1.7	3.6	0.7	1.7	6	6	37	32	10	10
12 mA	-0.3	0.7	1.7	3.6	0.7	1.7	12	12	74	65	10	10
16 mA	-0.3	0.7	1.7	3.6	0.7	1.7	16	16	87	83	10	10
24 mA	-0.3	0.7	1.7	3.6	0.7	1.7	24	24	124	169	10	10

Notes:

1. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.
2. Currents are measured at 125°C junction temperature.
3. Software default selection highlighted in gray.

Table 2-44 • Minimum and Maximum DC Input and Output Levels
Applicable to Standard Plus I/O Banks

2.5 V LVCMOS	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}	I_{OSL}	I_{OSH}	I_{IL}	I_{IH}
Drive Strength	Min., V	Max., V	Min., V	Max., V	Max., V	Min., V	mA	mA	Max., mA ¹	Max., mA ¹	μA^2	μA^2
2 mA	-0.3	0.7	1.7	3.6	0.7	1.7	2	2	18	16	10	10
6 mA	-0.3	0.7	1.7	3.6	0.7	1.7	6	6	37	32	10	10
12 mA	-0.3	0.7	1.7	3.6	0.7	1.7	12	12	74	65	10	10

Notes:

1. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.
2. Currents are measured at 125°C junction temperature.
3. Software default selection highlighted in gray.

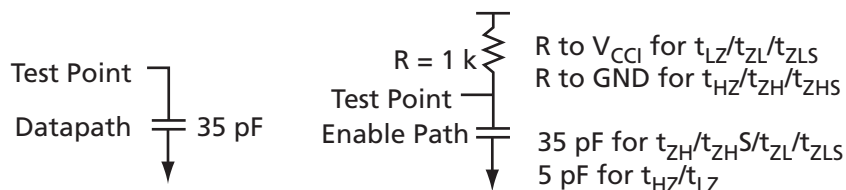


Figure 2-8 • AC Loading

Table 2-45 • AC Waveforms, Measuring Points, and Capacitive Loads

Input LOW (V)	Input HIGH (V)	Measuring Point* (V)	C_{LOAD} (pF)
0	2.5	1.2	35

* Measuring point = V_{trip} . See Table 2-18 on page 2-17 for a complete table of trip points.

Timing Characteristics

Table 2-46 • 2.5 V LVC MOS High Slew

Automotive-Case Conditions: $T_J = 135^{\circ}\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$, Worst-Case $V_{CCI} = 2.3\text{ V}$
Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	STD	0.64	9.69	0.05	1.45	0.46	8.76	9.69	1.48	1.25	11.26	12.187	ns
	-1	0.55	8.24	0.04	1.23	0.39	7.45	8.24	1.48	1.25	9.58	10.367	ns
6 mA	STD	0.64	5.78	0.05	1.45	0.46	5.63	5.78	1.68	1.62	8.13	8.277	ns
	-1	0.55	4.91	0.04	1.23	0.39	4.79	4.91	1.69	1.63	6.92	7.04	ns
12 mA	STD	0.64	3.98	0.05	1.45	0.46	4.05	3.84	1.82	1.86	6.55	6.338	ns
	-1	0.55	3.39	0.04	1.23	0.39	3.45	3.27	1.83	1.86	5.58	5.392	ns
16 mA	STD	0.64	3.75	0.05	1.45	0.46	1.85	1.69	3.76	3.97	3.06	2.926	ns
	-1	0.55	3.19	0.04	1.23	0.39	1.85	1.69	3.20	3.38	3.06	2.929	ns
24 mA	STD	0.64	3.45	0.05	1.45	0.46	1.70	1.35	3.84	4.47	2.92	2.585	ns
	-1	0.55	2.94	0.04	1.23	0.39	1.71	1.35	3.27	3.80	2.92	2.586	ns

Notes:

1. Software default selection highlighted in gray.
2. For specific junction temperature and voltage supply levels, refer to [Table 2-5 on page 2-5](#) for derating values.

Table 2-47 • 2.5 V LVC MOS Low Slew

Automotive-Case Conditions: $T_J = 135^{\circ}\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$, Worst-Case $V_{CCI} = 2.3\text{ V}$
Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	STD	0.64	12.12	0.05	1.45	0.46	12.54	12.74	1.48	1.19	15.04	15.243	ns
	-1	0.55	10.31	0.04	1.23	0.39	10.67	10.84	1.48	1.20	12.80	12.966	ns
6 mA	STD	0.64	8.24	0.05	1.45	0.46	9.07	8.74	1.68	1.57	11.57	11.237	ns
	-1	0.55	7.01	0.04	1.23	0.39	7.71	7.43	1.69	1.57	9.84	9.559	ns
12 mA	STD	0.64	6.91	0.05	1.45	0.46	7.04	6.62	1.82	1.80	9.54	9.117	ns
	-1	0.55	5.88	0.04	1.23	0.39	5.99	5.63	1.83	1.80	8.11	7.756	ns
16 mA	STD	0.64	6.44	0.05	1.45	0.46	6.56	6.18	1.86	1.86	9.06	8.678	ns
	-1	0.55	5.48	0.04	1.23	0.39	5.58	5.26	1.86	1.86	7.71	7.382	ns
24 mA	STD	0.64	6.16	0.05	1.45	0.46	6.15	6.16	1.90	2.10	8.65	8.657	ns
	-1	0.55	5.24	0.04	1.23	0.39	5.23	5.24	1.90	2.10	7.36	7.364	ns

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-5 on page 2-5](#) for derating values.

Table 2-48 • 2.5 V LVC MOS High Slew

Automotive-Case Conditions: $T_J = 135^{\circ}\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$, Worst-Case $V_{CCI} = 2.3\text{ V}$
Applicable to Standard Plus I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	STD	0.64	9.26	0.05	1.45	0.46	8.28	9.26	1.24	1.12	10.78	11.756	ns
	-1	0.55	7.87	0.04	1.23	0.39	7.05	7.87	1.24	1.13	9.17	10	ns
6 mA	STD	0.64	5.43	0.05	1.45	0.46	5.19	5.43	1.43	1.47	7.69	7.926	ns
	-1	0.55	4.62	0.04	1.23	0.39	4.42	4.62	1.43	1.47	6.55	6.743	ns
12 mA	STD	0.64	3.59	0.05	1.45	0.46	3.65	3.51	1.56	1.69	6.15	6.012	ns
	-1	0.55	3.05	0.04	1.23	0.39	3.11	2.99	1.56	1.69	5.23	5.114	ns

Notes:

1. Software default selection highlighted in gray.
2. For specific junction temperature and voltage supply levels, refer to [Table 2-5 on page 2-5](#) for derating values.

Table 2-49 • 2.5 V LVC MOS Low Slew

Automotive-Case Conditions: $T_J = 135^{\circ}\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$, Worst-Case $V_{CCI} = 2.3\text{ V}$
Applicable to Standard Plus I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	STD	0.64	12.12	0.05	1.45	0.46	11.89	12.12	1.25	1.08	14.39	14.622	ns
	-1	0.55	10.31	0.04	1.23	0.39	10.12	10.31	1.25	1.08	12.24	12.438	ns
6 mA	STD	0.64	8.24	0.05	1.45	0.46	8.39	8.23	1.43	1.42	10.89	10.73	ns
	-1	0.55	7.01	0.04	1.23	0.39	7.14	7.00	1.43	1.42	9.26	9.128	ns
12 mA	STD	0.64	6.30	0.05	1.45	0.46	6.41	6.16	1.56	1.63	8.91	8.656	ns
	-1	0.55	5.35	0.04	1.23	0.39	5.45	5.24	1.56	1.63	7.58	7.364	ns

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-5 on page 2-5](#) for derating values.

Table 2-50 • 2.5 V LVCMOS High Slew

Automotive-Case Conditions: $T_J = 115^{\circ}\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$, Worst-Case $V_{CCI} = 2.3\text{ V}$
Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	STD	0.63	9.37	0.05	1.40	0.45	8.47	9.37	1.43	1.21	10.89	11.79	ns
	-1	0.53	7.97	0.04	1.19	0.38	7.21	7.97	1.43	1.21	9.27	10.03	ns
6 mA	STD	0.63	5.59	0.05	1.40	0.45	5.45	5.59	1.63	1.57	7.87	8.01	ns
	-1	0.53	4.75	0.04	1.19	0.38	4.63	4.75	1.63	1.57	6.69	6.81	ns
12 mA	STD	0.63	3.85	0.05	1.40	0.45	3.92	3.71	1.77	1.80	6.34	6.13	ns
	-1	0.53	3.28	0.04	1.19	0.38	3.34	3.16	1.77	1.80	5.39	5.22	ns
16 mA	STD	0.63	3.63	0.05	1.40	0.45	1.79	1.64	3.64	3.84	2.96	2.83	ns
	-1	0.53	3.08	0.04	1.19	0.38	1.79	1.64	3.09	3.27	2.96	2.83	ns
24 mA	STD	0.63	3.34	0.05	1.40	0.45	1.65	1.31	3.72	4.32	2.82	2.50	ns
	-1	0.53	2.84	0.04	1.19	0.38	1.65	1.31	3.16	3.68	2.82	2.50	ns

Notes:

1. Software default selection highlighted in gray.
2. For specific junction temperature and voltage supply levels, refer to [Table 2-5 on page 2-5](#) for derating values.

Table 2-51 • 2.5 V LVCMOS Low Slew

Automotive-Case Conditions: $T_J = 115^{\circ}\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$, Worst-Case $V_{CCI} = 2.3\text{ V}$
Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	STD	0.63	11.73	0.05	1.40	0.45	12.14	12.33	1.43	1.16	14.55	14.75	ns
	-1	0.53	9.98	0.04	1.19	0.38	10.32	10.49	1.43	1.16	12.38	12.55	ns
6 mA	STD	0.63	7.97	0.05	1.40	0.45	8.77	8.45	1.63	1.51	11.19	10.87	ns
	-1	0.53	6.78	0.04	1.19	0.38	7.46	7.19	1.63	1.52	9.52	9.25	ns
12 mA	STD	0.63	6.68	0.05	1.40	0.45	6.81	6.40	1.77	1.74	9.23	8.82	ns
	-1	0.53	5.69	0.04	1.19	0.38	5.79	5.45	1.77	1.74	7.85	7.50	ns
16 mA	STD	0.63	6.24	0.05	1.40	0.45	6.35	5.98	1.80	1.80	8.77	8.40	ns
	-1	0.53	5.30	0.04	1.19	0.38	5.40	5.08	1.80	1.80	7.46	7.14	ns
24 mA	STD	0.63	5.96	0.05	1.40	0.45	5.95	5.96	1.84	2.03	8.37	8.38	ns
	-1	0.53	5.07	0.04	1.19	0.38	5.06	5.07	1.84	2.03	7.12	7.12	ns

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-5 on page 2-5](#) for derating values.

Table 2-52 • 2.5 V LVC MOS High Slew

Automotive-Case Conditions: $T_J = 115^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$, Worst-Case $V_{CCI} = 2.3\text{ V}$
Applicable to Standard Plus I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	STD	0.63	8.95	0.05	1.40	0.45	8.01	8.95	1.20	1.09	10.43	11.37	ns
	-1	0.53	7.62	0.04	1.19	0.38	6.82	7.62	1.20	1.09	8.87	9.68	ns
6 mA	STD	0.63	5.25	0.05	1.40	0.45	5.03	5.25	1.38	1.42	7.44	7.67	ns
	-1	0.53	4.47	0.04	1.19	0.38	4.27	4.47	1.38	1.42	6.33	6.52	ns
12 mA	STD	0.63	3.47	0.05	1.40	0.45	3.53	3.40	1.51	1.63	5.95	5.82	ns
	-1	0.53	2.95	0.04	1.19	0.38	3.01	2.89	1.51	1.63	5.06	4.95	ns

Notes:

1. Software default selection highlighted in gray.
2. For specific junction temperature and voltage supply levels, refer to [Table 2-5 on page 2-5](#) for derating values.

Table 2-53 • 2.5 V LVC MOS Low Slew

Automotive-Case Conditions: $T_J = 115^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$, Worst-Case $V_{CCI} = 2.3\text{ V}$
Applicable to Standard Plus I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	STD	0.63	11.73	0.05	1.40	0.45	11.51	11.73	1.21	1.04	13.93	14.15	ns
	-1	0.53	9.98	0.04	1.19	0.38	9.79	9.98	1.21	1.04	11.85	12.03	ns
6 mA	STD	0.63	7.97	0.05	1.40	0.45	8.12	7.96	1.38	1.37	10.54	10.38	ns
	-1	0.53	6.78	0.04	1.19	0.38	6.91	6.77	1.39	1.37	8.96	8.83	ns
12 mA	STD	0.63	6.09	0.05	1.40	0.45	6.20	5.96	1.51	1.58	8.62	8.38	ns
	-1	0.53	5.18	0.04	1.19	0.38	5.28	5.07	1.51	1.58	7.33	7.12	ns

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-5 on page 2-5](#) for derating values.

1.8 V LVCMOS

Low-voltage CMOS for 1.8 V is an extension of the LVCMOS standard (JESD8-5) used for general-purpose 1.8 V applications. It uses a 1.8 V input buffer and a push-pull output buffer.

Table 2-54 • Minimum and Maximum DC Input and Output Levels
Applicable to Advanced I/O Banks

1.8 V LVCMOS	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}	I_{OSL}	I_{OSH}	I_{IL}	I_{IH}
Drive Strength	Min., V	Max., V	Min., V	Max., V	Max., V	Min., V	mA	mA	Max., mA ¹	Max., mA ¹	μA^2	μA^2
2 mA	-0.3	$0.35 * V_{CCI}$	$0.65 * V_{CCI}$	3.6	0.45	$V_{CCI} - 0.45$	2	2	11	9	10	10
4 mA	-0.3	$0.35 * V_{CCI}$	$0.65 * V_{CCI}$	3.6	0.45	$V_{CCI} - 0.45$	4	4	22	17	10	10
6 mA	-0.3	$0.35 * V_{CCI}$	$0.65 * V_{CCI}$	3.6	0.45	$V_{CCI} - 0.45$	6	6	44	35	10	10
8 mA	-0.3	$0.35 * V_{CCI}$	$0.65 * V_{CCI}$	3.6	0.45	$V_{CCI} - 0.45$	8	8	51	45	10	10
12 mA	-0.3	$0.35 * V_{CCI}$	$0.65 * V_{CCI}$	3.6	0.45	$V_{CCI} - 0.45$	12	12	74	91	10	10
16 mA	-0.3	$0.35 * V_{CCI}$	$0.65 * V_{CCI}$	3.6	0.45	$V_{CCI} - 0.45$	16	16	74	91	10	10

Notes:

1. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.
2. Currents are measured at 125°C junction temperature.
3. Software default selection highlighted in gray.

Table 2-55 • Minimum and Maximum DC Input and Output Levels
Applicable to Standard Plus I/O I/O Banks

1.8 V LVCMOS	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}	I_{OSL}	I_{OSH}	I_{IL}	I_{IH}
Drive Strength	Min., V	Max., V	Min., V	Max., V	Max., V	Min., V	mA	mA	Max., mA ¹	Max., mA ¹	μA^2	μA^2
2 mA	-0.3	$0.35 * V_{CCI}$	$0.65 * V_{CCI}$	3.6	0.45	$V_{CCI} - 0.45$	2	2	11	9	10	10
4 mA	-0.3	$0.35 * V_{CCI}$	$0.65 * V_{CCI}$	3.6	0.45	$V_{CCI} - 0.45$	4	4	22	17	10	10
6 mA	-0.3	$0.35 * V_{CCI}$	$0.65 * V_{CCI}$	3.6	0.45	$V_{CCI} - 0.45$	6	6	44	35	10	10
8 mA	-0.3	$0.35 * V_{CCI}$	$0.65 * V_{CCI}$	3.6	0.45	$V_{CCI} - 0.45$	8	8	44	35	10	10

Notes:

1. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.
2. Currents are measured at 125°C junction temperature.
3. Software default selection highlighted in gray.

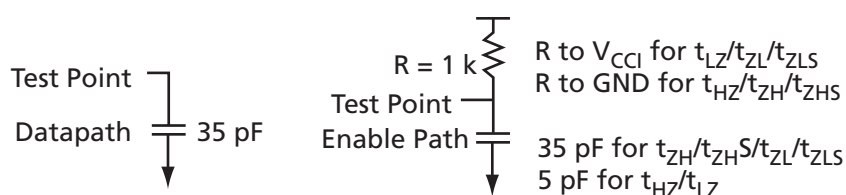


Figure 2-9 • AC Loading

Table 2-56 • AC Waveforms, Measuring Points, and Capacitive Loads

Input LOW (V)	Input HIGH (V)	Measuring Point* (V)	C _{LOAD} (pF)
0	1.8	0.9	35

* Measuring point = V_{trip} . See [Table 2-18 on page 2-17](#) for a complete table of trip points.

Timing Characteristics

Table 2-57 • 1.8 V LVC MOS High Slew

Automotive-Case Conditions: $T_J = 135^{\circ}\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$, Worst-Case $V_{CCI} = 2.3\text{ V}$
Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	STD	0.64	13.26	0.05	1.36	0.46	10.22	13.26	1.53	0.90	12.72	15.764	ns
	-1	0.55	11.28	0.04	1.16	0.39	8.69	11.28	1.53	0.90	10.82	13.41	ns
4 mA	STD	0.64	7.73	0.05	1.36	0.46	6.55	7.73	1.78	1.54	9.05	10.232	ns
	-1	0.55	6.58	0.04	1.16	0.39	5.58	6.58	1.78	1.54	7.70	8.704	ns
6 mA	STD	0.64	4.97	0.05	1.36	0.46	4.67	4.97	1.95	1.83	7.17	7.472	ns
	-1	0.55	4.23	0.04	1.16	0.39	3.98	4.23	1.95	1.83	6.10	6.356	ns
8 mA	STD	0.64	4.39	0.05	1.36	0.46	4.39	4.39	1.99	1.91	6.89	6.888	ns
	-1	0.55	3.73	0.04	1.16	0.39	3.74	3.73	1.99	1.91	5.86	5.859	ns
12 mA	STD	0.64	3.95	0.05	1.36	0.46	1.95	1.68	4.14	4.56	3.16	2.915	ns
	-1	0.55	3.36	0.04	1.16	0.39	1.95	1.68	3.52	3.88	3.16	2.918	ns
16 mA	STD	0.64	3.95	0.05	1.36	0.46	1.95	1.68	4.14	4.56	3.16	2.915	ns
	-1	0.55	3.36	0.04	1.16	0.39	1.95	1.68	3.52	3.88	3.16	2.918	ns

Notes:

1. Software default selection highlighted in gray.
2. For specific junction temperature and voltage supply levels, refer to [Table 2-5 on page 2-5](#) for derating values.

Table 2-58 • 1.8 V LVC MOS Low Slew

Automotive-Case Conditions: $T_J = 135^{\circ}\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$, Worst-Case $V_{CCI} = 2.3\text{ V}$
Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	STD	0.64	17.36	0.05	1.45	0.46	15.78	17.36	1.53	0.87	18.28	19.864	ns
	-1	0.55	14.77	0.04	1.23	0.39	13.42	14.77	1.54	0.87	15.55	16.897	ns
4 mA	STD	0.64	11.71	0.05	1.45	0.46	11.64	11.71	1.78	1.48	14.14	14.214	ns
	-1	0.55	9.96	0.04	1.23	0.39	9.90	9.96	1.78	1.48	12.03	12.091	ns
6 mA	STD	0.64	9.00	0.05	1.45	0.46	9.17	8.77	1.95	1.77	11.67	11.267	ns
	-1	0.55	7.66	0.04	1.23	0.39	7.80	7.46	1.95	1.77	9.92	9.585	ns
8 mA	STD	0.64	8.39	0.05	1.45	0.46	8.54	8.16	1.99	1.85	11.04	10.66	ns
	-1	0.55	7.14	0.04	1.23	0.39	7.27	6.94	1.99	1.85	9.40	9.068	ns
12 mA	STD	0.64	8.15	0.05	1.45	0.46	8.09	8.15	2.05	2.14	10.59	10.654	ns
	-1	0.55	6.94	0.04	1.23	0.39	6.88	6.94	2.05	2.14	9.01	9.063	ns
16 mA	STD	0.64	8.15	0.05	1.45	0.46	8.09	8.15	2.05	2.14	10.59	10.654	ns
	-1	0.55	6.94	0.04	1.23	0.39	6.88	6.94	2.05	2.14	9.01	9.063	ns

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-5 on page 2-5](#) for derating values.

Table 2-59 • 1.8 V LVC MOS High Slew

Automotive-Case Conditions: $T_J = 135^{\circ}\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$, Worst-Case $V_{CCI} = 2.3\text{ V}$
Applicable to Standard Plus I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	STD	0.64	13.26	0.05	1.36	0.46	9.75	12.67	1.24	0.82	12.26	15.17	ns
	-1	0.55	11.28	0.04	1.16	0.39	8.30	10.78	1.24	0.83	10.43	12.905	ns
4 mA	STD	0.64	7.73	0.05	1.36	0.46	6.13	7.25	1.46	1.41	8.63	9.749	ns
	-1	0.55	6.58	0.04	1.16	0.39	5.21	6.17	1.46	1.41	7.34	8.293	ns
6 mA	STD	0.64	4.97	0.05	1.36	0.46	4.29	4.54	1.62	1.68	6.79	7.039	ns
	-1	0.55	4.23	0.04	1.16	0.39	3.65	3.86	1.62	1.68	5.78	5.987	ns
8 mA	STD	0.64	4.39	0.05	1.36	0.46	4.29	4.54	1.62	1.68	6.79	7.039	ns
	-1	0.55	3.73	0.04	1.16	0.39	3.65	3.86	1.62	1.68	5.78	5.987	ns

Notes:

1. Software default selection highlighted in gray.
2. For specific junction temperature and voltage supply levels, refer to [Table 2-5 on page 2-5](#) for derating values.

Table 2-60 • 1.8 V LVC MOS Low Slew

Automotive-Case Conditions: $T_J = 135^{\circ}\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$, Worst-Case $V_{CCI} = 2.3\text{ V}$
Applicable to Standard Plus I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	STD	0.64	17.36	0.05	1.45	0.46	15.09	16.55	1.24	0.79	17.59	19.052	ns
	-1	0.55	14.77	0.04	1.23	0.39	12.84	14.08	1.24	0.79	14.96	16.207	ns
4 mA	STD	0.64	11.71	0.05	1.45	0.46	10.88	11.07	1.47	1.35	13.38	13.567	ns
	-1	0.55	9.96	0.04	1.23	0.39	9.26	9.41	1.47	1.35	11.38	11.541	ns
6 mA	STD	0.64	9.00	0.05	1.45	0.46	8.47	8.18	1.62	1.62	10.97	10.685	ns
	-1	0.55	7.66	0.04	1.23	0.39	7.21	6.96	1.62	1.62	9.33	9.089	ns
8 mA	STD	0.64	8.39	0.05	1.45	0.46	8.47	8.18	1.62	1.62	10.97	10.685	ns
	-1	0.55	7.14	0.04	1.23	0.39	7.21	6.96	1.62	1.62	9.33	9.089	ns

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-5 on page 2-5](#) for derating values.

Table 2-61 • 1.8 V LVC MOS High Slew

Automotive-Case Conditions: $T_J = 115^{\circ}\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$, Worst-Case $V_{CCI} = 2.3\text{ V}$
Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	STD	0.63	12.83	0.05	1.32	0.45	9.88	12.83	1.48	0.87	12.30	15.25	ns
	-1	0.53	10.92	0.04	1.12	0.38	8.41	10.92	1.48	0.87	10.46	12.97	ns
4 mA	STD	0.63	7.48	0.05	1.32	0.45	6.34	7.48	1.72	1.49	8.76	9.90	ns
	-1	0.53	6.36	0.04	1.12	0.38	5.39	6.36	1.72	1.49	7.45	8.42	ns
6 mA	STD	0.63	4.81	0.05	1.32	0.45	4.52	4.81	1.89	1.77	6.94	7.23	ns
	-1	0.53	4.09	0.04	1.12	0.38	3.85	4.09	1.89	1.77	5.90	6.15	ns
8 mA	STD	0.63	4.25	0.05	1.32	0.45	4.25	4.25	1.92	1.85	6.67	6.66	ns
	-1	0.53	3.61	0.04	1.12	0.38	3.61	3.61	1.93	1.85	5.67	5.67	ns
12 mA	STD	0.63	3.82	0.05	1.32	0.45	1.89	1.63	4.00	4.41	3.06	2.82	ns
	-1	0.53	3.25	0.04	1.12	0.38	1.89	1.63	3.41	3.75	3.06	2.82	ns
16 mA	STD	0.63	3.82	0.05	1.32	0.45	1.89	1.63	4.00	4.41	3.06	2.82	ns
	-1	0.53	3.25	0.04	1.12	0.38	1.89	1.63	3.41	3.75	3.06	2.82	ns

Notes:

1. Software default selection highlighted in gray.
2. For specific junction temperature and voltage supply levels, refer to [Table 2-5 on page 2-5](#) for derating values.

Table 2-62 • 1.8 V LVC MOS Low Slew

Automotive-Case Conditions: $T_J = 115^{\circ}\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$, Worst-Case $V_{CCI} = 2.3\text{ V}$
Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	STD	0.63	16.80	0.05	1.40	0.45	15.27	16.80	1.48	0.84	17.69	19.22	ns
	-1	0.53	14.29	0.04	1.19	0.38	12.99	14.29	1.49	0.84	15.05	16.35	ns
4 mA	STD	0.63	11.33	0.05	1.40	0.45	11.26	11.33	1.73	1.43	13.68	13.75	ns
	-1	0.53	9.64	0.04	1.19	0.38	9.58	9.64	1.73	1.43	11.64	11.70	ns
6 mA	STD	0.63	8.71	0.05	1.40	0.45	8.87	8.48	1.89	1.72	11.29	10.90	ns
	-1	0.53	7.41	0.04	1.19	0.38	7.54	7.22	1.89	1.72	9.60	9.27	ns
8 mA	STD	0.63	8.12	0.05	1.40	0.45	8.27	7.89	1.93	1.79	10.69	10.31	ns
	-1	0.53	6.90	0.04	1.19	0.38	7.03	6.72	1.93	1.79	9.09	8.77	ns
12 mA	STD	0.63	7.89	0.05	1.40	0.45	7.83	7.89	1.98	2.07	10.25	10.31	ns
	-1	0.53	6.71	0.04	1.19	0.38	6.66	6.71	1.98	2.07	8.72	8.77	ns
16 mA	STD	0.63	7.89	0.05	1.40	0.45	7.83	7.89	1.98	2.07	10.25	10.31	ns
	-1	0.53	6.71	0.04	1.19	0.38	6.66	6.71	1.98	2.07	8.72	8.77	ns

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-5 on page 2-5](#) for derating values.

Table 2-63 • 1.8 V LVC MOS High Slew

Automotive-Case Conditions: $T_J = 115^{\circ}\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$, Worst-Case $V_{CCI} = 2.3\text{ V}$
Applicable to Standard Plus I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	STD	0.63	12.83	0.05	1.32	0.45	9.44	12.26	1.20	0.80	11.86	14.68	ns
	-1	0.53	10.92	0.04	1.12	0.38	8.03	10.43	1.20	0.80	10.09	12.49	ns
4 mA	STD	0.63	7.48	0.05	1.32	0.45	5.93	7.01	1.41	1.36	8.35	9.43	ns
	-1	0.53	6.36	0.04	1.12	0.38	5.04	5.97	1.42	1.37	7.10	8.02	ns
6 mA	STD	0.63	4.81	0.05	1.32	0.45	4.15	4.39	1.57	1.63	6.57	6.81	ns
	-1	0.53	4.09	0.04	1.12	0.38	3.53	3.74	1.57	1.63	5.59	5.79	ns
8 mA	STD	0.63	4.25	0.05	1.32	0.45	4.15	4.39	1.57	1.63	6.57	6.81	ns
	-1	0.53	3.61	0.04	1.12	0.38	3.53	3.74	1.57	1.63	5.59	5.79	ns

Notes:

1. Software default selection highlighted in gray.
2. For specific junction temperature and voltage supply levels, refer to [Table 2-5 on page 2-5](#) for derating values.

Table 2-64 • 1.8 V LVCMOS Low Slew

Automotive-Case Conditions: $T_J = 115^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$, Worst-Case $V_{CCI} = 2.3\text{ V}$
Applicable to Standard Plus I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	STD	0.63	16.80	0.05	1.40	0.45	14.60	16.01	1.20	0.77	17.02	18.43	ns
	-1	0.53	14.29	0.04	1.19	0.38	12.42	13.62	1.20	0.77	14.48	15.68	ns
4 mA	STD	0.63	11.33	0.05	1.40	0.45	10.53	10.71	1.42	1.31	12.95	13.13	ns
	-1	0.53	9.64	0.04	1.19	0.38	8.96	9.11	1.42	1.31	11.01	11.17	ns
6 mA	STD	0.63	8.71	0.05	1.40	0.45	8.19	7.92	1.57	1.57	10.61	10.34	ns
	-1	0.53	7.41	0.04	1.19	0.38	6.97	6.74	1.57	1.57	9.03	8.79	ns
8 mA	STD	0.63	8.12	0.05	1.40	0.45	8.19	7.92	1.57	1.57	10.61	10.34	ns
	-1	0.53	6.90	0.04	1.19	0.38	6.97	6.74	1.57	1.57	9.03	8.79	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-5 for derating values.

1.5 V LVCMOS (JESD8-11)

Low-Voltage CMOS for 1.5 V is an extension of the LVCMOS standard (JESD8-5) used for general-purpose 1.5 V applications. It uses a 1.5 V input buffer and a push-pull output buffer.

Table 2-65 • Minimum and Maximum DC Input and Output Levels
Applicable to Advanced I/O Banks

1.5 V LVCMOS	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}	I_{OSL}	I_{OSH}	I_{IL}	I_{IH}
Drive Strength	Min., V	Max., V	Min., V	Max., V	Max., V	Min., V	mA	mA	Max., mA ¹	Max., mA ¹	μA^2	μA^2
2 mA	-0.3	$0.30 * V_{CCI}$	$0.7 * V_{CCI}$	3.6	$0.25 * V_{CCI}$	$0.75 * V_{CCI}$	2	2	16	13	10	10
4 mA	-0.3	$0.30 * V_{CCI}$	$0.7 * V_{CCI}$	3.6	$0.25 * V_{CCI}$	$0.75 * V_{CCI}$	4	4	33	25	10	10
6 mA	-0.3	$0.30 * V_{CCI}$	$0.7 * V_{CCI}$	3.6	$0.25 * V_{CCI}$	$0.75 * V_{CCI}$	6	6	39	32	10	10
8 mA	-0.3	$0.30 * V_{CCI}$	$0.7 * V_{CCI}$	3.6	$0.25 * V_{CCI}$	$0.75 * V_{CCI}$	8	8	55	66	10	10
12 mA	-0.3	$0.30 * V_{CCI}$	$0.7 * V_{CCI}$	3.6	$0.25 * V_{CCI}$	$0.75 * V_{CCI}$	12	12	55	66	10	10

Notes:

1. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.
2. Currents are measured at 125°C junction temperature.
3. Software default selection highlighted in gray.

Table 2-66 • Minimum and Maximum DC Input and Output Levels
Applicable to Standard Plus I/O Banks

1.5 V LVCMOS	V_{IL}		V_{IH}		V_{OL}	V_{OH}	I_{OL}	I_{OH}	I_{OSL}	I_{OSH}	I_{IL}	I_{IH}
Drive Strength	Min., V	Max., V	Min., V	Max., V	Max., V	Min., V	mA	mA	Max., mA ¹	Max., mA ¹	μA^2	μA^2
2 mA	-0.3	$0.30 * V_{CCI}$	$0.7 * V_{CCI}$	3.6	$0.25 * V_{CCI}$	$0.75 * V_{CCI}$	2	2	0	0	10	10
4 mA	-0.3	$0.30 * V_{CCI}$	$0.7 * V_{CCI}$	3.6	$0.25 * V_{CCI}$	$0.75 * V_{CCI}$	4	4	0	0	10	10

Notes:

1. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.
2. Currents are measured at 125°C junction temperature.
3. Software default selection highlighted in gray.

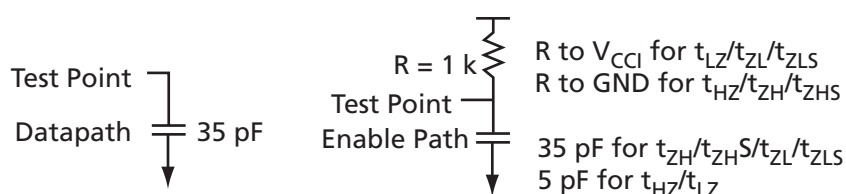


Figure 2-10 • AC Loading

Table 2-67 • AC Waveforms, Measuring Points, and Capacitive Loads

Input LOW (V)	Input HIGH (V)	Measuring Point* (V)	C_{LOAD} (pF)
0	1.5	0.75	35

* Measuring point = V_{trip} . See Table 2-18 on page 2-17 for a complete table of trip points.

Timing Characteristics

Table 2-68 • 1.5 V LVCMOS High Slew
Automotive-Case Conditions: $T_J = 135^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$, Worst-Case $V_{CCI} = 2.3\text{ V}$
Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	STD	0.64	9.35	0.05	1.61	0.46	7.63	9.35	1.87	1.50	10.13	11.851	ns
	-1	0.55	7.95	0.04	1.37	0.39	6.49	7.95	1.87	1.50	8.62	10.081	ns
4 mA	STD	0.64	5.94	0.05	1.61	0.46	5.42	5.94	2.07	1.84	7.92	8.442	ns
	-1	0.55	5.05	0.04	1.37	0.39	4.61	5.05	2.07	1.85	6.74	7.181	ns
6 mA	STD	0.64	5.22	0.05	1.61	0.46	5.09	5.22	2.11	1.93	7.59	7.718	ns
	-1	0.55	4.44	0.04	1.37	0.39	4.33	4.44	2.11	1.93	6.45	6.566	ns
8 mA	STD	0.64	4.56	0.05	1.61	0.46	2.25	1.98	4.41	4.70	3.46	3.211	ns
	-1	0.55	3.88	0.04	1.37	0.39	2.25	1.98	3.75	4.00	3.46	3.213	ns
12 mA	STD	0.64	4.56	0.05	1.61	0.46	2.25	1.98	4.41	4.70	3.46	3.211	ns
	-1	0.55	3.88	0.04	1.37	0.39	2.25	1.98	3.75	4.00	3.46	3.213	ns

Notes:

1. Software default selection highlighted in gray.
2. For specific junction temperature and voltage supply levels, refer to [Table 2-5 on page 2-5](#) for derating values.

Table 2-69 • 1.5 V LVCMOS Low Slew
Automotive-Case Conditions: $T_J = 135^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$, Worst-Case $V_{CCI} = 2.3\text{ V}$
Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	STD	0.64	14.29	0.05	1.45	0.46	14.32	14.29	1.88	1.43	16.82	16.794	ns
	-1	0.55	12.16	0.04	1.23	0.39	12.18	12.16	1.88	1.43	14.31	14.286	ns
4 mA	STD	0.64	11.19	0.05	1.45	0.46	11.40	10.67	2.07	1.77	13.90	13.175	ns
	-1	0.55	9.52	0.04	1.23	0.39	9.70	9.08	2.07	1.77	11.82	11.207	ns
6 mA	STD	0.64	10.44	0.05	1.45	0.46	10.63	9.94	2.12	1.86	13.13	12.442	ns
	-1	0.55	8.88	0.04	1.23	0.39	9.04	8.46	2.12	1.86	11.17	10.584	ns
8 mA	STD	0.64	9.96	0.05	1.45	0.46	10.15	9.94	2.18	2.19	12.65	12.445	ns
	-1	0.55	8.47	0.04	1.23	0.39	8.63	8.46	2.19	2.20	10.76	10.586	ns
12 mA	STD	0.64	9.96	0.05	1.45	0.46	10.15	9.94	2.18	2.19	12.65	12.445	ns
	-1	0.55	8.47	0.04	1.23	0.39	8.63	8.46	2.19	2.20	10.76	10.586	ns

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-5 on page 2-5](#) for derating values.

Table 2-70 • 1.5 V LVC MOS High Slew

Automotive-Case Conditions: $T_J = 135^{\circ}\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$, Worst-Case $V_{CCI} = 2.3\text{ V}$
Applicable to Standard Plus I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	STD	0.64	8.76	0.05	1.59	0.46	7.63	9.35	1.87	1.50	10.13	11.851	ns
	-1	0.55	7.45	0.04	1.35	0.39	6.49	7.95	1.87	1.50	8.62	10.081	ns
4 mA	STD	0.64	5.41	0.05	1.59	0.46	5.42	5.94	2.07	1.84	7.92	8.442	ns
	-1	0.55	4.60	0.04	1.35	0.39	4.61	5.05	2.07	1.85	6.74	7.181	ns

Notes:

1. Software default selection highlighted in gray.
2. For specific junction temperature and voltage supply levels, refer to [Table 2-5 on page 2-5](#) for derating values.

Table 2-71 • 1.5 V LVC MOS Low Slew

Automotive-Case Conditions: $T_J = 135^{\circ}\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$, Worst-Case $V_{CCI} = 2.3\text{ V}$
Applicable to Standard Plus I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	STD	0.64	13.51	0.05	1.45	0.46	14.32	14.29	1.88	1.43	16.82	16.794	ns
	-1	0.55	11.49	0.04	1.23	0.39	12.18	12.16	1.88	1.43	14.31	14.286	ns
4 mA	STD	0.64	10.38	0.05	1.45	0.46	11.40	10.67	2.07	1.77	13.90	13.175	ns
	-1	0.55	8.83	0.04	1.23	0.39	9.70	9.08	2.07	1.77	11.82	11.207	ns

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-5 on page 2-5](#) for derating values.

Table 2-72 • 1.5 V LVC MOS High Slew

Automotive-Case Conditions: $T_J = 115^{\circ}\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$, Worst-Case $V_{CCI} = 2.3\text{ V}$
Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	STD	0.63	9.05	0.05	1.56	0.45	7.38	9.05	1.81	1.45	9.80	11.47	ns
	-1	0.53	7.70	0.04	1.32	0.38	6.28	7.70	1.81	1.45	8.34	9.75	ns
4 mA	STD	0.63	5.75	0.05	1.56	0.45	5.25	5.75	2.00	1.78	7.67	8.17	ns
	-1	0.53	4.89	0.04	1.32	0.38	4.46	4.89	2.00	1.78	6.52	6.95	ns
6 mA	STD	0.63	5.05	0.05	1.56	0.45	4.92	5.05	2.04	1.87	7.34	7.47	ns
	-1	0.53	4.29	0.04	1.32	0.38	4.19	4.29	2.04	1.87	6.24	6.35	ns
8 mA	STD	0.63	4.41	0.05	1.56	0.45	2.18	1.91	4.27	4.55	3.35	3.11	ns
	-1	0.53	3.75	0.04	1.32	0.38	2.18	1.91	3.63	3.87	3.35	3.11	ns
12 mA	STD	0.63	4.41	0.05	1.56	0.45	2.18	1.91	4.27	4.55	3.35	3.11	ns
	-1	0.53	3.75	0.04	1.32	0.38	2.18	1.91	3.63	3.87	3.35	3.11	ns

Notes:

1. Software default selection highlighted in gray.
2. For specific junction temperature and voltage supply levels, refer to [Table 2-5 on page 2-5](#) for derating values.

Table 2-73 • 1.5 V LVCMOS Low Slew

Automotive-Case Conditions: $T_J = 115^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$, Worst-Case $V_{CCI} = 2.3\text{ V}$
Applicable to Advanced I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	STD	0.63	13.83	0.05	1.40	0.45	13.86	13.83	1.82	1.39	16.28	16.25	ns
	-1	0.53	11.76	0.04	1.19	0.38	11.79	11.76	1.82	1.39	13.85	13.82	ns
4 mA	STD	0.63	10.83	0.05	1.40	0.45	11.03	10.33	2.00	1.71	13.45	12.75	ns
	-1	0.53	9.21	0.04	1.19	0.38	9.38	8.79	2.01	1.72	11.44	10.84	ns
6 mA	STD	0.63	10.10	0.05	1.40	0.45	10.28	9.62	2.05	1.80	12.70	12.04	ns
	-1	0.53	8.59	0.04	1.19	0.38	8.75	8.18	2.05	1.80	10.81	10.24	ns
8 mA	STD	0.63	9.64	0.05	1.40	0.45	9.82	9.62	2.11	2.12	12.23	12.04	ns
	-1	0.53	8.20	0.04	1.19	0.38	8.35	8.18	2.11	2.12	10.41	10.24	ns
12 mA	STD	0.63	9.64	0.05	1.40	0.45	9.82	9.62	2.11	2.12	12.23	12.04	ns
	-1	0.53	8.20	0.04	1.19	0.38	8.35	8.18	2.11	2.12	10.41	10.24	ns

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-5 on page 2-5](#) for derating values.

Table 2-74 • 1.5 V LVCMOS High Slew

Automotive-Case Conditions: $T_J = 115^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$, Worst-Case $V_{CCI} = 2.3\text{ V}$
Applicable to Standard Plus I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	STD	0.63	8.47	0.05	1.54	0.45	7.38	9.05	1.81	1.45	9.80	11.47	ns
	-1	0.53	7.21	0.04	1.31	0.38	6.28	7.70	1.81	1.45	8.34	9.75	ns
4 mA	STD	0.63	5.24	0.05	1.54	0.45	5.25	5.75	2.00	1.78	7.67	8.17	ns
	-1	0.53	4.45	0.04	1.31	0.38	4.46	4.89	2.00	1.78	6.52	6.95	ns

Notes:

1. Software default selection highlighted in gray.
2. For specific junction temperature and voltage supply levels, refer to [Table 2-5 on page 2-5](#) for derating values.

Table 2-75 • 1.5 V LVCMOS Low Slew

Automotive-Case Conditions: $T_J = 115^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$, Worst-Case $V_{CCI} = 2.3\text{ V}$
Applicable to Standard Plus I/O Banks

Drive Strength	Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
2 mA	STD	0.63	13.07	0.05	1.40	0.45	13.86	13.83	1.82	1.39	16.28	16.25	ns
	-1	0.53	11.12	0.04	1.19	0.38	11.79	11.76	1.82	1.39	13.85	13.82	ns
4 mA	STD	0.63	10.04	0.05	1.40	0.45	11.03	10.33	2.00	1.71	13.45	12.75	ns
	-1	0.53	8.54	0.04	1.19	0.38	9.38	8.79	2.01	1.72	11.44	10.84	ns

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-5 on page 2-5](#) for derating values.

3.3 V PCI, 3.3 V PCI-X

The Peripheral Component Interface for 3.3 V standard specifies support for 33 MHz and 66 MHz PCI Bus applications.

Table 2-76 • Minimum and Maximum DC Input and Output Levels

3.3 V PCI/PCI-X	V _{IL}		V _{IH}		V _{OL}	V _{OH}	I _{OL}	I _{OH}	I _{OSL}	I _{OSH}	I _{IL}	I _{IH}
Drive Strength	Min, V	Max, V	Min, V	Max, V	Max, V	Min, V	mA	mA	Max, mA ¹	Max, mA ¹	μA ²	μA ²
Per PCI specification	Per PCI curves										10	10

Notes:

1. Currents are measured at high temperature (100°C junction temperature) and maximum voltage.
2. Currents are measured at 125°C junction temperature.

AC loadings are defined per the PCI/PCI-X specifications for the datapath; Actel loadings for enable path characterization are described in Figure 2-11.

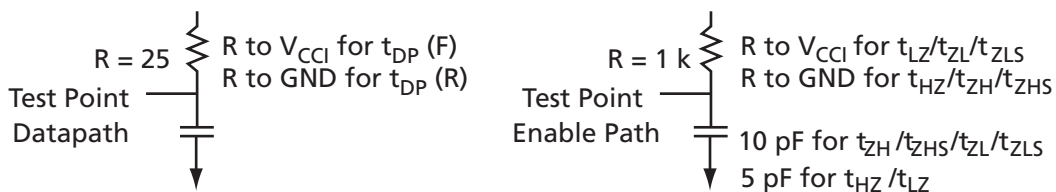


Figure 2-11 • AC Loading

AC loadings are defined per PCI/PCI-X specifications for the datapath; Actel loading for tristate is described in Table 2-77.

Table 2-77 • AC Waveforms, Measuring Points, and Capacitive Loads

Input LOW (V)	Input HIGH (V)	Measuring Point* (V)	C _{LOAD} (pF)
0	3.3	0.285 * V _{CC1} for t _{DP(R)} 0.615 * V _{CC1} for t _{DP(F)}	10

* Measuring point = V_{trip}. See Table 2-18 on page 2-17 for a complete table of trip points.

Timing Characteristics

Table 2-78 • 3.3 V PCI/PCI-X

Automotive-Case Conditions: T_J = 135°C, Worst-Case V_{CC} = 1.425 V, Worst-Case V_{CC1} = 3.0 V
Applicable to Advanced I/O Banks

Speed Grade	t _{DOUT}	t _{DP}	t _{DIN}	t _{PY}	t _{EOUT}	t _{ZL}	t _{ZH}	t _{LZ}	t _{HZ}	t _{ZLS}	t _{ZHS}	Units
Std.	0.64	2.58	0.05	0.95	0.46	1.27	0.94	3.12	3.60	2.49	2.18	ns
-1	0.55	2.19	0.04	0.81	0.39	1.27	0.94	2.65	3.06	2.49	2.18	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-5 for derating values.

Table 2-79 • 3.3 V PCI/PCI-X

Automotive-Case Conditions: $T_J = 135^{\circ}\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$, Worst-Case $V_{CCI} = 3.0\text{ V}$
Applicable to Standard Plus I/O Banks

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.64	3.00	0.05	0.93	0.46	1.27	0.94	3.12	3.60	2.49	2.18	ns
-1	0.55	2.55	0.04	0.79	0.39	1.27	0.94	2.65	3.06	2.49	2.18	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-5 for derating values.

Table 2-80 • 3.3 V PCI/PCI-X

Automotive-Case Conditions: $T_J = 115^{\circ}\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$, Worst-Case $V_{CCI} = 3.0\text{ V}$
Applicable to Advanced I/O Banks

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.628	2.50	0.05	0.92	0.45	1.23	0.91	3.02	3.48	2.40	2.11	ns
-1	0.53	2.12	0.04	0.78	0.38	1.23	0.91	2.57	2.96	2.41	2.11	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-5 for derating values.

Table 2-81 • 3.3 V PCI/PCI-X

Automotive-Case Conditions: $T_J = 115^{\circ}\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$, Worst-Case $V_{CCI} = 3.0\text{ V}$
Applicable to Standard Plus I/O Banks

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	t_{EOUT}	t_{ZL}	t_{ZH}	t_{LZ}	t_{HZ}	t_{ZLS}	t_{ZHS}	Units
Std.	0.628	2.90	0.05	0.90	0.45	1.23	0.91	3.02	3.48	2.40	2.11	ns
-1	0.53	2.47	0.04	0.77	0.38	1.23	0.91	2.57	2.96	2.41	2.11	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-5 for derating values.

Differential I/O Characteristics

Physical Implementation

Configuration of the I/O modules as a differential pair is handled by Actel Designer software when the user instantiates a differential I/O macro in the design.

Differential I/Os can also be used in conjunction with the embedded Input Register (InReg), Output Register (OutReg), Enable Register (EnReg), and Double Data Rate (DDR). However, there is no support for bidirectional I/Os or tristates with the LVPECL standards.

LVDS

Low-Voltage Differential Signaling (ANSI/TIA/EIA-644) is a high-speed, differential I/O standard. It requires that one data bit be carried through two signal lines, so two pins are needed. It also requires external resistor termination.

The full implementation of the LVDS transmitter and receiver is shown in an example in Figure 2-12 on page 2-49. The building blocks of the LVDS transmitter-receiver are one transmitter macro, one receiver macro, three board resistors at the transmitter end, and one resistor at the receiver end. The values for the three driver resistors are different from those used in the LVPECL implementation because the output standard specifications are different.

Along with LVDS I/O, ProASIC3 also supports Bus LVDS structure and Multipoint LVDS (M-LVDS) configuration (up to 40 nodes).

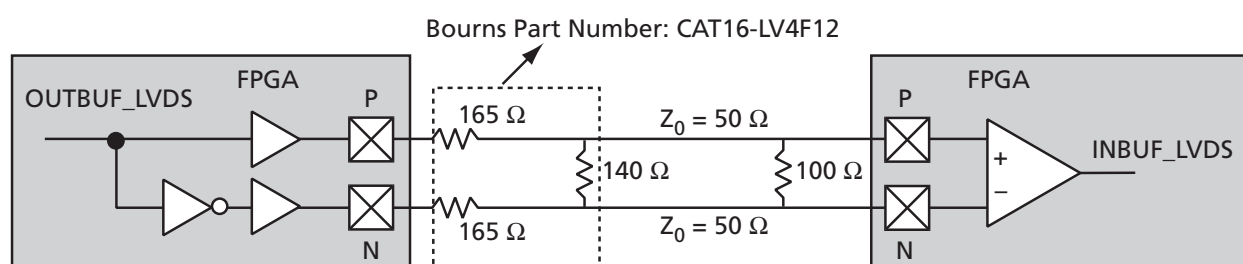


Figure 2-12 • LVDS Circuit Diagram and Board-Level Implementation

Table 2-82 • Minimum and Maximum DC Input and Output Levels

DC Parameter	Description	Min.	Typ.	Max.	Units
V_{CCI}	Supply Voltage	2.375	2.5	2.625	V
V_{OL}	Output LOW Voltage	0.9	1.075	1.25	V
V_{OH}	Output HIGH Voltage	1.25	1.425	1.6	V
V_I	Input Voltage	0	–	2.925	V
V_{ODIFF}	Differential Output Voltage	250	350	450	mV
V_{OCM}	Output Common-Mode Voltage	1.125	1.25	1.375	V
V_{ICM}	Input Common-Mode Voltage	0.05	1.25	2.35	V
V_{IDIFF}	Input Differential Voltage	100	350	–	mV

Notes:

1. $\pm 5\%$
2. Differential input voltage = ± 350 mV

Table 2-83 • AC Waveforms, Measuring Points, and Capacitive Loads

Input LOW (V)	Input HIGH (V)	Measuring Point* (V)
1.075	1.325	Cross point

* Measuring point = V_{trip} . See Table 2-18 on page 2-17 for a complete table of trip points.

Timing Characteristics

Table 2-84 • LVDS

Automotive-Case Conditions: $T_j = 135^\circ\text{C}$, Worst-Case $V_{CC} = 1.425$ V, Worst-Case $V_{CCI} = 2.3$ V

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	Units
Std.	0.64	2.05	0.05	1.79	ns
–1	0.55	1.74	0.04	1.52	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-5 for derating values.

Table 2-85 • LVDS

Automotive-Case Conditions: $T_J = 115^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$, Worst-Case $V_{CCI} = 2.3\text{ V}$

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	Units
Std.	0.63	1.98	0.05	1.73	ns
-1	0.53	1.68	0.04	1.47	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-5 for derating values.

B-LVDS/M-LVDS

Bus LVDS (B-LVDS) and Multipoint LVDS (M-LVDS) specifications extend the existing LVDS standard to high-performance multipoint bus applications. Multidrop and multipoint bus configurations may contain any combination of drivers, receivers, and transceivers. Actel LVDS drivers provide the higher drive current required by B-LVDS and M-LVDS to accommodate the loading. The drivers require series terminations for better signal quality and to control voltage swing. Termination is also required at both ends of the bus since the driver can be located anywhere on the bus. These configurations can be implemented using the TRIBUF_LVDS and BIBUF_LVDS macros along with appropriate terminations. Multipoint designs using Actel LVDS macros can achieve up to 200 MHz with a maximum of 20 loads. A sample application is given in Figure 2-13. The input and output buffer delays are available in the LVDS section in Table 2-84 on page 2-49.

Example: For a bus consisting of 20 equidistant loads, the following terminations provide the required differential voltage, in worst-case Industrial operating conditions, at the farthest receiver: $R_S = 60\ \Omega$ and $R_T = 70\ \Omega$, given $Z_0 = 50\ \Omega$ (2") and $Z_{stub} = 50\ \Omega$ (~1.5").

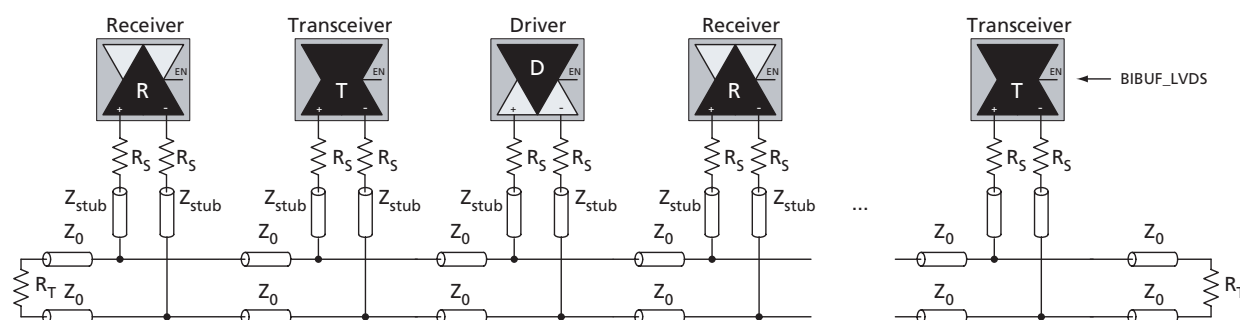


Figure 2-13 • B-LVDS/M-LVDS Multipoint Application Using LVDS I/O Buffers

LVPECL

Low-Voltage Positive Emitter-Coupled Logic (LVPECL) is another differential I/O standard. It requires that one data bit be carried through two signal lines. Like LVDS, two pins are needed. It also requires external resistor termination.

The full implementation of the LVDS transmitter and receiver is shown in an example in Figure 2-14 on page 2-51. The building blocks of the LVPECL transmitter-receiver are one transmitter macro, one receiver macro, three board resistors at the transmitter end, and one resistor at the receiver end. The values for the three driver resistors are different from those used in the LVDS implementation because the output standard specifications are different.

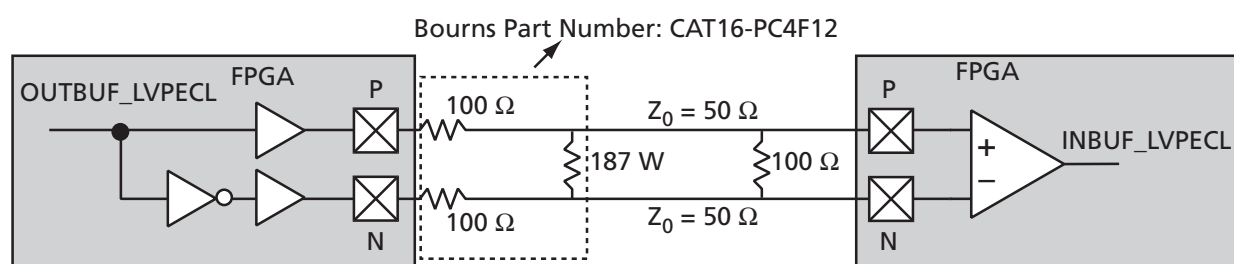


Figure 2-14 • LVPECL Circuit Diagram and Board-Level Implementation

Table 2-86 • Minimum and Maximum DC Input and Output Levels

DC Parameter	Description	Min.	Max.	Min.	Max.	Min.	Max.	Units
V_{CCI}	Supply Voltage	3.0		3.3		3.6		V
V_{OL}	Output LOW Voltage	0.96	1.27	1.06	1.43	1.30	1.57	V
V_{OH}	Output HIGH Voltage	1.8	2.11	1.92	2.28	2.13	2.41	V
V_{IL}, V_{IH}	Input LOW, Input HIGH Voltages	0	3.3	0	3.6	0	3.9	V
V_{ODIFF}	Differential Output Voltage	0.625	0.97	0.625	0.97	0.625	0.97	V
V_{OCM}	Output Common-Mode Voltage	1.762	1.98	1.762	1.98	1.762	1.98	V
V_{ICM}	Input Common-Mode Voltage	1.01	2.57	1.01	2.57	1.01	2.57	V
V_{IDIFF}	Input Differential Voltage	300		300		300		mV

Table 2-87 • AC Waveforms, Measuring Points, and Capacitive Loads

Input LOW (V)	Input HIGH (V)	Measuring Point* (V)
1.64	1.94	Cross point

* Measuring point = V_{trip} . See Table 2-18 on page 2-17 for a complete table of trip points.

Timing Characteristics

Table 2-88 • LVPECL

Automotive-Case Conditions: $T_J = 135^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$, Worst-Case $V_{CCI} = 3.0\text{ V}$

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	Units
Std.	0.64	2.01	0.05	1.57	ns
-1	0.55	1.71	0.04	1.34	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-5 for derating values.

Table 2-89 • LVPECL

Automotive-Case Conditions: $T_J = 115^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$, Worst-Case $V_{CCI} = 3.0\text{ V}$

Speed Grade	t_{DOUT}	t_{DP}	t_{DIN}	t_{PY}	Units
Std.	0.63	1.95	0.05	1.52	ns
-1	0.53	1.66	0.04	1.29	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-5 for derating values.

I/O Register Specifications

Fully Registered I/O Buffers with Synchronous Enable and Asynchronous Preset

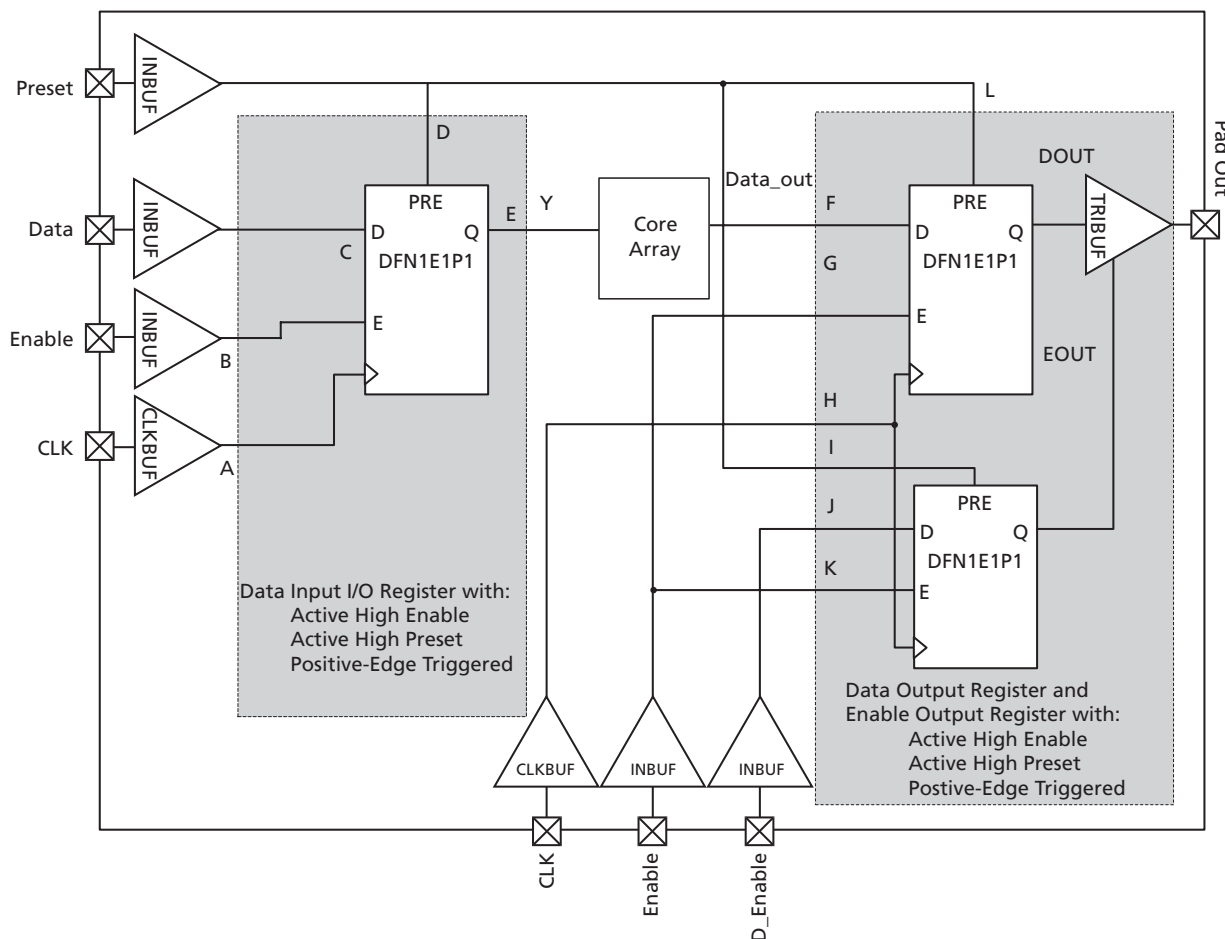


Figure 2-15 • Timing Model of Registered I/O Buffers with Synchronous Enable and Asynchronous Preset

Table 2-90 • Parameter Definition and Measuring Nodes

Parameter Name	Parameter Definition	Measuring Nodes (from, to)*
t _{OCLKQ}	Clock-to-Q of the Output Data Register	H, DOUT
t _{OSUD}	Data Setup Time for the Output Data Register	F, H
t _{OHD}	Data Hold Time for the Output Data Register	F, H
t _{OSUE}	Enable Setup Time for the Output Data Register	G, H
t _{OHE}	Enable Hold Time for the Output Data Register	G, H
t _{OPRE2Q}	Asynchronous Preset-to-Q of the Output Data Register	L, DOUT
t _{OREMPRE}	Asynchronous Preset Removal Time for the Output Data Register	L, H
t _{ORECPRE}	Asynchronous Preset Recovery Time for the Output Data Register	L, H
t _{OCLKQ}	Clock-to-Q of the Output Enable Register	H, EOUT
t _{OESUD}	Data Setup Time for the Output Enable Register	J, H
t _{OEH}	Data Hold Time for the Output Enable Register	J, H
t _{OESUE}	Enable Setup Time for the Output Enable Register	K, H
t _{OEH}	Enable Hold Time for the Output Enable Register	K, H
t _{OEPRE2Q}	Asynchronous Preset-to-Q of the Output Enable Register	I, EOUT
t _{OEREMPRE}	Asynchronous Preset Removal Time for the Output Enable Register	I, H
t _{OERECPRE}	Asynchronous Preset Recovery Time for the Output Enable Register	I, H
t _{ICLKQ}	Clock-to-Q of the Input Data Register	A, E
t _{ISUD}	Data Setup Time for the Input Data Register	C, A
t _{IHD}	Data Hold Time for the Input Data Register	C, A
t _{ISUE}	Enable Setup Time for the Input Data Register	B, A
t _{IHE}	Enable Hold Time for the Input Data Register	B, A
t _{IPRE2Q}	Asynchronous Preset-to-Q of the Input Data Register	D, E
t _{IEMPRE}	Asynchronous Preset Removal Time for the Input Data Register	D, A
t _{IETCPRE}	Asynchronous Preset Recovery Time for the Input Data Register	D, A

* See Figure 2-15 on page 2-52 for more information.

Fully Registered I/O Buffers with Synchronous Enable and Asynchronous Clear

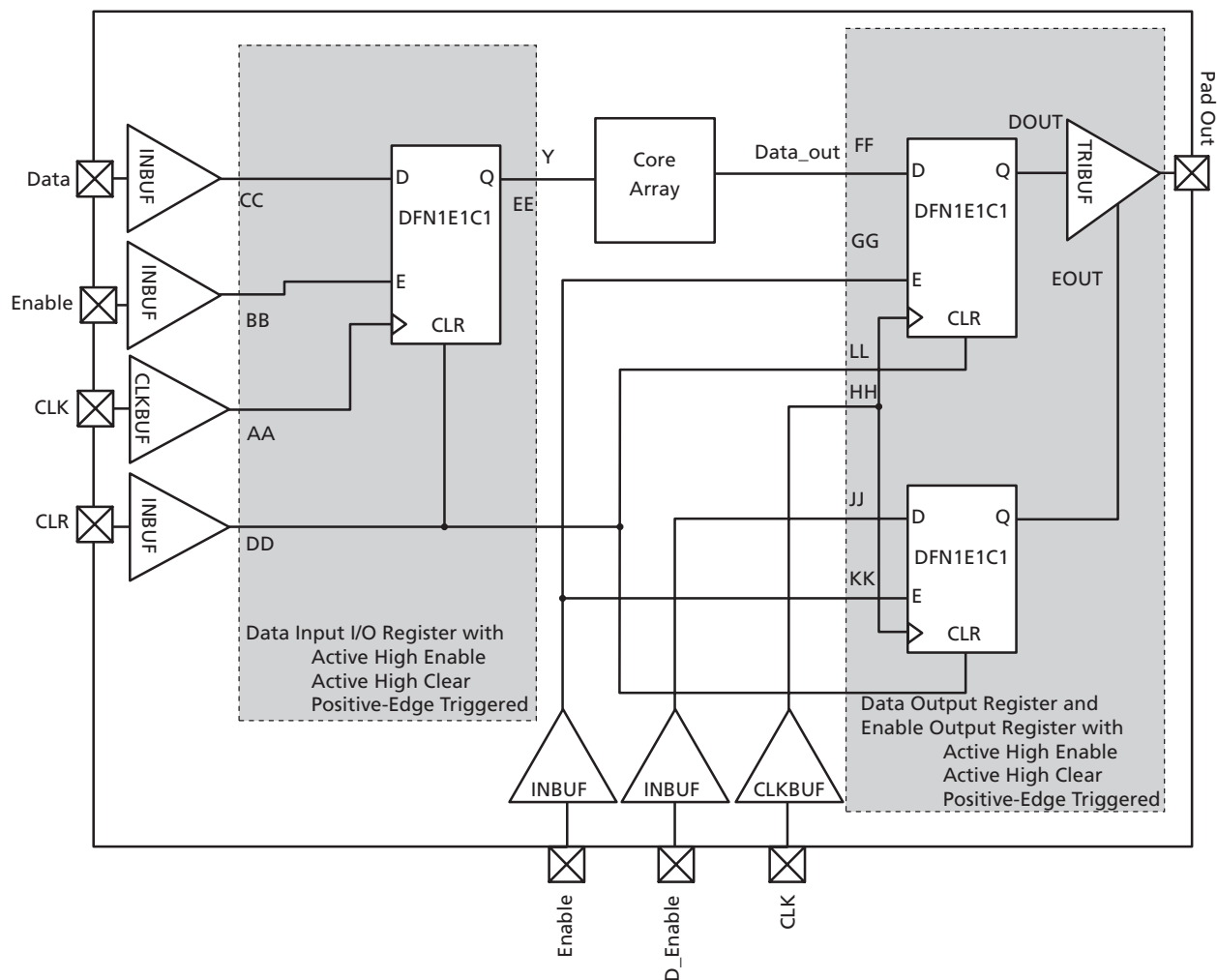


Figure 2-16 • Timing Model of the Registered I/O Buffers with Synchronous Enable and Asynchronous Clear

Table 2-91 • Parameter Definitions and Measuring Nodes

Parameter Name	Parameter Definition	Measuring Nodes (from, to)*
t _{OCLKQ}	Clock-to-Q of the Output Data Register	HH, DOUT
t _{OSUD}	Data Setup Time for the Output Data Register	FF, HH
t _{OHD}	Data Hold Time for the Output Data Register	FF, HH
t _{OSUE}	Enable Setup Time for the Output Data Register	GG, HH
t _{OHE}	Enable Hold Time for the Output Data Register	GG, HH
t _{OCLR2Q}	Asynchronous Clear-to-Q of the Output Data Register	LL, DOUT
t _{OREMCLR}	Asynchronous Clear Removal Time for the Output Data Register	LL, HH
t _{ORECCLR}	Asynchronous Clear Recovery Time for the Output Data Register	LL, HH
t _{OCLKQ}	Clock-to-Q of the Output Enable Register	HH, EOUT
t _{OSUD}	Data Setup Time for the Output Enable Register	JJ, HH
t _{OHD}	Data Hold Time for the Output Enable Register	JJ, HH
t _{OSUE}	Enable Setup Time for the Output Enable Register	KK, HH
t _{OHE}	Enable Hold Time for the Output Enable Register	KK, HH
t _{OCLR2Q}	Asynchronous Clear-to-Q of the Output Enable Register	II, EOUT
t _{OREMCLR}	Asynchronous Clear Removal Time for the Output Enable Register	II, HH
t _{ORECCLR}	Asynchronous Clear Recovery Time for the Output Enable Register	II, HH
t _{ICLKQ}	Clock-to-Q of the Input Data Register	AA, EE
t _{ISUD}	Data Setup Time for the Input Data Register	CC, AA
t _{IHD}	Data Hold Time for the Input Data Register	CC, AA
t _{ISUE}	Enable Setup Time for the Input Data Register	BB, AA
t _{IHE}	Enable Hold Time for the Input Data Register	BB, AA
t _{ICLR2Q}	Asynchronous Clear-to-Q of the Input Data Register	DD, EE
t _{IEMCLR}	Asynchronous Clear Removal Time for the Input Data Register	DD, AA
t _{IRECCLR}	Asynchronous Clear Recovery Time for the Input Data Register	DD, AA

* See Figure 2-16 on page 2-54 for more information.

Input Register

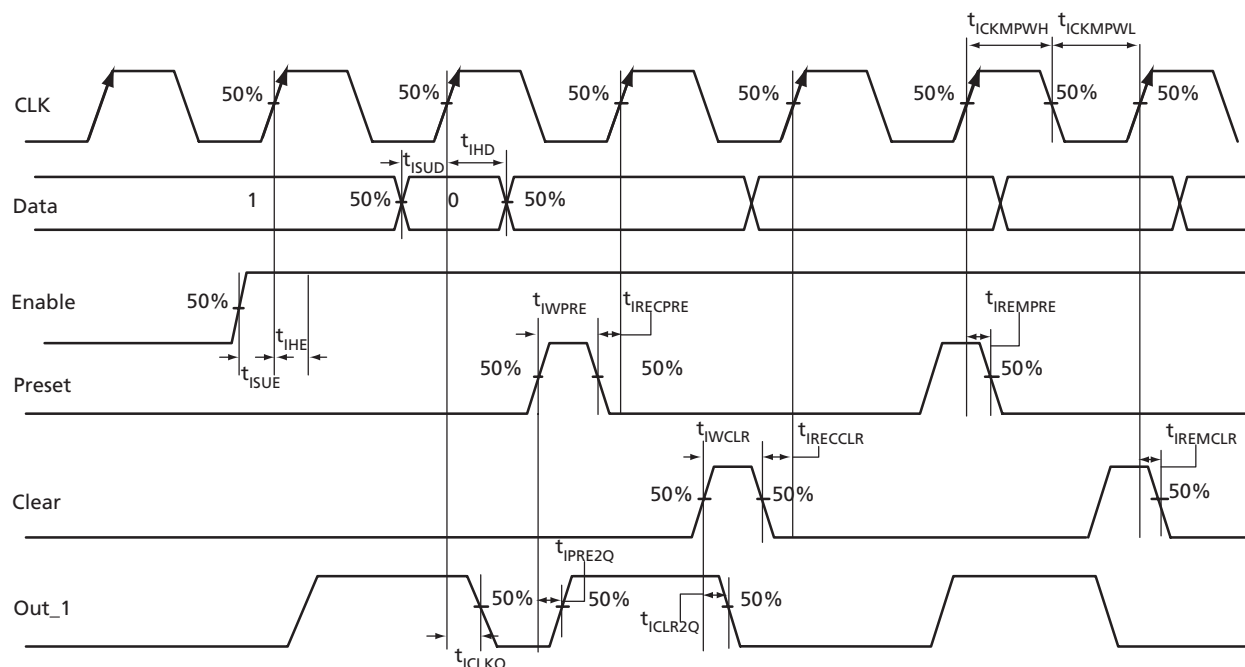


Figure 2-17 • Input Register Timing Diagram

Timing Characteristics

Table 2-92 • Input Data Register Propagation Delays
Automotive-Case Conditions: $T_J = 135^{\circ}\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$

Parameter	Description	-1	Std.	Units
t_{CLKQ}	Clock-to-Q of the Input Data Register	0.29	0.34	ns
t_{ISUD}	Data Setup Time for the Input Data Register	0.32	0.38	ns
t_{IHD}	Data Hold Time for the Input Data Register	0.00	0.00	ns
t_{ISUE}	Enable Setup Time for the Input Data Register	0.45	0.53	ns
t_{IHE}	Enable Hold Time for the Input Data Register	0.00	0.00	ns
t_{ICLR2Q}	Asynchronous Clear-to-Q of the Input Data Register	0.55	0.65	ns
t_{IPRE2Q}	Asynchronous Preset-to-Q of the Input Data Register	0.55	0.65	ns
t_{IEMCLR}	Asynchronous Clear Removal Time for the Input Data Register	0.00	0.00	ns
t_{IRECCLR}	Asynchronous Clear Recovery Time for the Input Data Register	0.27	0.32	ns
t_{IREMPRE}	Asynchronous Preset Removal Time for the Input Data Register	0.00	0.00	ns
t_{IRECPRE}	Asynchronous Preset Recovery Time for the Input Data Register	0.27	0.32	ns
t_{IWCLR}	Asynchronous Clear Minimum Pulse Width for the Input Data Register	0.25	0.30	ns
t_{IWPRE}	Asynchronous Preset Minimum Pulse Width for the Input Data Register	0.25	0.30	ns
t_{ICKMPWH}	Clock Minimum Pulse Width HIGH for the Input Data Register	0.41	0.48	ns
t_{ICKMPWL}	Clock Minimum Pulse Width LOW for the Input Data Register	0.37	0.43	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-5 for derating values.

Table 2-93 • Input Data Register Propagation Delays
Automotive-Case Conditions: $T_J = 115^{\circ}\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$

Parameter	Description	-1	Std.	Units
t _{1CLKQ}	Clock-to-Q of the Input Data Register	0.29	0.34	ns
t _{1SUD}	Data Setup Time for the Input Data Register	0.31	0.37	ns
t _{1HD}	Data Hold Time for the Input Data Register	0.00	0.00	ns
t _{1SUE}	Enable Setup Time for the Input Data Register	0.44	0.52	ns
t _{1HE}	Enable Hold Time for the Input Data Register	0.00	0.00	ns
t _{1CLR2Q}	Asynchronous Clear-to-Q of the Input Data Register	0.54	0.64	ns
t _{1PRE2Q}	Asynchronous Preset-to-Q of the Input Data Register	0.54	0.64	ns
t _{1REMCLR}	Asynchronous Clear Removal Time for the Input Data Register	0.00	0.00	ns
t _{1RECCLR}	Asynchronous Clear Recovery Time for the Input Data Register	0.27	0.31	ns
t _{1REMPRE}	Asynchronous Preset Removal Time for the Input Data Register	0.00	0.00	ns
t _{1RECPRE}	Asynchronous Preset Recovery Time for the Input Data Register	0.27	0.31	ns
t _{1IWCLR}	Asynchronous Clear Minimum Pulse Width for the Input Data Register	0.25	0.30	ns
t _{1IWPRE}	Asynchronous Preset Minimum Pulse Width for the Input Data Register	0.25	0.30	ns
t _{1CKMPWH}	Clock Minimum Pulse Width HIGH for the Input Data Register	0.41	0.48	ns
t _{1CKMPWL}	Clock Minimum Pulse Width LOW for the Input Data Register	0.37	0.43	ns

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-5 on page 2-5](#) for derating values.

Output Register

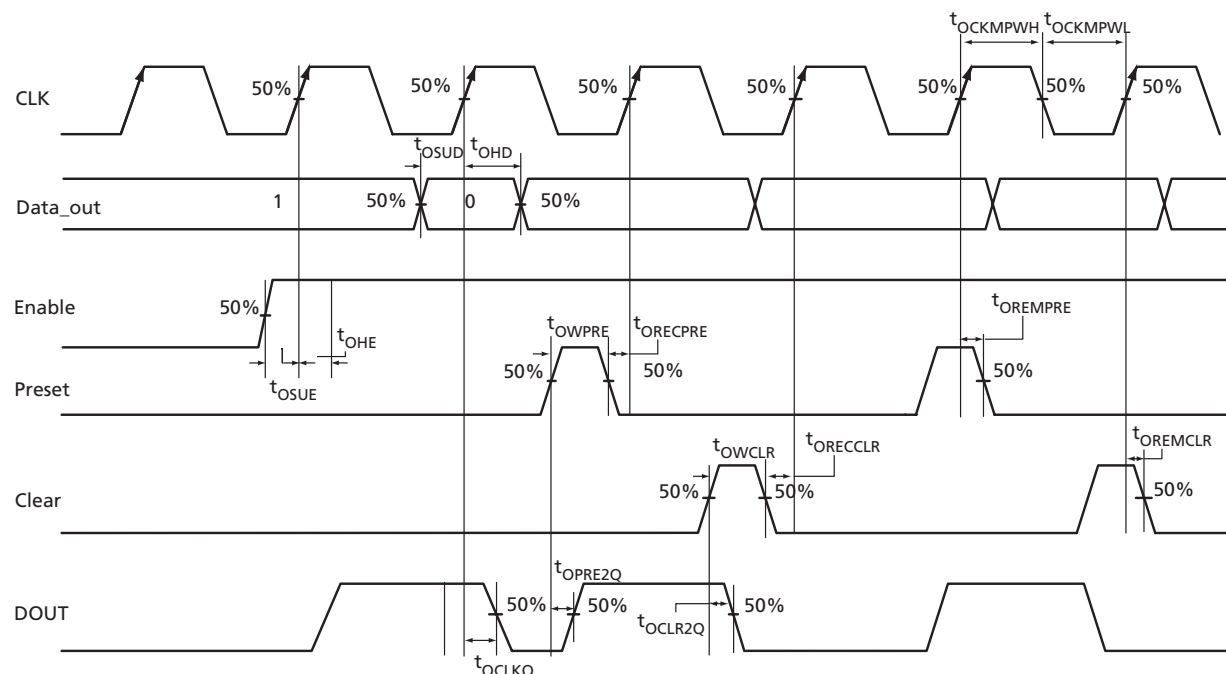


Figure 2-18 • Output Register Timing Diagram

Timing Characteristics

Table 2-94 • Output Data Register Propagation Delays
Automotive-Case Conditions: $T_J = 135^{\circ}\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$

Parameter	Description	-1	Std.	Units
t_{OCLKQ}	Clock-to-Q of the Output Data Register	0.72	0.84	ns
t_{OSUD}	Data Setup Time for the Output Data Register	0.38	0.45	ns
t_{OHD}	Data Hold Time for the Output Data Register	0.00	0.00	ns
t_{OSUE}	Enable Setup Time for the Output Data Register	0.53	0.63	ns
t_{OHE}	Enable Hold Time for the Output Data Register	0.00	0.00	ns
t_{OCLR2Q}	Asynchronous Clear-to-Q of the Output Data Register	0.98	1.15	ns
t_{OPRE2Q}	Asynchronous Preset-to-Q of the Output Data Register	0.98	1.15	ns
t_{OREMCLR}	Asynchronous Clear Removal Time for the Output Data Register	0.00	0.00	ns
t_{ORECCLR}	Asynchronous Clear Recovery Time for the Output Data Register	0.27	0.32	ns
t_{OREMPRE}	Asynchronous Preset Removal Time for the Output Data Register	0.00	0.00	ns
t_{ORECPRE}	Asynchronous Preset Recovery Time for the Output Data Register	0.27	0.32	ns
t_{OWCLR}	Asynchronous Clear Minimum Pulse Width for the Output Data Register	0.25	0.30	ns
t_{OWPRE}	Asynchronous Preset Minimum Pulse Width for the Output Data Register	0.25	0.30	ns
t_{OCKMPWH}	Clock Minimum Pulse Width HIGH for the Output Data Register	0.41	0.48	ns
t_{OCKMPWL}	Clock Minimum Pulse Width LOW for the Output Data Register	0.37	0.43	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-5 for derating values.

Table 2-95 • Output Data Register Propagation Delays
Automotive-Case Conditions: $T_J = 115^{\circ}\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$

Parameter	Description	-1	Std.	Units
t_{OCLKQ}	Clock-to-Q of the Output Data Register	0.70	0.82	ns
t_{OSUD}	Data Setup Time for the Output Data Register	0.37	0.44	ns
t_{OHD}	Data Hold Time for the Output Data Register	0.00	0.00	ns
t_{OSUE}	Enable Setup Time for the Output Data Register	0.52	0.61	ns
t_{OHE}	Enable Hold Time for the Output Data Register	0.00	0.00	ns
t_{OCLR2Q}	Asynchronous Clear-to-Q of the Output Data Register	0.96	1.12	ns
t_{OPRE2Q}	Asynchronous Preset-to-Q of the Output Data Register	0.96	1.12	ns
t_{OREMCLR}	Asynchronous Clear Removal Time for the Output Data Register	0.00	0.00	ns
t_{ORECCLR}	Asynchronous Clear Recovery Time for the Output Data Register	0.27	0.31	ns
t_{OREMPRE}	Asynchronous Preset Removal Time for the Output Data Register	0.00	0.00	ns
t_{ORECPRE}	Asynchronous Preset Recovery Time for the Output Data Register	0.27	0.31	ns
t_{OWCLR}	Asynchronous Clear Minimum Pulse Width for the Output Data Register	0.25	0.30	ns
t_{OWPRE}	Asynchronous Preset Minimum Pulse Width for the Output Data Register	0.25	0.30	ns
t_{OCKMPWH}	Clock Minimum Pulse Width HIGH for the Output Data Register	0.41	0.48	ns
t_{OCKMPWL}	Clock Minimum Pulse Width LOW for the Output Data Register	0.37	0.43	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-5 for derating values.

Output Enable Register

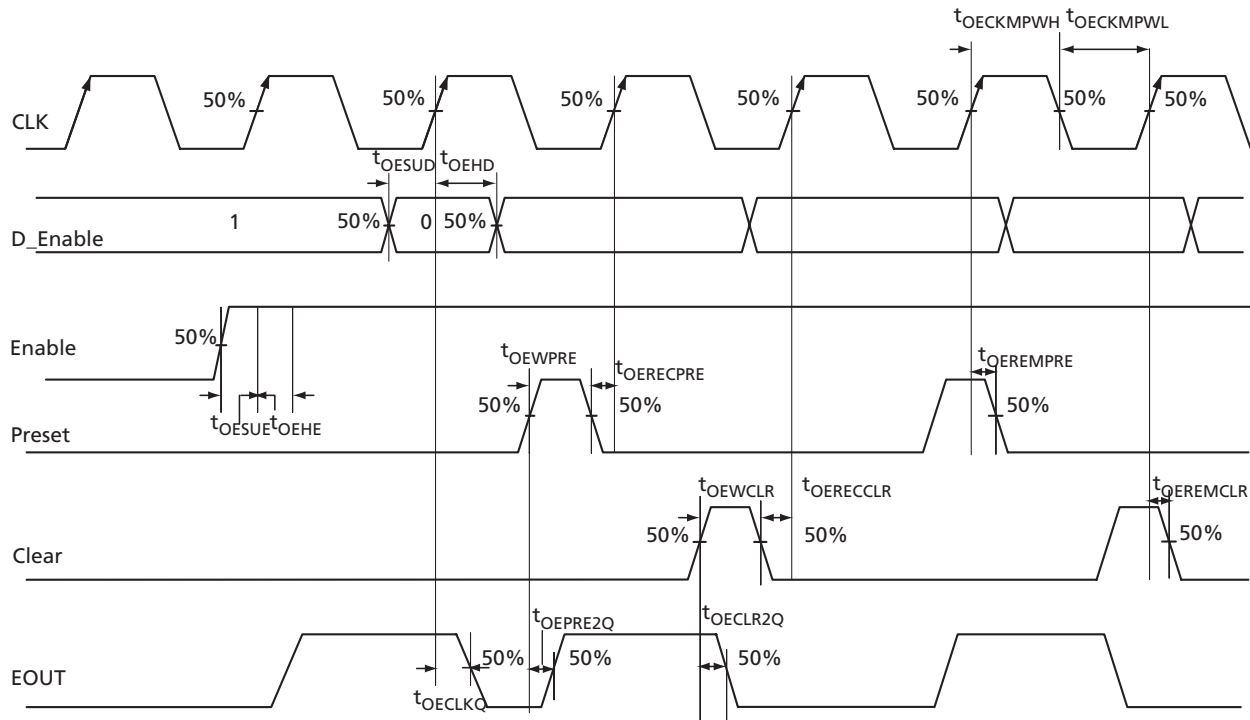


Figure 2-19 • Output Enable Register Timing Diagram

Timing Characteristics

Table 2-96 • Output Enable Register Propagation Delays
Automotive-Case Conditions: $T_j = 135^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$

Parameter	Description	-1	Std.	Units
t_{OECLKQ}	Clock-to-Q of the Output Enable Register	0.54	0.64	ns
t_{OESUD}	Data Setup Time for the Output Enable Register	0.38	0.45	ns
t_{OEHD}	Data Hold Time for the Output Enable Register	0.00	0.00	ns
t_{OESUE}	Enable Setup Time for the Output Enable Register	0.53	0.62	ns
t_{OEHE}	Enable Hold Time for the Output Enable Register	0.00	0.00	ns
$t_{OECLR2Q}$	Asynchronous Clear-to-Q of the Output Enable Register	0.81	0.95	ns
$t_{OEPRE2Q}$	Asynchronous Preset-to-Q of the Output Enable Register	0.81	0.95	ns
$t_{OEREMCLR}$	Asynchronous Clear Removal Time for the Output Enable Register	0.00	0.00	ns
$t_{OERECCLR}$	Asynchronous Clear Recovery Time for the Output Enable Register	0.27	0.32	ns
$t_{OEREMPRE}$	Asynchronous Preset Removal Time for the Output Enable Register	0.00	0.00	ns
$t_{OERECPRE}$	Asynchronous Preset Recovery Time for the Output Enable Register	0.27	0.32	ns
t_{OEWCLR}	Asynchronous Clear Minimum Pulse Width for the Output Enable Register	0.25	0.30	ns
t_{OEWPRE}	Asynchronous Preset Minimum Pulse Width for the Output Enable Register	0.25	0.30	ns
$t_{OECKMPWH}$	Clock Minimum Pulse Width HIGH for the Output Enable Register	0.41	0.48	ns
$t_{OECKMPWL}$	Clock Minimum Pulse Width LOW for the Output Enable Register	0.37	0.43	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-5 for derating values.

Table 2-97 • Output Enable Register Propagation Delays
Automotive-Case Conditions: $T_J = 115^{\circ}\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$

Parameter	Description	–1	Std.	Units
t_{OECLKQ}	Clock-to-Q of the Output Enable Register	0.53	0.62	ns
t_{OESUD}	Data Setup Time for the Output Enable Register	0.37	0.44	ns
t_{OEHD}	Data Hold Time for the Output Enable Register	0.00	0.00	ns
t_{OESUE}	Enable Setup Time for the Output Enable Register	0.52	0.61	ns
t_{OEHE}	Enable Hold Time for the Output Enable Register	0.00	0.00	ns
$t_{OECLR2Q}$	Asynchronous Clear-to-Q of the Output Enable Register	0.79	0.93	ns
$t_{OEPRE2Q}$	Asynchronous Preset-to-Q of the Output Enable Register	0.79	0.93	ns
$t_{OEREMCLR}$	Asynchronous Clear Removal Time for the Output Enable Register	0.00	0.00	ns
$t_{OERECLR}$	Asynchronous Clear Recovery Time for the Output Enable Register	0.27	0.31	ns
$t_{OEREMPRE}$	Asynchronous Preset Removal Time for the Output Enable Register	0.00	0.00	ns
$t_{OERCPRE}$	Asynchronous Preset Recovery Time for the Output Enable Register	0.27	0.31	ns
$t_{OEWCCLR}$	Asynchronous Clear Minimum Pulse Width for the Output Enable Register	0.25	0.30	ns
$t_{OEWCPRE}$	Asynchronous Preset Minimum Pulse Width for the Output Enable Register	0.25	0.30	ns
$t_{OECKMPWH}$	Clock Minimum Pulse Width HIGH for the Output Enable Register	0.41	0.48	ns
$t_{OECKMPWL}$	Clock Minimum Pulse Width LOW for the Output Enable Register	0.37	0.43	ns

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-5 on page 2-5](#) for derating values.

DDR Module Specifications

Input DDR Module

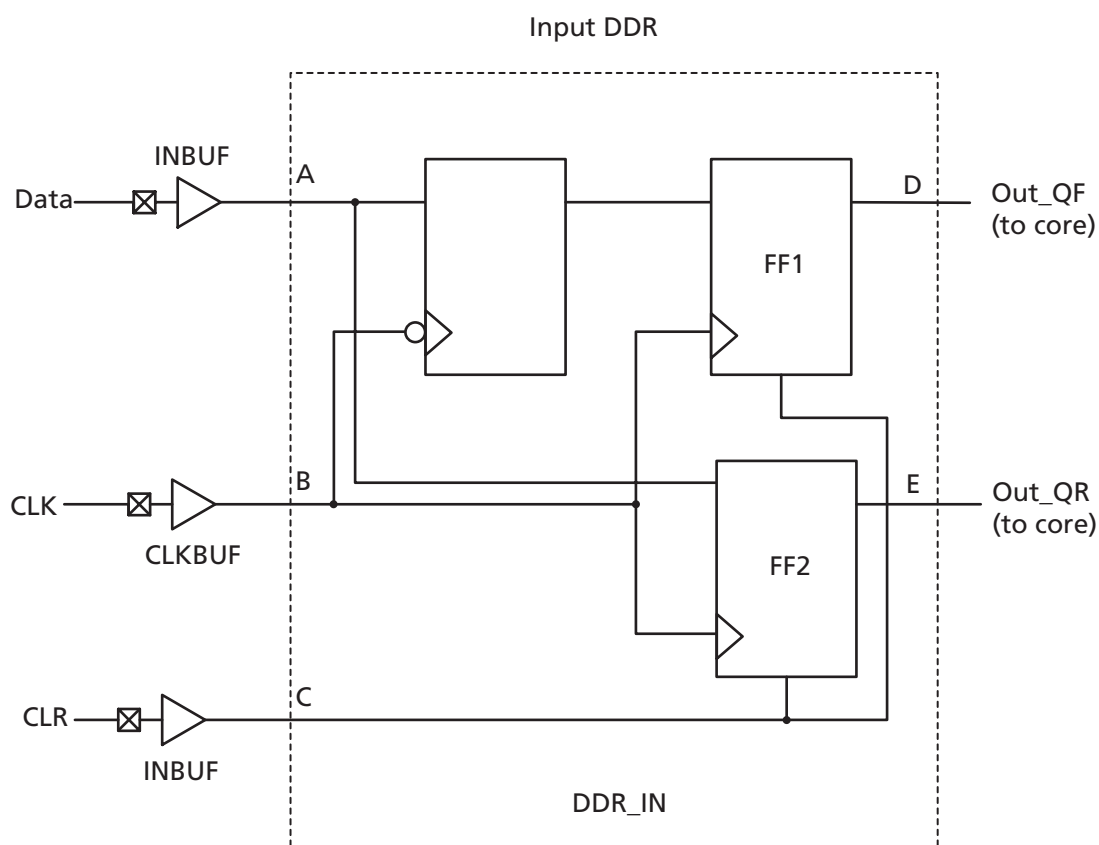


Figure 2-20 • Input DDR Timing Model

Table 2-98 • Parameter Definitions

Parameter Name	Parameter Definition	Measuring Nodes (from, to)
$t_{DDRICKQ1}$	Clock-to-Out Out_QR	B, D
$t_{DDRICKQ2}$	Clock-to-Out Out_QF	B, E
$t_{DDRISUD}$	Data Setup Time of DDR Input	A, B
t_{DDRIHD}	Data Hold Time of DDR Input	A, B
$t_{DDRICLR2Q1}$	Clear-to-Out Out_QR	C, D
$t_{DDRICLR2Q2}$	Clear-to-Out Out_QF	C, E
$t_{DDRIREMCLR}$	Clear Removal	C, B
$t_{DDRIRECCLR}$	Clear Recovery	C, B

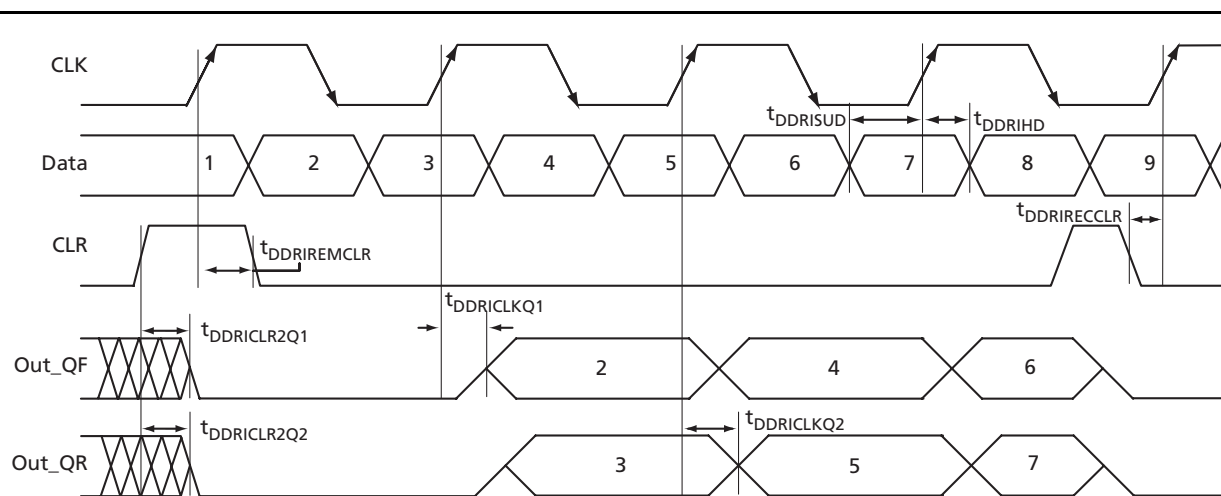


Figure 2-21 • Input DDR Timing Diagram

Timing Characteristics

Table 2-99 • Input DDR Propagation Delays

Automotive-Case Conditions: $T_J = 135^{\circ}\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$

Parameter	Description	-1	Std.	Units
t_{DDRICKQ1}	Clock-to-Out Out_QR for Input DDR	0.33	0.39	ns
t_{DDRICKQ2}	Clock-to-Out Out_QF for Input DDR	0.47	0.56	ns
t_{DDRISUD}	Data Setup for Input DDR	0.34	0.40	ns
t_{DDRIHD}	Data Hold for Input DDR	0.00	0.00	ns
$t_{\text{DDRICLR2Q1}}$	Asynchronous Clear-to-Out Out_QR for Input DDR	0.56	0.66	ns
$t_{\text{DDRICLR2Q2}}$	Asynchronous Clear-to-Out Out_QF for Input DDR	0.69	0.82	ns
$t_{\text{DDRIEMCLR}}$	Asynchronous Clear Removal Time for Input DDR	0.00	0.00	ns
$t_{\text{DDRIECCLR}}$	Asynchronous Clear Recovery Time for Input DDR	0.27	0.32	ns
t_{DDRIWCLR}	Asynchronous Clear Minimum Pulse Width for Input DDR	0.25	0.30	ns
$t_{\text{DDRICKMPWH}}$	Clock Minimum Pulse Width HIGH for Input DDR	0.41	0.48	ns
$t_{\text{DDRICKMPWL}}$	Clock Minimum Pulse Width LOW for Input DDR	0.37	0.43	ns
F_{DDRIMAX}	Maximum Frequency for Input DDR	TBD	TBD	MHz

Note: For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-5 for derating values.

Table 2-100 • Input DDR Propagation Delays

Automotive-Case Conditions: $T_J = 115^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$

Parameter	Description	-1	Std.	Units
$t_{\text{DDRICKLQ1}}$	Clock-to-Out Out_QR for Input DDR	0.33	0.38	ns
$t_{\text{DDRICKLQ2}}$	Clock-to-Out Out_QF for Input DDR	0.46	0.54	ns
t_{DDRISUD}	Data Setup for Input DDR	0.34	0.40	ns
t_{DDRiHD}	Data Hold for Input DDR	0.00	0.00	ns
$t_{\text{DDRICLR2Q1}}$	Asynchronous Clear-to-Out Out_QR for Input DDR	0.55	0.65	ns
$t_{\text{DDRICLR2Q2}}$	Asynchronous Clear-to-Out Out_QF for Input DDR	0.68	0.80	ns
$t_{\text{DDRIREMCLR}}$	Asynchronous Clear Removal Time for Input DDR	0.00	0.00	ns
$t_{\text{DDRIRECCLR}}$	Asynchronous Clear Recovery Time for Input DDR	0.27	0.31	ns
t_{DDRiWCLR}	Asynchronous Clear Minimum Pulse Width for Input DDR	0.25	0.30	ns
$t_{\text{DDRICKMPWH}}$	Clock Minimum Pulse Width HIGH for Input DDR	0.41	0.48	ns
$t_{\text{DDRICKMPWL}}$	Clock Minimum Pulse Width LOW for Input DDR	0.37	0.43	ns
F_{DDRIMAX}	Maximum Frequency for Input DDR	TBD	TBD	MHz

Note: For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-5 for derating values.

Output DDR Module

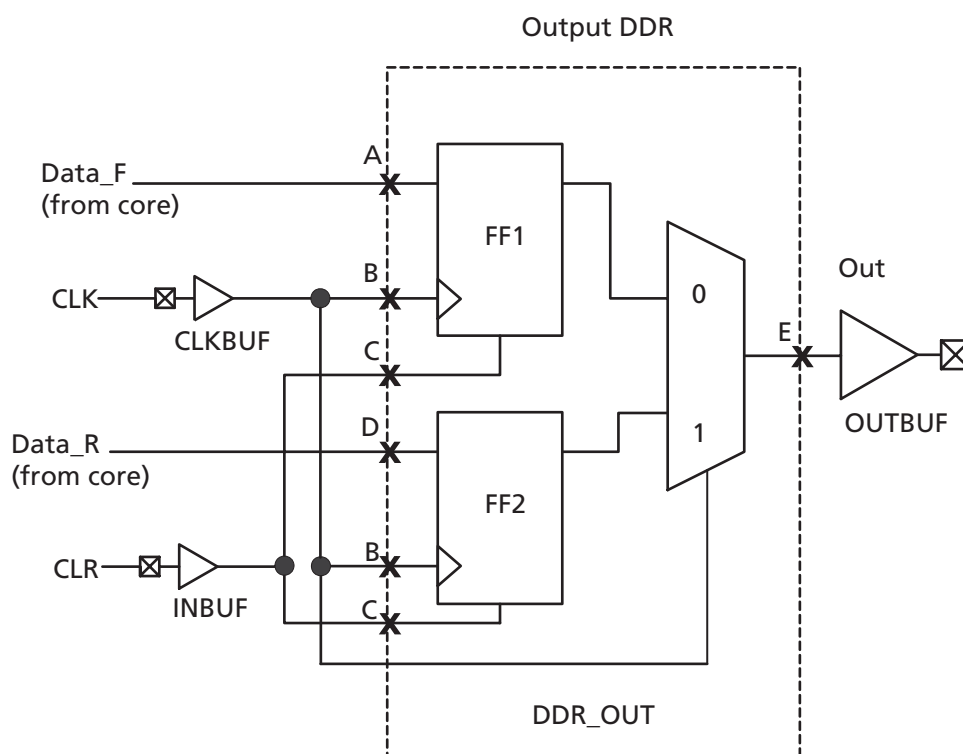


Figure 2-22 • Output DDR Timing Model

Table 2-101 • Parameter Definitions

Parameter Name	Parameter Definition	Measuring Nodes (from, to)
t_{DDROCLKQ}	Clock-to-Out	B, E
$t_{\text{DDROCLR2Q}}$	Asynchronous Clear-to-Out	C, E
$t_{\text{DDROREMCLR}}$	Clear Removal	C, B
$t_{\text{DDROECCLR}}$	Clear Recovery	C, B
t_{DDROSUD1}	Data Setup Data_F	A, B
t_{DDROSUD2}	Data Setup Data_R	D, B
t_{DDROHD1}	Data Hold Data_F	A, B
t_{DDROHD2}	Data Hold Data_R	D, B

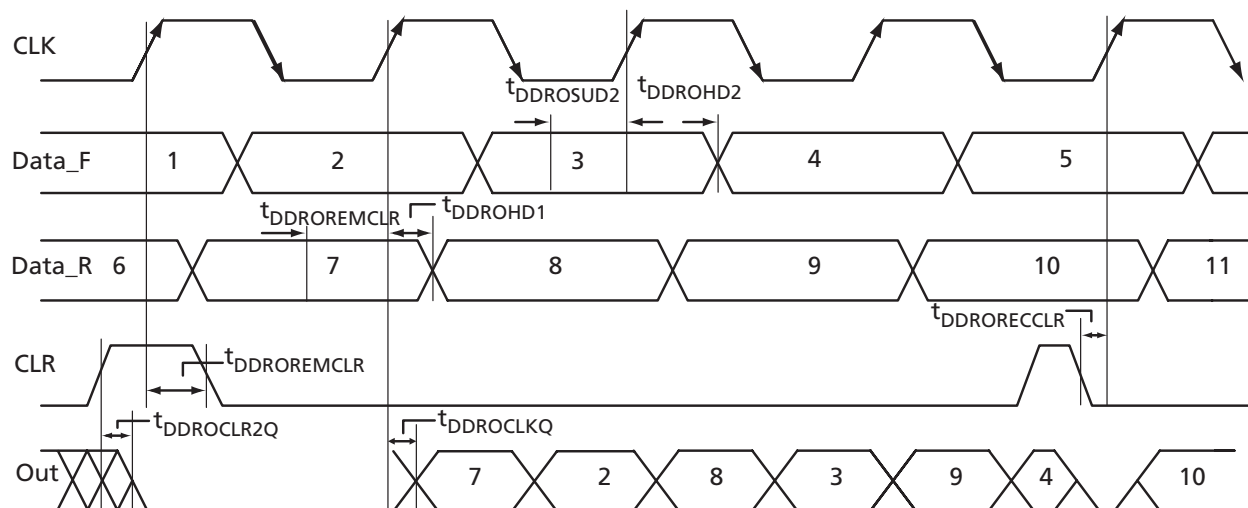


Figure 2-23 • Output DDR Timing Diagram

Timing Characteristics

Table 2-102 • Output DDR Propagation Delays
Commercial-Case Conditions: $T_J = 135^{\circ}\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$

Parameter	Description	–1	Std.	Units
t_{DDROCLKQ}	Clock-to-Out of DDR for Output DDR	0.85	1.00	ns
t_{DDROSUD1}	Data_F Data Setup for Output DDR	0.46	0.54	ns
t_{DDROSUD2}	Data_R Data Setup for Output DDR	0.46	0.54	ns
t_{DDROHD1}	Data_F Data Hold for Output DDR	0.00	0.00	ns
t_{DDROHD2}	Data_R Data Hold for Output DDR	0.00	0.00	ns
$t_{\text{DDROCLR2Q}}$	Asynchronous Clear-to-Out for Output DDR	0.97	1.15	ns
$t_{\text{DDROREMCLR}}$	Asynchronous Clear Removal Time for Output DDR	0.00	0.00	ns
$t_{\text{DDRORECCLR}}$	Asynchronous Clear Recovery Time for Output DDR	0.27	0.32	ns
$t_{\text{DDROWCLR1}}$	Asynchronous Clear Minimum Pulse Width for Output DDR	0.25	0.30	ns
$t_{\text{DDROCKMPWH}}$	Clock Minimum Pulse Width HIGH for the Output DDR	0.41	0.48	ns
$t_{\text{DDROCKMPWL}}$	Clock Minimum Pulse Width LOW for the Output DDR	0.37	0.43	ns
F_{DDOMAX}	Maximum Frequency for the Output DDR	TBD	TBD	MHz

Note: For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-5 for derating values.

Table 2-103 • Output DDR Propagation Delays
Commercial-Case Conditions: $T_J = 115^{\circ}\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$

Parameter	Description	–1	Std.	Units
t_{DDROCLKQ}	Clock-to-Out of DDR for Output DDR	0.84	0.98	ns
t_{DDROSUD1}	Data_F Data Setup for Output DDR	0.45	0.53	ns
t_{DDROSUD2}	Data_R Data Setup for Output DDR	0.45	0.53	ns
t_{DDROHD1}	Data_F Data Hold for Output DDR	0.00	0.00	ns
t_{DDROHD2}	Data_R Data Hold for Output DDR	0.00	0.00	ns
$t_{\text{DDROCLR2Q}}$	Asynchronous Clear-to-Out for Output DDR	0.96	1.12	ns
$t_{\text{DDROREMCLR}}$	Asynchronous Clear Removal Time for Output DDR	0.00	0.00	ns
$t_{\text{DDRORECCLR}}$	Asynchronous Clear Recovery Time for Output DDR	0.27	0.31	ns
$t_{\text{DDROWCLR1}}$	Asynchronous Clear Minimum Pulse Width for Output DDR	0.25	0.30	ns
$t_{\text{DDROCKMPWH}}$	Clock Minimum Pulse Width HIGH for the Output DDR	0.41	0.48	ns
$t_{\text{DDROCKMPWL}}$	Clock Minimum Pulse Width LOW for the Output DDR	0.37	0.43	ns
F_{DDOMAX}	Maximum Frequency for the Output DDR	TBD	TBD	MHz

Note: For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-5 for derating values.

VersaTile Characteristics

VersaTile Specifications as a Combinatorial Module

The ProASIC3 library offers all combinations of LUT-3 combinatorial functions. In this section, timing characteristics are presented for a sample of the library. For more details, refer to the *Fusion, IGLOOle, and ProASIC3/E Macro Library Guide*.

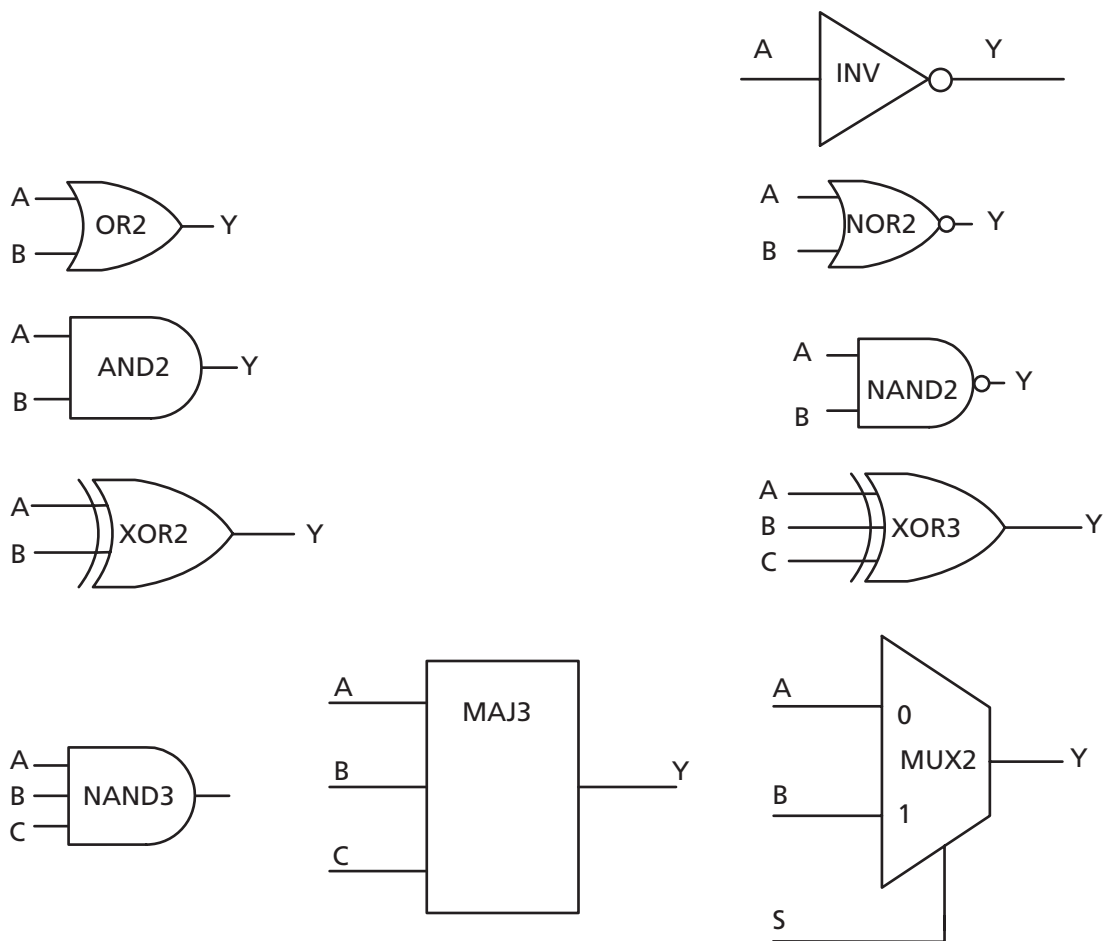


Figure 2-24 • Sample of Combinatorial Cells

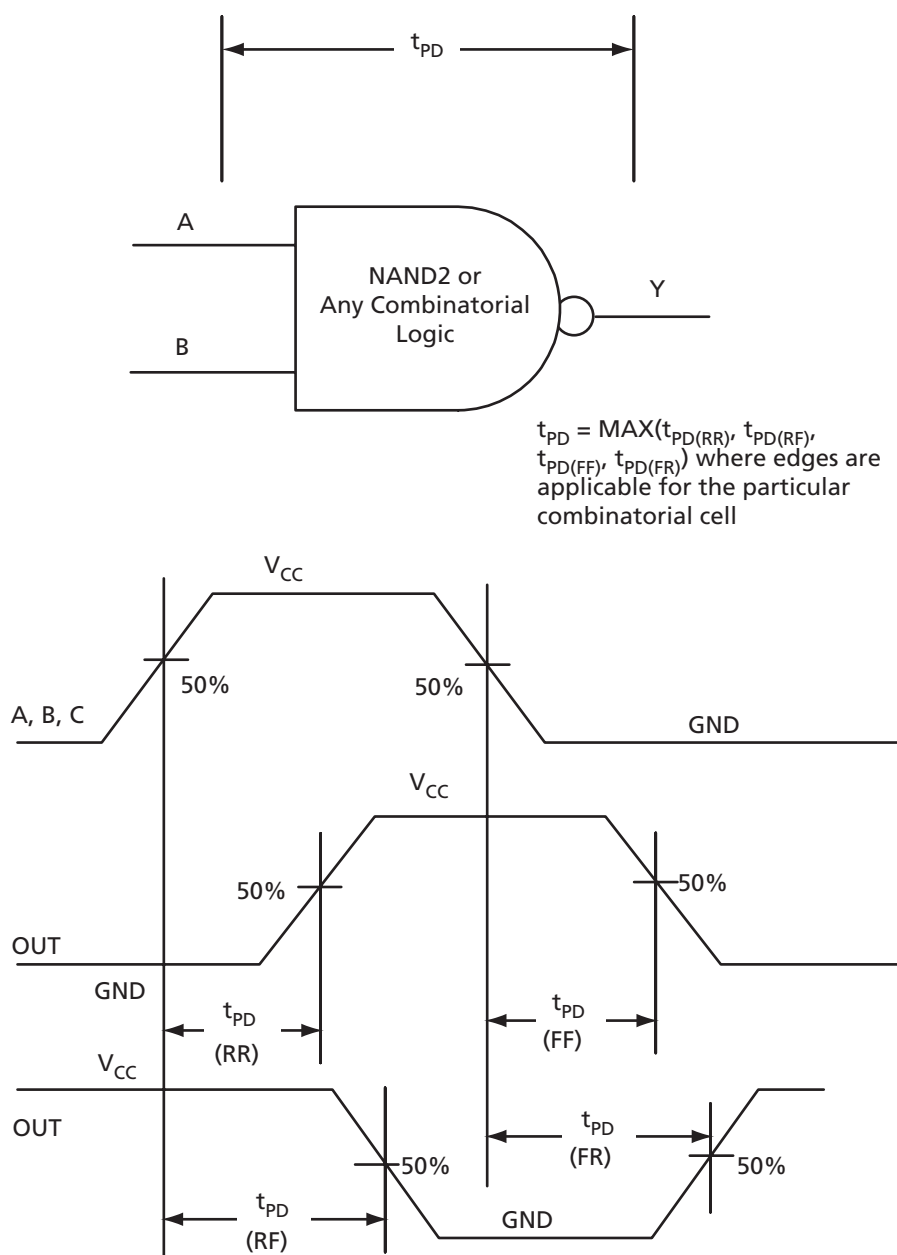


Figure 2-25 • Timing Model and Waveforms

Timing Characteristics

Table 2-104 • Combinatorial Cell Propagation Delays

Automotive-Case Conditions: $T_J = 135^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$

Combinatorial Cell	Equation	Parameter	-1	Std.	Units
INV	$Y = !A$	t_{PD}	0.49	0.57	ns
AND2	$Y = A \cdot B$	t_{PD}	0.57	0.67	ns
NAND2	$Y = !(A \cdot B)$	t_{PD}	0.57	0.67	ns
OR2	$Y = A + B$	t_{PD}	0.59	0.69	ns
NOR2	$Y = !(A + B)$	t_{PD}	0.59	0.69	ns
XOR2	$Y = A \oplus B$	t_{PD}	0.90	1.05	ns
MAJ3	$Y = \text{MAJ}(A, B, C)$	t_{PD}	0.85	1.00	ns
XOR3	$Y = A \oplus B \oplus C$	t_{PD}	1.06	1.25	ns
MUX2	$Y = A !S + B S$	t_{PD}	0.62	0.72	ns
AND3	$Y = A \cdot B \cdot C$	t_{PD}	0.68	0.80	ns

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-5 on page 2-5](#) for derating values.

Table 2-105 • Combinatorial Cell Propagation Delays

Automotive-Case Conditions: $T_J = 115^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$

Combinatorial Cell	Equation	Parameter	-1	Std.	Units
INV	$Y = !A$	t_{PD}	0.48	0.56	ns
AND2	$Y = A \cdot B$	t_{PD}	0.56	0.66	ns
NAND2	$Y = !(A \cdot B)$	t_{PD}	0.56	0.66	ns
OR2	$Y = A + B$	t_{PD}	0.58	0.68	ns
NOR2	$Y = !(A + B)$	t_{PD}	0.58	0.68	ns
XOR2	$Y = A \oplus B$	t_{PD}	0.88	1.03	ns
MAJ3	$Y = \text{MAJ}(A, B, C)$	t_{PD}	0.83	0.98	ns
XOR3	$Y = A \oplus B \oplus C$	t_{PD}	1.04	1.23	ns
MUX2	$Y = A !S + B S$	t_{PD}	0.60	0.71	ns
AND3	$Y = A \cdot B \cdot C$	t_{PD}	0.67	0.79	ns

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-5 on page 2-5](#) for derating values.

VersaTile Specifications as a Sequential Module

The ProASIC3 library offers a wide variety of sequential cells, including flip-flops and latches. Each has a data input and optional enable, clear, or preset. In this section, timing characteristics are presented for a representative sample from the library. For more details, refer to the [Fusion](#), [IGLOO/Ie](#) and [ProASIC3/Ie Macro Library Guide](#).

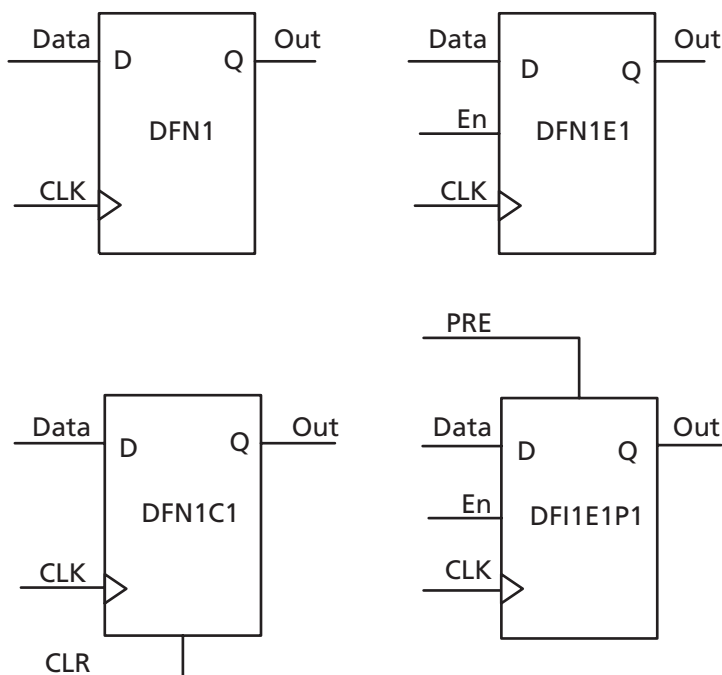


Figure 2-26 • Sample of Sequential Cells

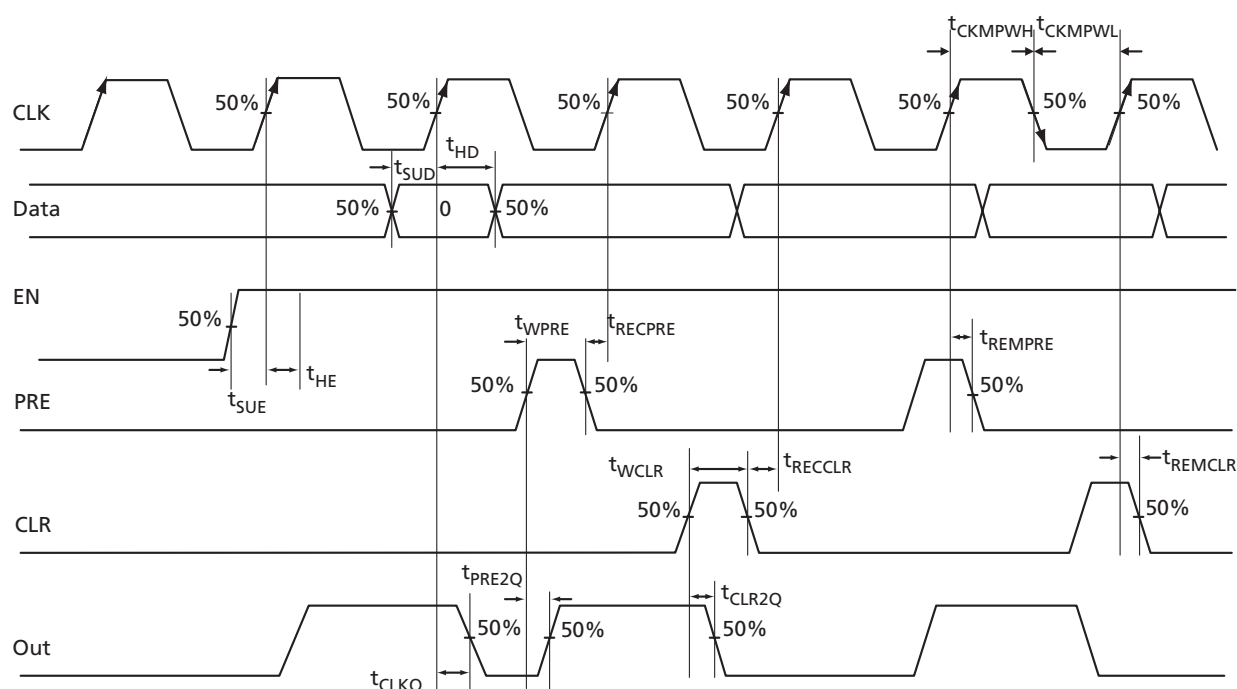


Figure 2-27 • Timing Model and Waveforms

Timing Characteristics

Table 2-106 • Register Delays

Automotive-Case Conditions: $T_J = 135^{\circ}\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$

Parameter	Description	-1	Std.	Units
t_{CLKQ}	Clock-to-Q of the Core Register	0.67	0.79	ns
t_{SUD}	Data Setup Time for the Core Register	0.52	0.61	ns
t_{HD}	Data Hold Time for the Core Register	0.00	0.00	ns
t_{SUE}	Enable Setup Time for the Core Register	0.55	0.65	ns
t_{HE}	Enable Hold Time for the Core Register	0.00	0.00	ns
t_{CLR2Q}	Asynchronous Clear-to-Q of the Core Register	0.49	0.57	ns
t_{PRE2Q}	Asynchronous Preset-to-Q of the Core Register	0.49	0.57	ns
t_{REMCLR}	Asynchronous Clear Removal Time for the Core Register	0.00	0.00	ns
t_{RECCLR}	Asynchronous Clear Recovery Time for the Core Register	0.27	0.32	ns
t_{REMPRE}	Asynchronous Preset Removal Time for the Core Register	0.00	0.00	ns
t_{RECPRE}	Asynchronous Preset Recovery Time for the Core Register	0.27	0.32	ns
t_{WCLR}	Asynchronous Clear Minimum Pulse Width for the Core Register	0.25	0.30	ns
t_{WPRE}	Asynchronous Preset Minimum Pulse Width for the Core Register	0.25	0.30	ns
t_{CKMPWH}	Clock Minimum Pulse Width HIGH for the Core Register	0.41	0.48	ns
t_{CKMPWL}	Clock Minimum Pulse Width LOW for the Core Register	0.37	0.43	ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-5 for derating values.

Table 2-107 • Register Delays

Automotive-Case Conditions: $T_J = 115^{\circ}\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$

Parameter	Description	–1	Std.	Units
t_{CLKQ}	Clock-to-Q of the Core Register	0.66	0.77	ns
t_{SUD}	Data Setup Time for the Core Register	0.51	0.60	ns
t_{HD}	Data Hold Time for the Core Register	0.00	0.00	ns
t_{SUE}	Enable Setup Time for the Core Register	0.54	0.64	ns
t_{HE}	Enable Hold Time for the Core Register	0.00	0.00	ns
t_{CLR2Q}	Asynchronous Clear-to-Q of the Core Register	0.48	0.56	ns
t_{PRE2Q}	Asynchronous Preset-to-Q of the Core Register	0.48	0.56	ns
t_{REMCLR}	Asynchronous Clear Removal Time for the Core Register	0.00	0.00	ns
t_{RECCLR}	Asynchronous Clear Recovery Time for the Core Register	0.27	0.31	ns
t_{REMPRE}	Asynchronous Preset Removal Time for the Core Register	0.00	0.00	ns
t_{RECPRE}	Asynchronous Preset Recovery Time for the Core Register	0.27	0.31	ns
t_{WCLR}	Asynchronous Clear Minimum Pulse Width for the Core Register	0.25	0.30	ns
t_{WPRE}	Asynchronous Preset Minimum Pulse Width for the Core Register	0.25	0.30	ns
t_{CKMPWH}	Clock Minimum Pulse Width HIGH for the Core Register	0.41	0.48	ns
t_{CKMPWL}	Clock Minimum Pulse Width LOW for the Core Register	0.37	0.43	ns

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-5 on page 2-5](#) for derating values.

Global Resource Characteristics

A3P250 Clock Tree Topology

Clock delays are device-specific. Figure 2-28 is an example of a global tree used for clock routing. The global tree presented in Figure 2-28 is driven by a CCC located on the west side of the A3P250 device. It is used to drive all D-flip-flops in the device.

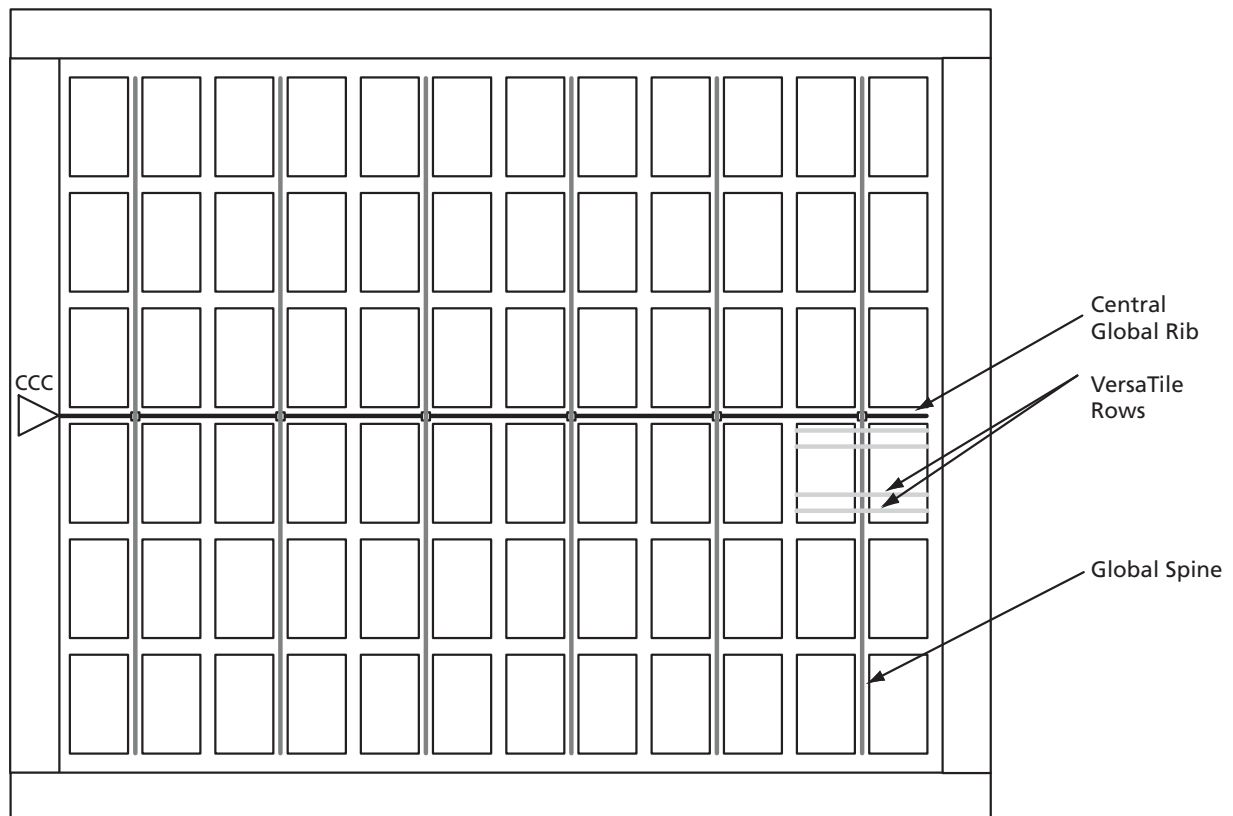


Figure 2-28 • Example of Global Tree Use in an A3P250 Device for Clock Routing

Global Tree Timing Characteristics

Global clock delays include the central rib delay, the spine delay, and the row delay. Delays do not include I/O input buffer clock delays, as these are I/O standard-dependent, and the clock may be driven and conditioned internally by the CCC module. For more details on clock conditioning capabilities, refer to the "Clock Conditioning Circuits" section on page 2-77. Table 2-114 on page 2-76 to Table 2-125 on page 2-95 present minimum and maximum global clock delays within each device. Minimum and maximum delays are measured with minimum and maximum loading.

Timing Characteristics

Table 2-108 • A3P060 Global Resource

Commercial-Case Conditions: $T_J = 135^{\circ}\text{C}$, $V_{CC} = 1.425\text{ V}$

Parameter	Description	–1		Std.		Units
		Min. ¹	Max. ²	Min. ¹	Max. ²	
t_{RCKL}	Input LOW Delay for Global Clock	0.87	1.16	1.02	1.37	ns
t_{RCKH}	Input HIGH Delay for Global Clock	0.86	1.20	1.01	1.42	ns
t_{RCKMPWH}	Minimum Pulse Width HIGH for Global Clock					ns
t_{RCKMPWL}	Minimum Pulse Width LOW for Global Clock					ns
t_{RCKSW}	Maximum Skew for Global Clock		0.35		0.41	ns
F_{RMAX}	Maximum Frequency for Global Clock					MHz

Notes:

1. Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).
2. Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).
3. For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-5 for derating values.

Table 2-109 • A3P060 Global Resource

Commercial-Case Conditions: $T_J = 115^{\circ}\text{C}$, $V_{CC} = 1.425\text{ V}$

Parameter	Description	–1		Std.		Units
		Min. ¹	Max. ²	Min. ¹	Max. ²	
t_{RCKL}	Input LOW Delay for Global Clock	0.85	1.13	1.00	1.33	ns
t_{RCKH}	Input HIGH Delay for Global Clock	0.84	1.18	0.99	1.38	ns
t_{RCKMPWH}	Minimum Pulse Width HIGH for Global Clock					ns
t_{RCKMPWL}	Minimum Pulse Width LOW for Global Clock					ns
t_{RCKSW}	Maximum Skew for Global Clock		0.34		0.40	ns
F_{RMAX}	Maximum Frequency for Global Clock					MHz

Notes:

1. Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).
2. Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).
3. For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-5 for derating values.

Table 2-110 • A3P125 Global Resource

Commercial-Case Conditions: $T_J = 135^{\circ}\text{C}$, $V_{CC} = 1.425\text{ V}$

Parameter	Description	–1		Std.		Units
		Min. ¹	Max. ²	Min. ¹	Max. ²	
t_{RCKL}	Input LOW Delay for Global Clock	0.93	1.22	1.09	1.43	ns
t_{RCKH}	Input HIGH Delay for Global Clock	0.92	1.26	1.08	1.49	ns
t_{RCKMPWH}	Minimum Pulse Width HIGH for Global Clock					ns
t_{RCKMPWL}	Minimum Pulse Width LOW for Global Clock					ns
t_{RCKSW}	Maximum Skew for Global Clock		0.35		0.41	ns
F_{RMAX}	Maximum Frequency for Global Clock					MHz

Notes:

1. Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).
2. Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).
3. For specific junction temperature and voltage supply levels, refer to [Table 2-5 on page 2-5](#) for derating values.

Table 2-111 • A3P125 Global Resource

Commercial-Case Conditions: $T_J = 115^{\circ}\text{C}$, $V_{CC} = 1.425\text{ V}$

Parameter	Description	–1		Std.		Units
		Min. ¹	Max. ²	Min. ¹	Max. ²	
t_{RCKL}	Input LOW Delay for Global Clock	0.90	1.19	1.06	1.40	ns
t_{RCKH}	Input HIGH Delay for Global Clock	0.90	1.23	1.05	1.45	ns
t_{RCKMPWH}	Minimum Pulse Width HIGH for Global Clock					ns
t_{RCKMPWL}	Minimum Pulse Width LOW for Global Clock					ns
t_{RCKSW}	Maximum Skew for Global Clock		0.34		0.40	ns
F_{RMAX}	Maximum Frequency for Global Clock					MHz

Notes:

1. Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).
2. Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).
3. For specific junction temperature and voltage supply levels, refer to [Table 2-5 on page 2-5](#) for derating values.

Table 2-112 • A3P250 Global Resource

Commercial-Case Conditions: $T_J = 135^{\circ}\text{C}$, $V_{CC} = 1.425\text{ V}$

Parameter	Description	–1		Std.		Units
		Min. ¹	Max. ²	Min. ¹	Max. ²	
t_{RCKL}	Input LOW Delay for Global Clock	0.96	1.25	1.13	1.47	ns
t_{RCKH}	Input HIGH Delay for Global Clock	0.94	1.28	1.10	1.51	ns
t_{RCKMPWH}	Minimum Pulse Width HIGH for Global Clock					ns
t_{RCKMPWL}	Minimum Pulse Width LOW for Global Clock					ns
t_{RCKSW}	Maximum Skew for Global Clock		0.35		0.41	ns
F_{RMAX}	Maximum Frequency for Global Clock					MHz

Notes:

1. Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).
2. Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).
3. For specific junction temperature and voltage supply levels, refer to [Table 2-5 on page 2-5](#) for derating values.

Table 2-113 • A3P250 Global Resource

Commercial-Case Conditions: $T_J = 115^{\circ}\text{C}$, $V_{CC} = 1.425\text{ V}$

Parameter	Description	–1		Std.		Units
		Min. ¹	Max. ²	Min. ¹	Max. ²	
t_{RCKL}	Input LOW Delay for Global Clock	0.94	1.22	1.10	1.44	ns
t_{RCKH}	Input HIGH Delay for Global Clock	0.92	1.25	1.08	1.47	ns
t_{RCKMPWH}	Minimum Pulse Width HIGH for Global Clock					ns
t_{RCKMPWL}	Minimum Pulse Width LOW for Global Clock					ns
t_{RCKSW}	Maximum Skew for Global Clock		0.34		0.40	ns
F_{RMAX}	Maximum Frequency for Global Clock					MHz

Notes:

1. Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).
2. Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).
3. For specific junction temperature and voltage supply levels, refer to [Table 2-5 on page 2-5](#) for derating values.

Table 2-114 • A3P1000 Global Resource
Automotive-Case Conditions: $T_J = 135^{\circ}\text{C}$, $V_{CC} = 1.425\text{ V}$

Parameter	Description	–1		Std.		Units
		Min. ¹	Max. ²	Min. ¹	Max. ²	
t_{RCKL}	Input LOW Delay for Global Clock	1.17	1.46	1.37	1.72	ns
t_{RCKH}	Input HIGH Delay for Global Clock	1.15	1.50	1.36	1.76	ns
t_{RCKMPWH}	Minimum Pulse Width HIGH for Global Clock					ns
t_{RCKMPWL}	Minimum Pulse Width LOW for Global Clock					ns
t_{RCKSW}	Maximum Skew for Global Clock		0.35		0.41	ns
F_{RMAX}	Maximum Frequency for Global Clock					MHz

Notes:

1. Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).
2. Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).
3. For specific junction temperature and voltage supply levels, refer to [Table 2-5 on page 2-5](#) for derating values.

Table 2-115 • A3P1000 Global Resource
Automotive-Case Conditions: $T_J = 115^{\circ}\text{C}$, $V_{CC} = 1.425\text{ V}$

Parameter	Description	–1		Std.		Units
		Min. ¹	Max. ²	Min. ¹	Max. ²	
t_{RCKL}	Input LOW Delay for Global Clock	1.14	1.43	1.34	1.68	ns
t_{RCKH}	Input HIGH Delay for Global Clock	1.13	1.46	1.32	1.72	ns
t_{RCKMPWH}	Minimum Pulse Width HIGH for Global Clock					ns
t_{RCKMPWL}	Minimum Pulse Width LOW for Global Clock					ns
t_{RCKSW}	Maximum Skew for Global Clock		0.34		0.40	ns
F_{RMAX}	Maximum Frequency for Global Clock					MHz

Notes:

1. Value reflects minimum load. The delay is measured from the CCC output to the clock pin of a sequential element, located in a lightly loaded row (single element is connected to the global net).
2. Value reflects maximum load. The delay is measured on the clock pin of the farthest sequential element, located in a fully loaded row (all available flip-flops are connected to the global net in the row).
3. For specific junction temperature and voltage supply levels, refer to [Table 2-5 on page 2-5](#) for derating values.

Clock Conditioning Circuits

CCC Electrical Specifications

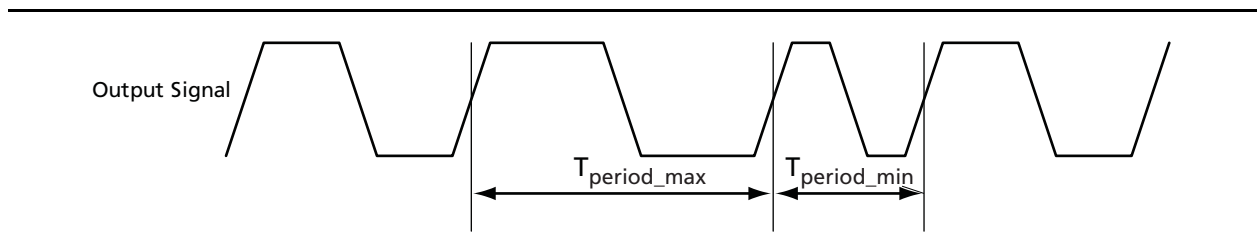
Timing Characteristics

Table 2-116 • Automotive ProASIC3 CCC/PLL Specification

Parameter	Minimum	Typical	Maximum	Units
Clock Conditioning Circuitry Input Frequency f_{IN_CCC}	1.5		350	MHz
Clock Conditioning Circuitry Output Frequency f_{OUT_CCC}	0.75		350	MHz
Delay Increments in Programmable Delay Blocks ^{1, 2}		160		ps
Number of Programmable Values in Each Programmable Delay Block			32	
Input Period Jitter			1.5	ns
CCC Output Peak-to-Peak Period Jitter F_{CCC_OUT}	Max Peak-to-Peak Period Jitter			
	1 Global Network Used		3 Global Networks Used	
0.75 MHz to 24 MHz	0.50%		0.70%	
24 MHz to 100 MHz	1.00%		1.20%	
100 MHz to 250 MHz	1.75%		2.00%	
250 MHz to 350 MHz	2.50%		5.60%	
Acquisition Time				
(A3P250 and A3P1000 only) LockControl = 0			300	μs
LockControl = 1			300	μs
(all other dies) LockControl = 0			300	μs
LockControl = 1			6.0	ms
Tracking Jitter ⁴				
(A3P250 and A3P1000 only) LockControl = 0			1.6	ns
LockControl = 1			1.6	ns
(all other dies) LockControl = 0			1.6	ns
LockControl = 1			0.8	ns
Output Duty Cycle	48.5		51.5	%
Delay Range in Block: Programmable Delay 1 ^{1, 2}	0.6		5.56	ns
Delay Range in Block: Programmable Delay 2 ^{1, 2}	0.025		5.56	ns
Delay Range in Block: Fixed Delay ^{1, 2}		2.2		ns

Notes:

1. This delay is a function of voltage and temperature. See [Table 2-5 on page 2-5](#) for deratings.
2. $T_J = 25^\circ\text{C}$, $V_{CC} = 1.5\text{ V}$
3. Tracking jitter is defined as the variation in clock edge position of PLL outputs with reference to the PLL input clock edge. Tracking jitter does not measure the variation in PLL output period, which is covered by the period jitter parameter.



Note: Peak-to-peak jitter measurements are defined by $T_{\text{peak-to-peak}} = T_{\text{period_max}} - T_{\text{period_min}}$.

Figure 2-29 • Peak-to-Peak Jitter Definition

Embedded SRAM and FIFO Characteristics

SRAM

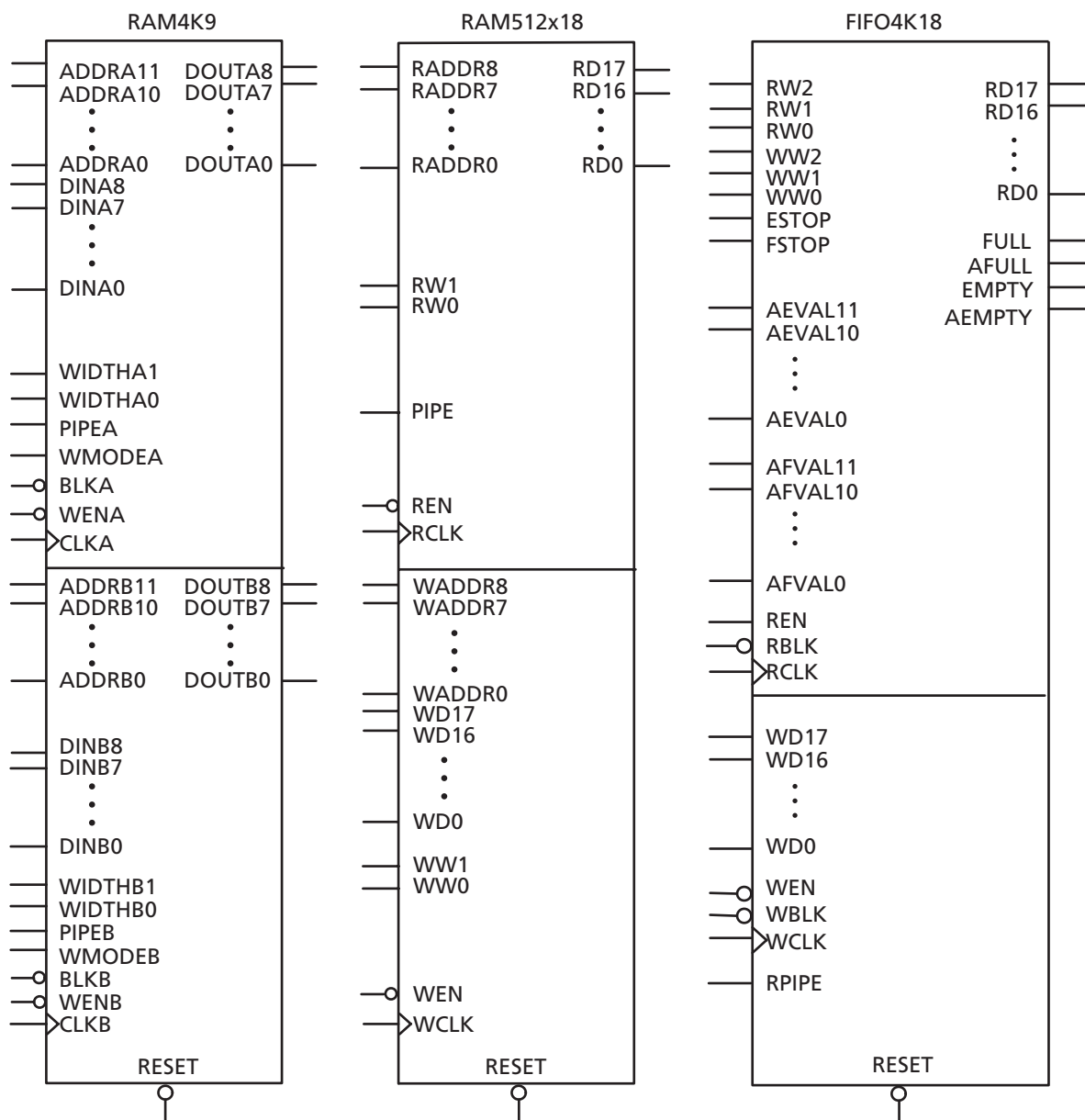


Figure 2-30 • RAM Models

Timing Waveforms

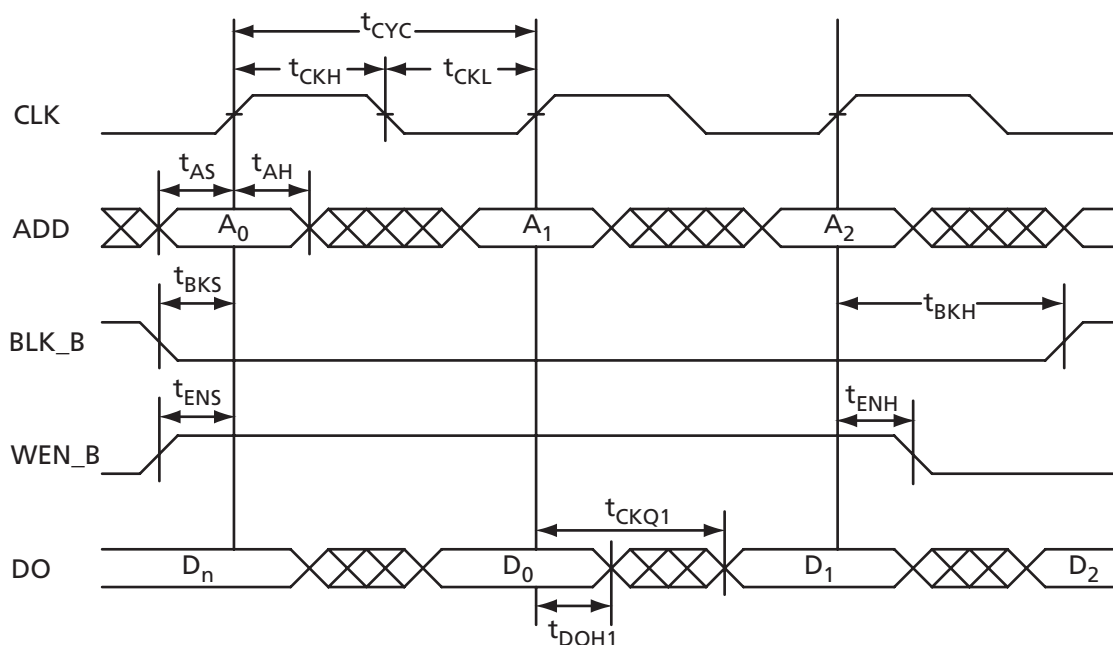


Figure 2-31 • RAM Read for Pass-Through Output

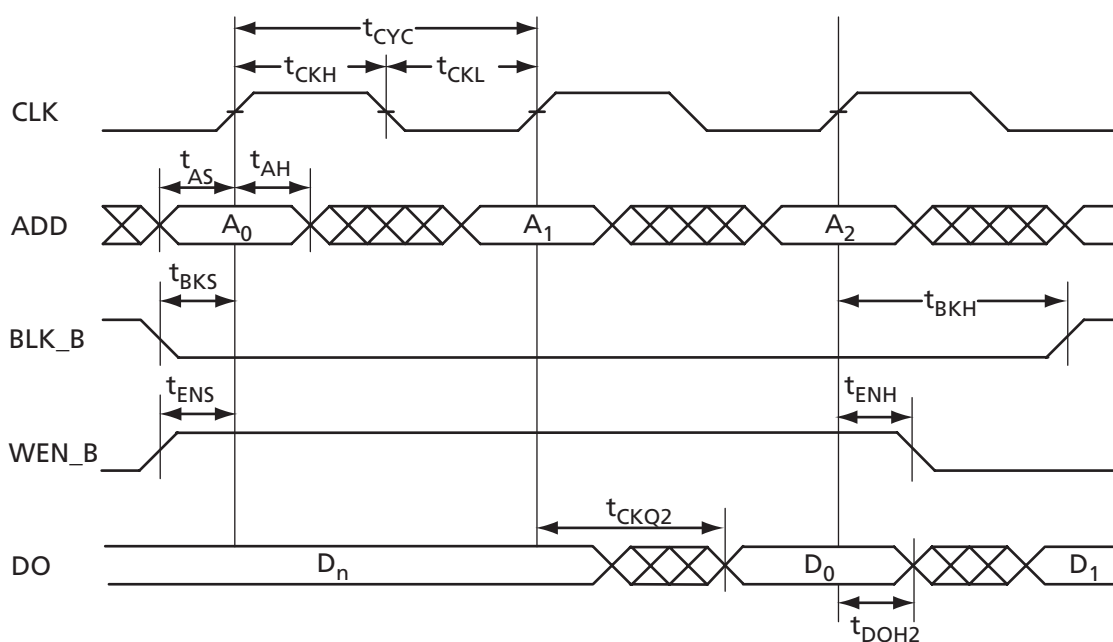


Figure 2-32 • RAM Read for Pipelined Output

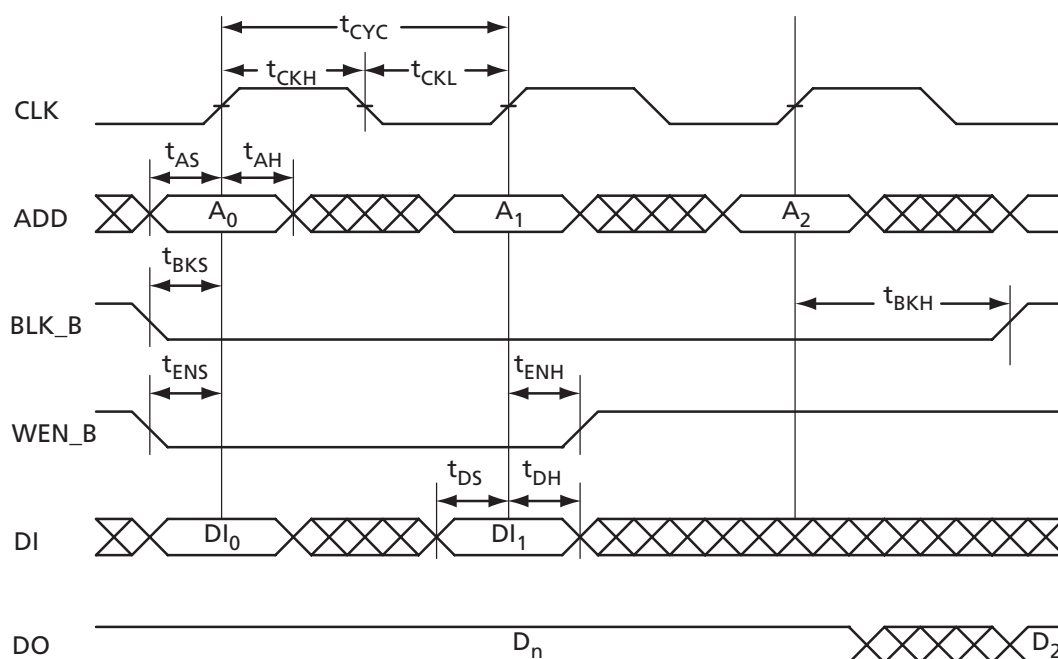


Figure 2-33 • RAM Write, Output Retained (WMODE = 0)

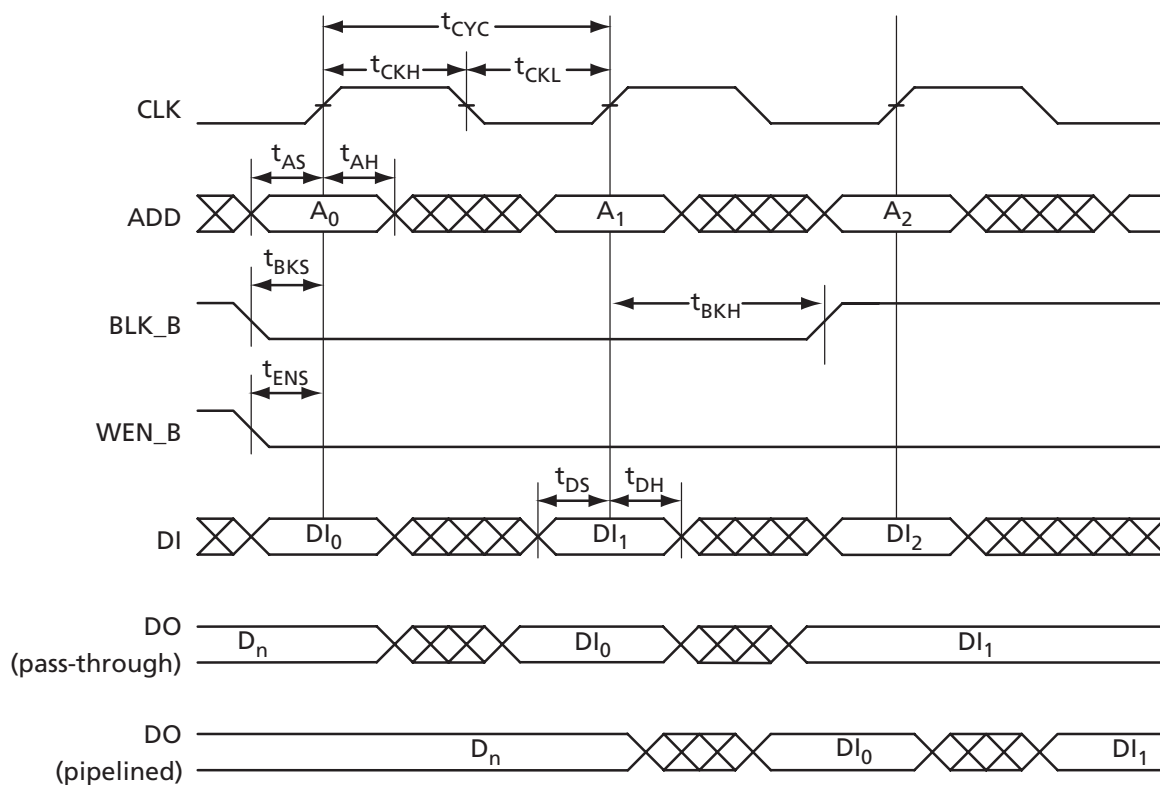


Figure 2-34 • RAM Write, Output as Write Data (WMODE = 1)

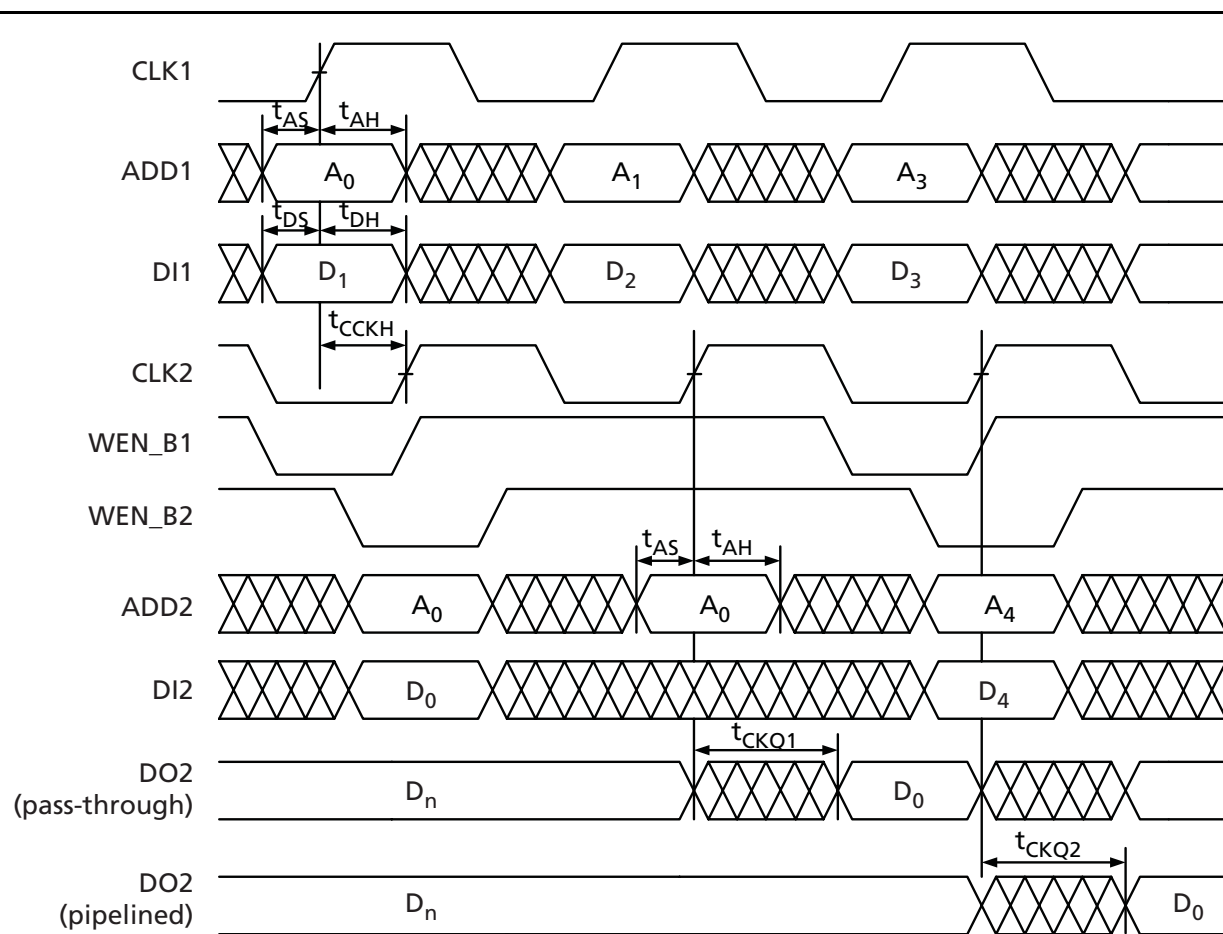


Figure 2-35 • Write Access after Write to Same Address

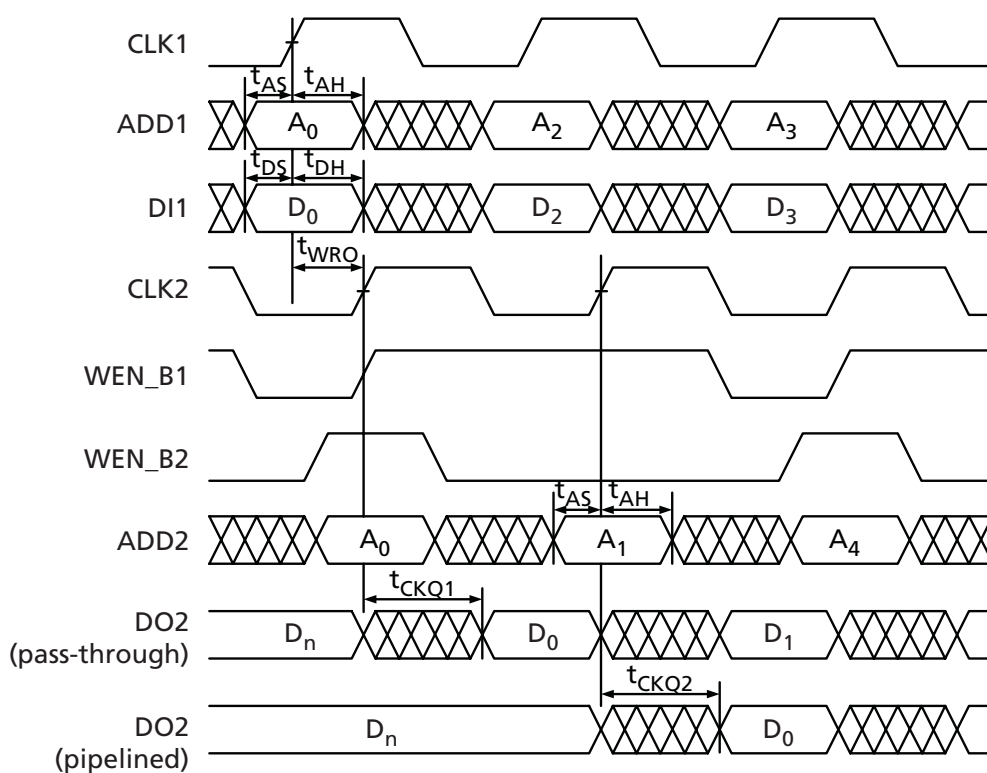


Figure 2-36 • Read Access after Write to Same Address

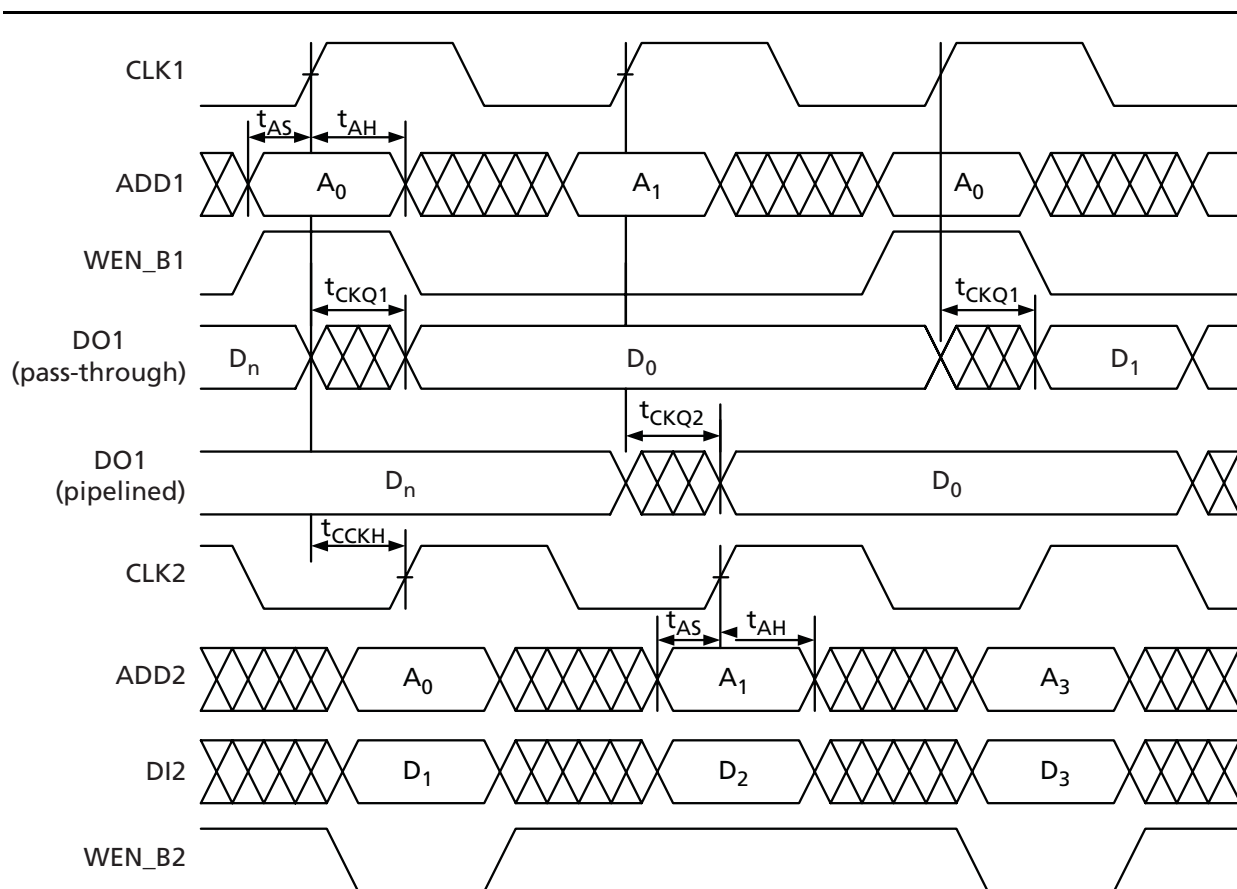


Figure 2-37 • Write Access after Read to Same Address

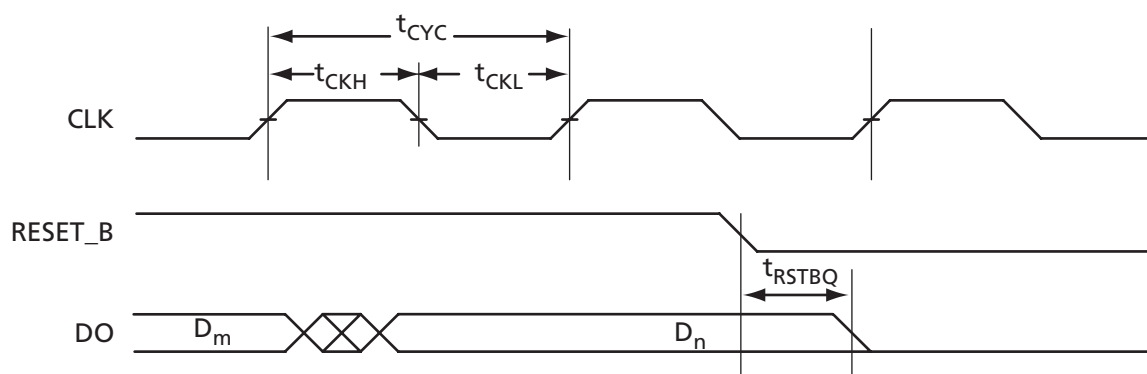


Figure 2-38 • RAM Reset

Timing Characteristics

Table 2-117 • RAM4K9

Automotive-Case Conditions: $T_J = 135^{\circ}\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$

Parameter	Description	-1	Std.	Units
t_{AS}	Address Setup Time	0.30	0.36	ns
t_{AH}	Address Hold Time	0.00	0.00	ns
t_{ENS}	REN_B, WEN_B Setup Time	0.17	0.20	ns
t_{ENH}	REN_B, WEN_B Hold Time	0.12	0.14	ns
t_{BKS}	BLK_B Setup Time	0.28	0.33	ns
t_{BKH}	BLK_B Hold Time	0.02	0.03	ns
t_{DS}	Input Data (DI) Setup Time	0.22	0.26	ns
t_{DH}	Input Data (DI) Hold Time	0.00	0.00	ns
t_{CKQ1}	Clock HIGH to New Data Valid on DO (output retained, WMODE = 0)	2.17	2.55	ns
	Clock HIGH to New Data Valid on DO (flow-through, WMODE = 1)	2.86	3.37	ns
t_{CKQ2}	Clock HIGH to New Data Valid on DO (pipelined)	1.09	1.28	ns
t_{WRO}	Address collision clk-to-clk delay for reliable read access after write on same address	TBD	TBD	ns
t_{CKH}	Address collision clk-to-clk delay for reliable write access after write/read on same address	TBD	TBD	ns
t_{RSTBQ}	RESET_B LOW to Data Out LOW on DO (flow-through)	1.12	1.32	ns
	RESET_B LOW to Data Out LOW on DO (pipelined)	1.12	1.32	ns
$t_{REMRSTB}$	RESET_B Removal	0.35	0.41	ns
$t_{RECRSTB}$	RESET_B Recovery	1.82	2.14	ns
$t_{MPWRSTB}$	RESET_B Minimum Pulse Width	0.26	0.30	ns
t_{CYC}	Clock Cycle Time	3.93	4.62	ns
F_{MAX}	Maximum Frequency	255	217	MHz

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-5 on page 2-5](#) for derating values.

Table 2-118 • RAM512X18

Automotive-Case Conditions: $T_J = 135^{\circ}\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$

Parameter	Description	–1	Std.	Units
t_{AS}	Address Setup Time	0.30	0.35	ns
t_{AH}	Address Hold Time	0.00	0.00	ns
t_{ENS}	REN_B, WEN_B Setup Time	0.11	0.13	ns
t_{ENH}	REN_B, WEN_B Hold Time	0.07	0.08	ns
t_{DS}	Input data (DI) Setup Time	0.22	0.26	ns
t_{DH}	Input data (DI) Hold Time	0.00	0.00	ns
t_{CKQ1}	Clock HIGH to New Data Valid on DO (output retained, WMODE = 0)	2.58	3.03	ns
t_{CKQ2}	Clock HIGH to New Data Valid on DO (pipelined)	1.07	1.26	ns
t_{WRO}	Address collision clk-to-clk delay for reliable read access after write on same address	TBD	TBD	ns
t_{CCKH}	Address collision clk-to-clk delay for reliable write access after write/read on same address	TBD	TBD	ns
t_{RSTBQ}	RESET_B LOW to Data Out LOW on DO (flow-through)	1.10	1.29	ns
	RESET_B LOW to Data Out LOW on DO (pipelined)	1.10	1.29	ns
$t_{REMRSTB}$	RESET_B Removal	0.34	0.40	ns
$t_{RECRSTB}$	RESET_B Recovery	1.79	2.10	ns
$t_{MPWRSTB}$	RESET_B Minimum Pulse Width	0.25	0.30	ns
t_{CYC}	Clock Cycle Time	3.85	4.53	ns
F_{MAX}	Maximum Frequency	260	221	MHz

Note: For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-5 for derating values.

Table 2-119 • RAM4K9

Automotive-Case Conditions: $T_J = 115^{\circ}\text{C}$, Worst Case $V_{CC} = 1.425\text{ V}$

Parameter	Description	–1	Std.	Units
t_{AS}	Address Setup Time	0.30	0.35	ns
t_{AH}	Address Hold Time	0.00	0.00	ns
t_{ENS}	REN_B, WEN_B Setup Time	0.17	0.20	ns
t_{ENH}	REN_B, WEN_B Hold Time	0.12	0.14	ns
t_{BKS}	BLK_B Setup Time	0.28	0.33	ns
t_{BKH}	BLK_B Hold Time	0.02	0.03	ns
t_{DS}	Input data (DI) Setup Time	0.22	0.26	ns
t_{DH}	Input data (DI) Hold Time	0.00	0.00	ns
t_{CKQ1}	Clock HIGH to New Data Valid on DO (output retained, WMODE = 0)	2.13	2.50	ns
	Clock HIGH to New Data Valid on DO (flow-through, WMODE = 1)	2.81	3.30	ns
t_{CKQ2}	Clock HIGH to New Data Valid on DO (pipelined)	1.07	1.25	ns
t_{WRO}	Address collision clk-to-clk delay for reliable read access after write on same address	TBD	TBD	ns
t_{CCKH}	Address collision clk-to-clk delay for reliable write access after write/read on same address	TBD	TBD	ns
t_{RSTBQ}	RESET_B LOW to Data Out LOW on DO (flow-through)	1.10	1.29	ns
	RESET_B LOW to Data Out LOW on DO (pipelined)	1.10	1.29	ns
$t_{REMRSTB}$	RESET_B Removal	0.34	0.40	ns
$t_{RECRSTB}$	RESET_B Recovery	1.79	2.10	ns
$t_{MPWRSTB}$	RESET_B Minimum Pulse Width	0.25	0.30	ns
t_{CYC}	Clock Cycle Time	3.85	4.53	ns
F_{MAX}	Maximum Frequency	260	221	MHz

Note: For specific junction temperature and voltage-supply levels, refer to [Table 2-5 on page 2-5](#) for derating values.

Table 2-120 • RAM512X18

Automotive-Case Conditions: $T_J = 115^{\circ}\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$

Parameter	Description	–1	Std.	Units
t_{AS}	Address Setup Time	0.30	0.35	ns
t_{AH}	Address Hold Time	0.00	0.00	ns
t_{ENS}	REN_B, WEN_B Setup Time	0.11	0.13	ns
t_{ENH}	REN_B, WEN_B Hold Time	0.07	0.08	ns
t_{DS}	Input data (DI) Setup Time	0.22	0.26	ns
t_{DH}	Input data (DI) Hold Time	0.00	0.00	ns
t_{CKQ1}	Clock HIGH to New Data Valid on DO (output retained, WMODE = 0)	2.58	3.03	ns
t_{CKQ2}	Clock HIGH to New Data Valid on DO (pipelined)	1.07	1.26	ns
t_{WRO}	Address collision clk-to-clk delay for reliable read access after write on same address	TBD	TBD	ns
t_{CCKH}	Address collision clk-to-clk delay for reliable write access after write/read on same address	TBD	TBD	ns
t_{RSTBQ}	RESET_B LOW to Data Out LOW on DO (flow-through)	1.10	1.29	ns
	RESET_B LOW to Data Out LOW on DO (pipelined)	1.10	1.29	ns
$t_{REMRSTB}$	RESET_B Removal	0.34	0.40	ns
$t_{RECRSTB}$	RESET_B Recovery	1.79	2.10	ns
$t_{MPWRSTB}$	RESET_B Minimum Pulse Width	0.25	0.30	ns
t_{CYC}	Clock Cycle Time	3.85	4.53	ns
F_{MAX}	Maximum Frequency	260	221	MHz

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-5 on page 2-5](#) for derating values.

FIFO

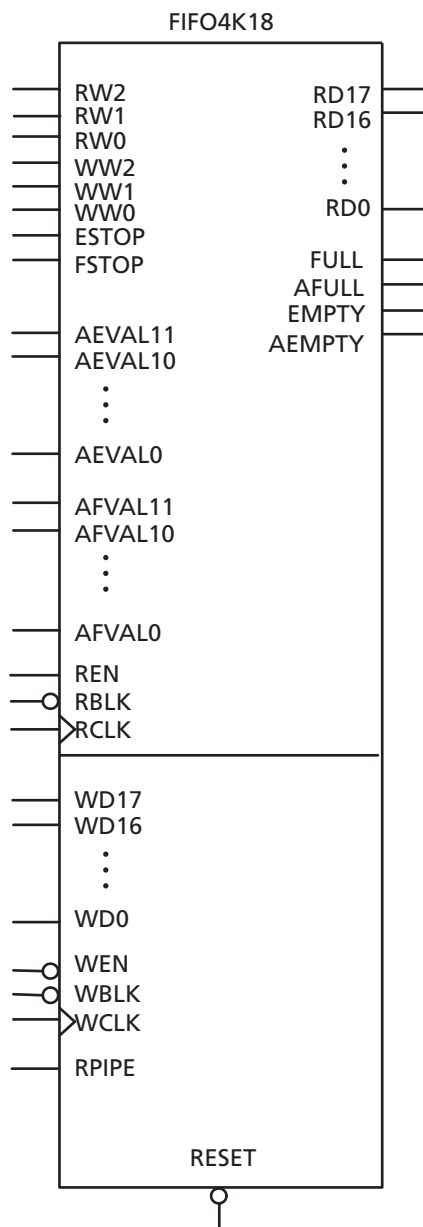


Figure 2-39 • FIFO Model

Timing Waveforms

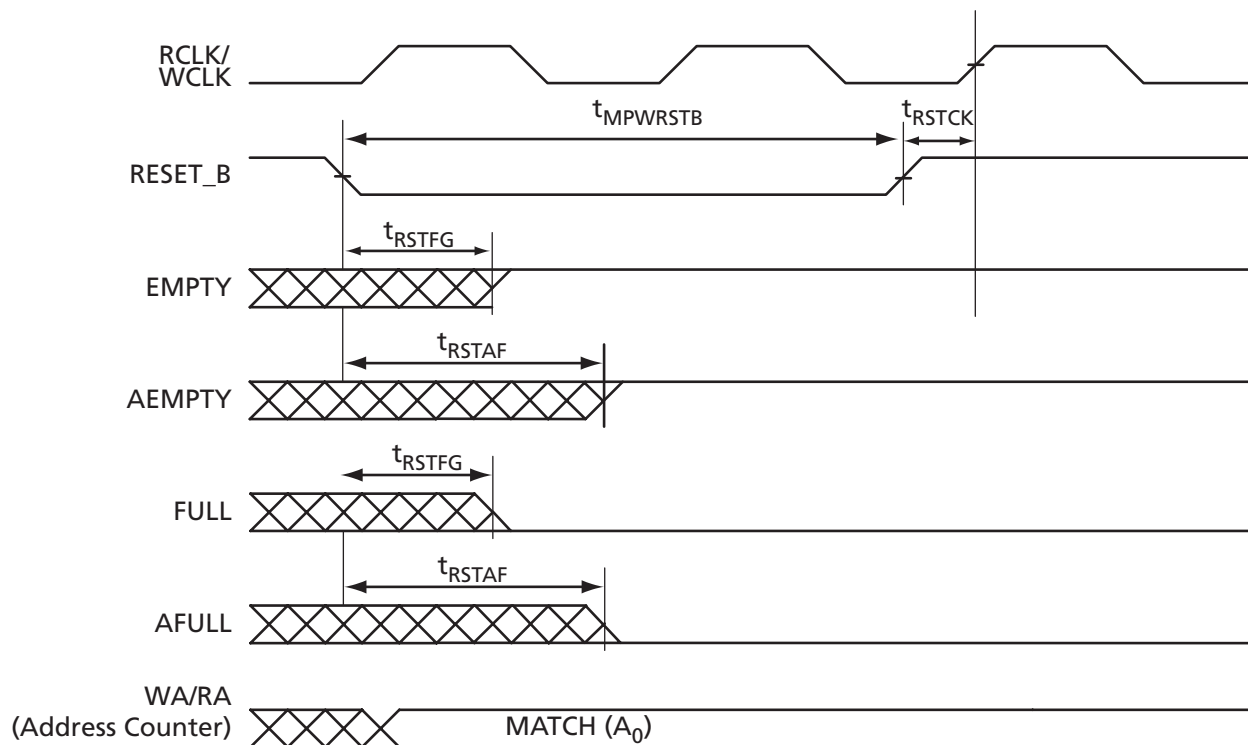


Figure 2-40 • FIFO Reset

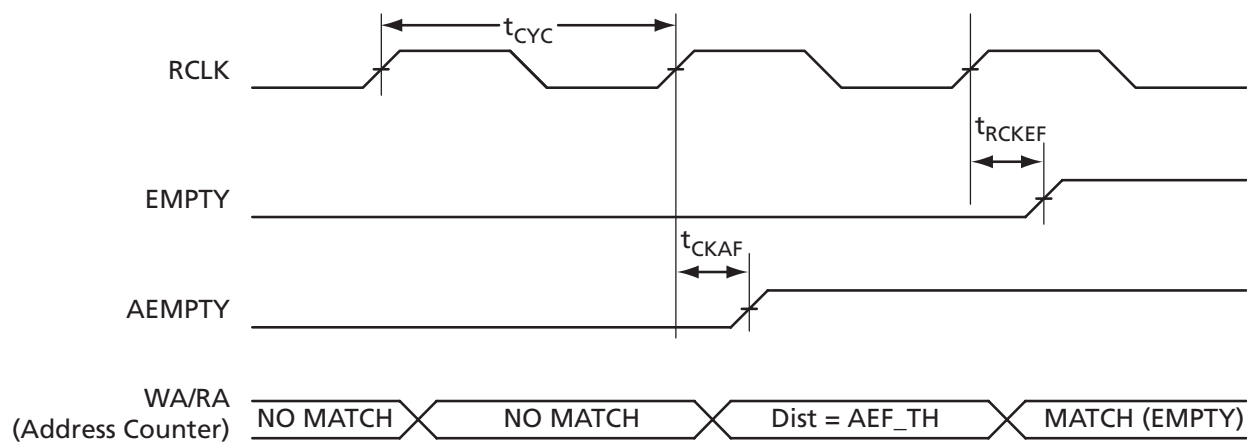


Figure 2-41 • FIFO EMPTY Flag and AEMPTY Flag Assertion

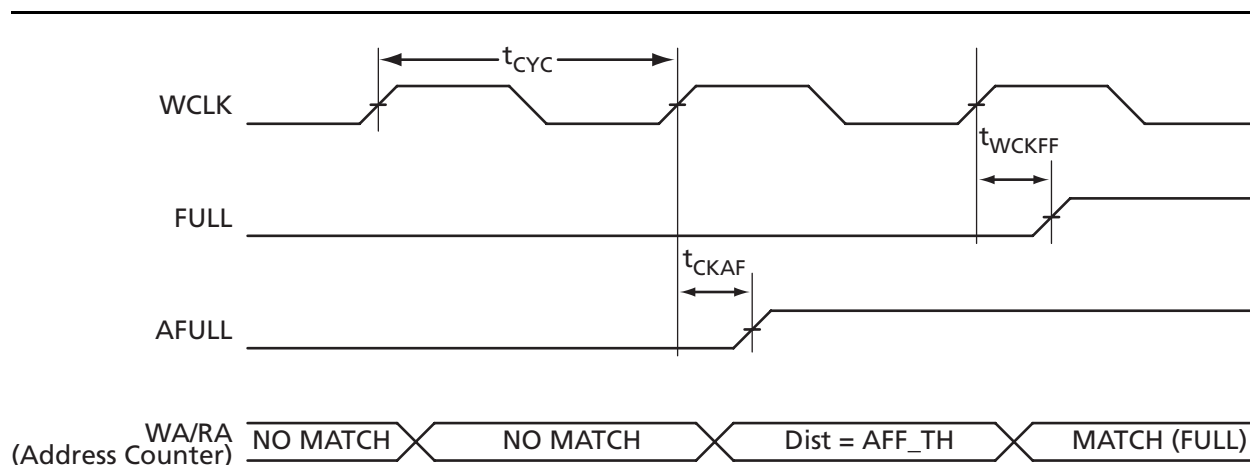


Figure 2-42 • FIFO FULL Flag and AFULL Flag Assertion

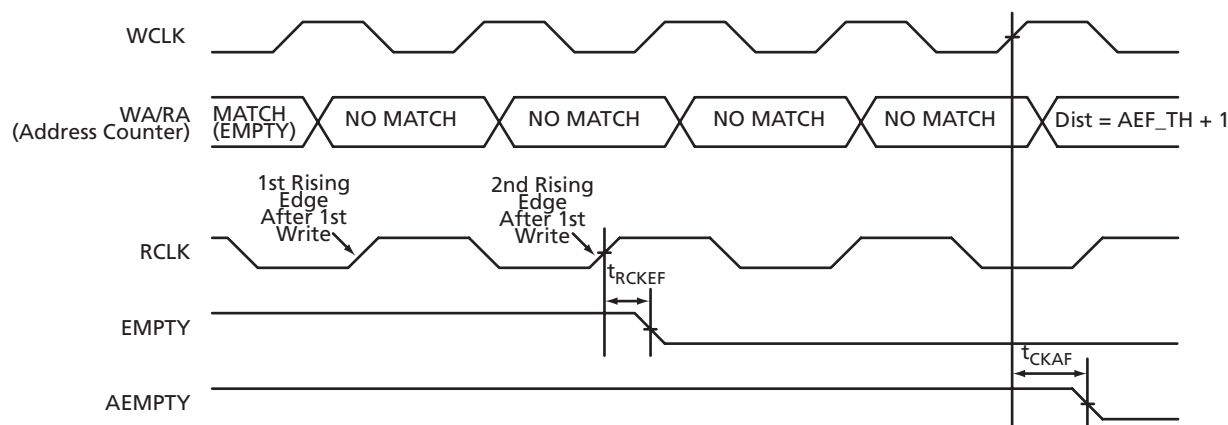


Figure 2-43 • FIFO EMPTY Flag and AEMPTY Flag Deassertion

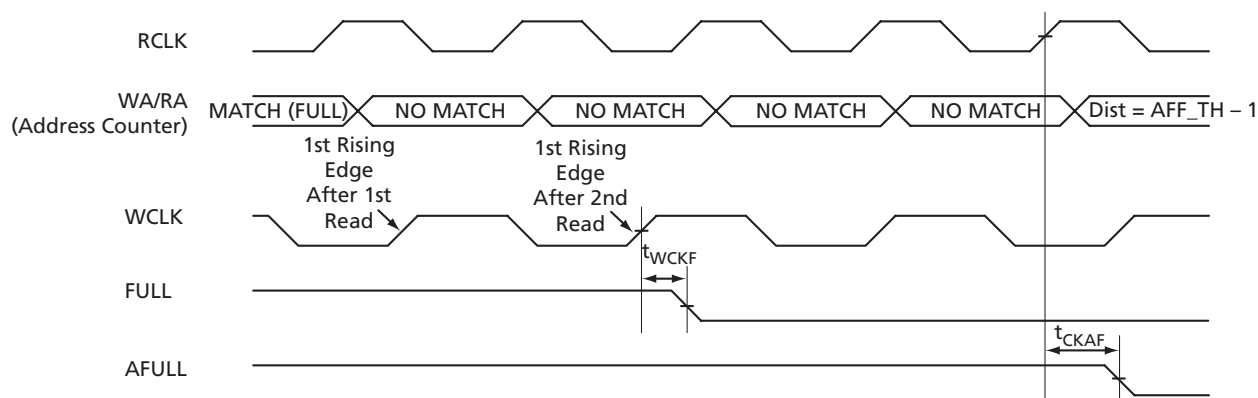


Figure 2-44 • FIFO FULL Flag and AFULL Flag Deassertion

Timing Characteristics

Table 2-121 • FIFO

Worst-Case Automotive Conditions: $T_J = 135^{\circ}\text{C}$, $V_{CC} = 1.425\text{ V}$

Parameter	Description	-1	Std.	Units
t_{ENS}	REN_B, WEN_B Setup Time	1.97	1.67	ns
t_{ENH}	REN_B, WEN_B Hold Time	0.03	0.02	ns
t_{BKS}	BLK_B Setup Time	0.28	0.32	ns
t_{BKH}	BLK_B Hold Time	0.00	0.00	ns
t_{DS}	Input Data (DI) Setup Time	0.26	0.22	ns
t_{DH}	Input Data (DI) Hold Time	0.00	0.00	ns
t_{CKQ1}	Clock HIGH to New Data Valid on DO (flow-through)	3.37	2.86	ns
t_{CKQ2}	Clock HIGH to New Data Valid on DO (pipelined)	1.28	1.09	ns
t_{RCKEF}	RCLK HIGH to Empty Flag Valid	2.45	2.09	ns
t_{WCKFF}	WCLK HIGH to Full Flag Valid	2.33	1.98	ns
t_{CKAF}	Clock HIGH to Almost Empty/Full Flag Valid	8.85	7.53	ns
t_{RSTFG}	RESET_B LOW to Empty/Full Flag Valid	2.42	2.06	ns
t_{RSTAF}	RESET_B LOW to Almost Empty/Full Flag Valid	8.76	7.45	ns
t_{RSTBQ}	RESET_B LOW to Data Out LOW on DO (flow-through)	1.32	1.12	ns
	RESET_B LOW to Data Out LOW on DO (pipelined)	1.32	1.12	ns
$t_{REMRSTB}$	RESET_B Removal	0.41	0.35	ns
$t_{RECRSTB}$	RESET_B Recovery	2.14	1.82	ns
$t_{MPWRSTB}$	RESET_B Minimum Pulse Width	0.30	0.26	ns
t_{CYC}	Clock Cycle Time	4.62	3.93	ns
F_{MAX}	Maximum Frequency for FIFO	217	255	MHz

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-5 on page 2-5](#) for derating values.

Table 2-122 • FIFO

Worst-Case Automotive Conditions: $T_J = 115^{\circ}\text{C}$, $V_{CC} = 1.425\text{ V}$

Parameter	Description	–1	Std.	Units
t_{ENS}	REN_B, WEN_B Setup Time	1.93	1.64	ns
t_{ENH}	REN_B, WEN_B Hold Time	0.03	0.02	ns
t_{BKS}	BLK_B Setup Time	0.27	0.32	ns
t_{BKH}	BLK_B Hold Time	0.00	0.00	ns
t_{DS}	Input Data (DI) Setup Time	0.26	0.22	ns
t_{DH}	Input Data (DI) Hold Time	0.00	0.00	ns
t_{CKQ1}	Clock HIGH to New Data Valid on DO (flow-through)	3.30	2.81	ns
t_{CKQ2}	Clock HIGH to New Data Valid on DO (pipelined)	1.25	1.07	ns
t_{RCKEF}	RCLK HIGH to Empty Flag Valid	2.41	2.05	ns
t_{WCKFF}	WCLK HIGH to Full Flag Valid	2.29	1.95	ns
t_{CKAF}	Clock HIGH to Almost Empty/Full Flag Valid	8.68	7.38	ns
t_{RSTFG}	RESET_B LOW to Empty/Full Flag Valid	2.37	2.02	ns
t_{RSTAF}	RESET_B LOW to Almost Empty/Full Flag Valid	8.59	7.30	ns
t_{RSTBQ}	RESET_B LOW to Data Out LOW on DO (flow-through)	1.29	1.10	ns
	RESET_B LOW to Data Out LOW on DO (pipelined)	1.29	1.10	ns
$t_{REMRSTB}$	RESET_B Removal	0.40	0.34	ns
$t_{RECRSTB}$	RESET_B Recovery	2.10	1.79	ns
$t_{MPWRSTB}$	RESET_B Minimum Pulse Width	0.30	0.25	ns
t_{CYC}	Clock Cycle Time	4.53	3.85	ns
F_{MAX}	Maximum Frequency for FIFO	221	260	MHz

Note: For specific junction temperature and voltage supply levels, refer to [Table 2-5 on page 2-5](#) for derating values.

Embedded FlashROM Characteristics

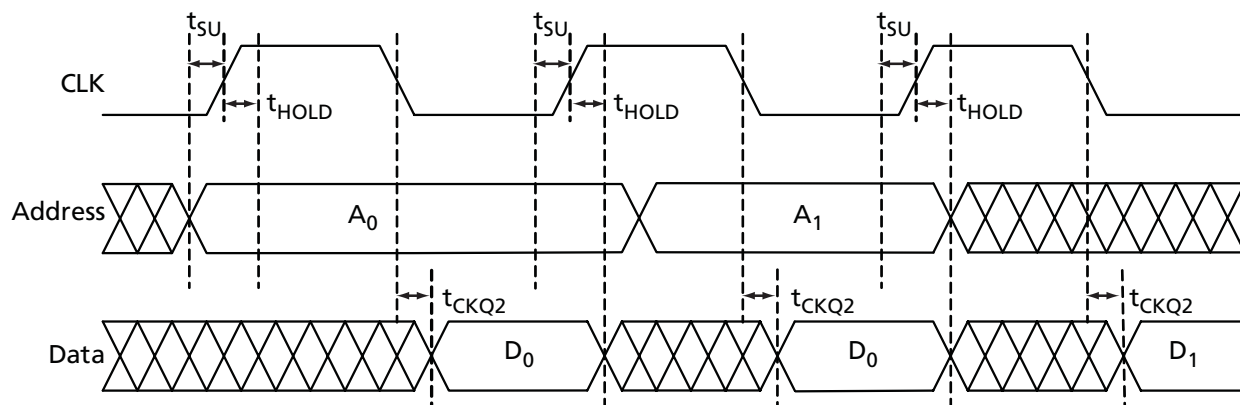


Figure 2-45 • Timing Diagram

Timing Characteristics

Table 2-123 • Embedded FlashROM Access Time

Automotive-Case Conditions: $T_J = 135^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$

Parameter	Description	–1	Std.	Units
t_{SU}	Address Setup Time	0.65	0.76	ns
t_{HOLD}	Address Hold Time	0.00	0.00	ns
t_{CKQ2}	Clock to Out	19.73	23.20	ns
F_{MAX}	Maximum Clock Frequency	15	15	MHz

Table 2-124 • Embedded FlashROM Access Time

Automotive-Case Conditions: $T_J = 115^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$

Parameter	Description	–1	Std.	Units
t_{SU}	Address Setup Time	0.64	0.75	ns
t_{HOLD}	Address Hold Time	0.00	0.00	ns
t_{CKQ2}	Clock to Out	19.35	22.74	ns
F_{MAX}	Maximum Clock Frequency	15	15	MHz

JTAG 1532 Characteristics

JTAG timing delays do not include JTAG I/Os. To obtain complete JTAG timing, add I/O buffer delays to the corresponding standard selected; refer to the I/O timing characteristics in the "User I/O Characteristics" section on page 2-12 for more details.

Timing Characteristics

Table 2-125 • JTAG 1532

Commercial-Case Conditions: $T_J = 70^\circ\text{C}$, Worst-Case $V_{CC} = 1.425\text{ V}$

Parameter	Description	-2	-1	Std.	Units
t_{DISU}	Test Data Input Setup Time				ns
t_{DIHD}	Test Data Input Hold Time				ns
t_{TMSSU}	Test Mode Select Setup Time				ns
t_{TMDHD}	Test Mode Select Hold Time				ns
t_{TCK2Q}	Clock to Q (data out)				ns
t_{RSTB2Q}	Reset to Q (data out)				ns
F_{TCKMAX}	TCK Maximum Frequency	20	20	20	MHz
$t_{TRSTREM}$	ResetB Removal Time				ns
$t_{TRSTREC}$	ResetB Recovery Time				ns
$t_{TRSTMPW}$	ResetB Minimum Pulse				ns

Note: For specific junction temperature and voltage supply levels, refer to Table 2-5 on page 2-5 for derating values.

Part Number and Revision Date

Part Number 51700099-002-0

Revised January 2008

Actel Safety Critical, Life Support, and High-Reliability Applications Policy

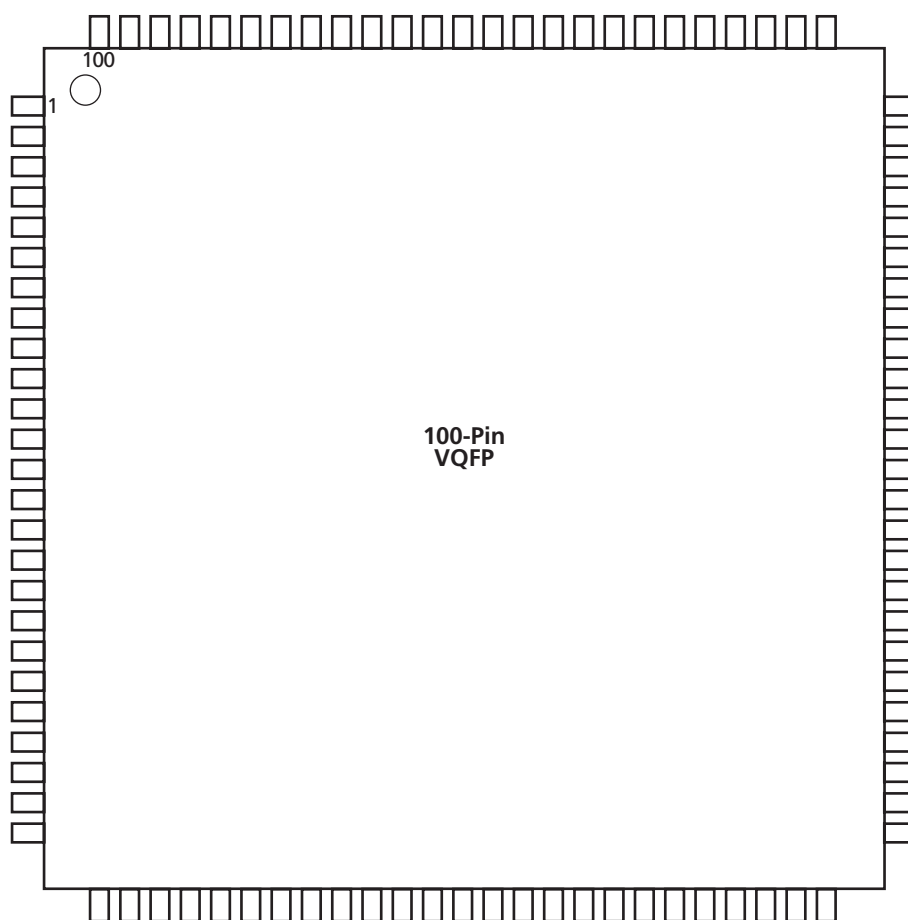
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[查询"A3P060-1FGG144T"供应商](#)



3 – Package Pin Assignments

100-Pin VQFP



Note: This is the top view of the package.

Note

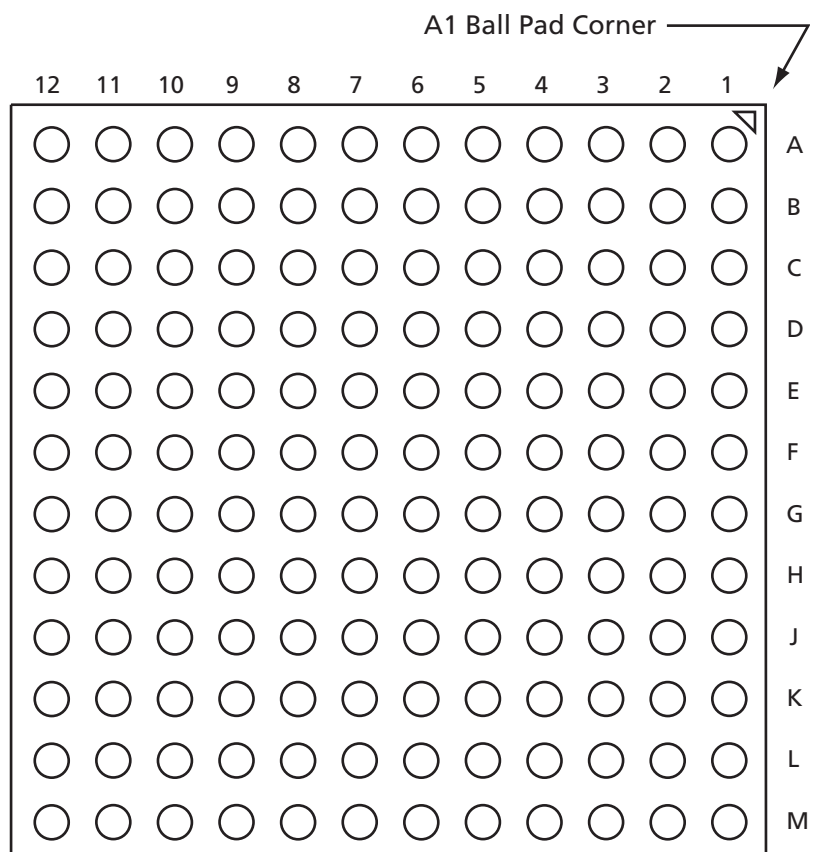
For Package Manufacturing and Environmental information, visit the Resource Center at <http://www.actel.com/products/solutions/package/docs.aspx>.

Package Pin Assignments

100-Pin VQFP		100-Pin VQFP		100-Pin VQFP	
Pin Number	A3P060 Function	Pin Number	A3P060 Function	Pin Number	A3P060 Function
1	GND	35	IO62RSB1	69	IO31RSB0
2	GAA2/IO51RSB1	36	IO61RSB1	70	GBC2/IO29RSB0
3	IO52RSB1	37	V _{CC}	71	GBB2/IO27RSB0
4	GAB2/IO53RSB1	38	GND	72	IO26RSB0
5	IO95RSB1	39	V _{CC} B1	73	GBA2/IO25RSB0
6	GAC2/IO94RSB1	40	IO60RSB1	74	VMV0
7	IO93RSB1	41	IO59RSB1	75	GNDQ
8	IO92RSB1	42	IO58RSB1	76	GBA1/IO24RSB0
9	GND	43	IO57RSB1	77	GBA0/IO23RSB0
10	GFB1/IO87RSB1	44	GDC2/IO56RSB1	78	GBB1/IO22RSB0
11	GFB0/IO86RSB1	45	GDB2/IO55RSB1	79	GBB0/IO21RSB0
12	V _{COMPLF}	46	GDA2/IO54RSB1	80	GBC1/IO20RSB0
13	GFA0/IO85RSB1	47	TCK	81	GBC0/IO19RSB0
14	V _{CCPLF}	48	TDI	82	IO18RSB0
15	GFA1/IO84RSB1	49	TMS	83	IO17RSB0
16	GFA2/IO83RSB1	50	VMV1	84	IO15RSB0
17	V _{CC}	51	GND	85	IO13RSB0
18	V _{CC} B1	52	V _{PUMP}	86	IO11RSB0
19	GEC1/IO77RSB1	53	NC	87	V _{CC} B0
20	GEB1/IO75RSB1	54	TDO	88	GND
21	GEB0/IO74RSB1	55	TRST	89	V _{CC}
22	GEA1/IO73RSB1	56	V _{JTAG}	90	IO10RSB0
23	GEA0/IO72RSB1	57	GDA1/IO49RSB0	91	IO09RSB0
24	VMV1	58	GDC0/IO46RSB0	92	IO08RSB0
25	GNDQ	59	GDC1/IO45RSB0	93	GAC1/IO07RSB0
26	GEA2/IO71RSB1	60	GCC2/IO43RSB0	94	GAC0/IO06RSB0
27	GEB2/IO70RSB1	61	GCB2/IO42RSB0	95	GAB1/IO05RSB0
28	GEC2/IO69RSB1	62	GCA0/IO40RSB0	96	GAB0/IO04RSB0
29	IO68RSB1	63	GCA1/IO39RSB0	97	GAA1/IO03RSB0
30	IO67RSB1	64	GCC0/IO36RSB0	98	GAA0/IO02RSB0
31	IO66RSB1	65	GCC1/IO35RSB0	99	IO01RSB0
32	IO65RSB1	66	V _{CC} B0	100	IO00RSB0
33	IO64RSB1	67	GND		
34	IO63RSB1	68	V _{CC}		

100-Pin VQFP		100-Pin VQFP		100-Pin VQFP	
Pin Number	A3P250 Function	Pin Number	A3P250 Function	Pin Number	A3P250 Function
1	GND	35	IO85RSB2	69	IO43NDB1
2	GAA2/IO118UDB3	36	IO84RSB2	70	GBC2/IO43PDB1
3	IO118VDB3	37	V _{CC}	71	GBB2/IO42PSB1
4	GAB2/IO117UDB3	38	GND	72	IO41NDB1
5	IO117VDB3	39	V _{CC} B2	73	GBA2/IO41PDB1
6	GAC2/IO116UDB3	40	IO77RSB2	74	VMV1
7	IO116VDB3	41	IO74RSB2	75	GNDQ
8	IO112PSB3	42	IO71RSB2	76	GBA1/IO40RSB0
9	GND	43	GDC2/IO63RSB2	77	GBA0/IO39RSB0
10	GFB1/IO109PDB3	44	GDB2/IO62RSB2	78	GBB1/IO38RSB0
11	GFB0/IO109NDB3	45	GDA2/IO61RSB2	79	GBB0/IO37RSB0
12	V _{COMPLF}	46	GNDQ	80	GBC1/IO36RSB0
13	GFA0/IO108NPB3	47	TCK	81	GBC0/IO35RSB0
14	V _{CCPLF}	48	TDI	82	IO29RSB0
15	GFA1/IO108PPB3	49	TMS	83	IO27RSB0
16	GFA2/IO107PSB3	50	VMV2	84	IO25RSB0
17	V _{CC}	51	GND	85	IO23RSB0
18	V _{CC} B3	52	V _{PUMP}	86	IO21RSB0
19	GFC2/IO105PSB3	53	NC	87	V _{CC} B0
20	GEC1/IO100PDB3	54	TDO	88	GND
21	GEC0/IO100NDB3	55	TRST	89	V _{CC}
22	GEA1/IO98PDB3	56	V _{JTAG}	90	IO15RSB0
23	GEA0/IO98NDB3	57	GDA1/IO60USB1	91	IO13RSB0
24	VMV3	58	GDC0/IO58VDB1	92	IO11RSB0
25	GNDQ	59	GDC1/IO58UDB1	93	GAC1/IO05RSB0
26	GEA2/IO97RSB2	60	IO52NDB1	94	GAC0/IO04RSB0
27	GEB2/IO96RSB2	61	GCB2/IO52PDB1	95	GAB1/IO03RSB0
28	GEC2/IO95RSB2	62	GCA1/IO50PDB1	96	GAB0/IO02RSB0
29	IO93RSB2	63	GCA0/IO50NDB1	97	GAA1/IO01RSB0
30	IO92RSB2	64	GCC0/IO48NDB1	98	GAA0/IO00RSB0
31	IO91RSB2	65	GCC1/IO48PDB1	99	GNDQ
32	IO90RSB2	66	V _{CC} B1	100	VMV0
33	IO88RSB2	67	GND		
34	IO86RSB2	68	V _{CC}		

144-Pin FBGA



Note: This is the bottom view of the package.

Note

For Package Manufacturing and Environmental information, visit the Resource Center at <http://www.actel.com/products/solutions/package/docs.aspx>.

144-Pin FBGA		144-Pin FBGA		144-Pin FBGA	
Pin Number	A3P060 Function	Pin Number	A3P060 Function	Pin Number	A3P060 Function
A1	GNDQ	D1	IO91RSB1	G1	GFA1/IO84RSB1
A2	VMV0	D2	IO92RSB1	G2	GND
A3	GAB0/IO04RSB0	D3	IO93RSB1	G3	V _{CCPLF}
A4	GAB1/IO05RSB0	D4	GAA2/IO51RSB1	G4	GFA0/IO85RSB1
A5	IO08RSB0	D5	GAC0/IO06RSB0	G5	GND
A6	GND	D6	GAC1/IO07RSB0	G6	GND
A7	IO11RSB0	D7	GBC0/IO19RSB0	G7	GND
A8	V _{CC}	D8	GBC1/IO20RSB0	G8	GDC1/IO45RSB0
A9	IO16RSB0	D9	GBB2/IO27RSB0	G9	IO32RSB0
A10	GBA0/IO23RSB0	D10	IO18RSB0	G10	GCC2/IO43RSB0
A11	GBA1/IO24RSB0	D11	IO28RSB0	G11	IO31RSB0
A12	GNDQ	D12	GCB1/IO37RSB0	G12	GCB2/IO42RSB0
B1	GAB2/IO53RSB1	E1	V _{CC}	H1	V _{CC}
B2	GND	E2	GFC0/IO88RSB1	H2	GFB2/IO82RSB1
B3	GAA0/IO02RSB0	E3	GFC1/IO89RSB1	H3	GFC2/IO81RSB1
B4	GAA1/IO03RSB0	E4	V _{CC} B1	H4	GEC1/IO77RSB1
B5	IO00RSB0	E5	IO52RSB1	H5	V _{CC}
B6	IO10RSB0	E6	V _{CC} B0	H6	IO34RSB0
B7	IO12RSB0	E7	V _{CC} B0	H7	IO44RSB0
B8	IO14RSB0	E8	GCC1/IO35RSB0	H8	GDB2/IO55RSB1
B9	GBB0/IO21RSB0	E9	V _{CC} B0	H9	GDC0/IO46RSB0
B10	GBB1/IO22RSB0	E10	V _{CC}	H10	V _{CC} B0
B11	GND	E11	GCA0/IO40RSB0	H11	IO33RSB0
B12	VMV0	E12	IO30RSB0	H12	V _{CC}
C1	IO95RSB1	F1	GFB0/IO86RSB1	J1	GEB1/IO75RSB1
C2	GFA2/IO83RSB1	F2	V _{CC} COMPLF	J2	IO78RSB1
C3	GAC2/IO94RSB1	F3	GFB1/IO87RSB1	J3	V _{CC} B1
C4	V _{CC}	F4	IO90RSB1	J4	GEC0/IO76RSB1
C5	IO01RSB0	F5	GND	J5	IO79RSB1
C6	IO09RSB0	F6	GND	J6	IO80RSB1
C7	IO13RSB0	F7	GND	J7	V _{CC}
C8	IO15RSB0	F8	GCC0/IO36RSB0	J8	TCK
C9	IO17RSB0	F9	GCB0/IO38RSB0	J9	GDA2/IO54RSB1
C10	GBA2/IO25RSB0	F10	GND	J10	TDO
C11	IO26RSB0	F11	GCA1/IO39RSB0	J11	GDA1/IO49RSB0
C12	GBC2/IO29RSB0	F12	GCA2/IO41RSB0	J12	GDB1/IO47RSB0

Package Pin Assignments

144-Pin FBGA	
Pin Number	A3P060 Function
K1	GEB0/IO74RSB1
K2	GEA1/IO73RSB1
K3	GEA0/IO72RSB1
K4	GEA2/IO71RSB1
K5	IO65RSB1
K6	IO64RSB1
K7	GND
K8	IO57RSB1
K9	GDC2/IO56RSB1
K10	GND
K11	GDA0/IO50RSB0
K12	GDB0/IO48RSB0
L1	GND
L2	VMV1
L3	GEB2/IO70RSB1
L4	IO67RSB1
L5	V _{CC} B1
L6	IO62RSB1
L7	IO59RSB1
L8	IO58RSB1
L9	TMS
L10	V _{JTAG}
L11	VMV1
L12	TRST
M1	GNDQ
M2	GEC2/IO69RSB1
M3	IO68RSB1
M4	IO66RSB1
M5	IO63RSB1
M6	IO61RSB1
M7	IO60RSB1
M8	NC
M9	TDI
M10	V _{CC} B1
M11	V _{PUMP}
M12	GNDQ

144-Pin FBGA		144-Pin FBGA		144-Pin FBGA	
Pin Number	A3P125 Function	Pin Number	A3P125 Function	Pin Number	A3P125 Function
A1	GNDQ	D1	IO128RSB1	G1	GFA1/IO121RSB1
A2	VMV0	D2	IO129RSB1	G2	GND
A3	GAB0/IO02RSB0	D3	IO130RSB1	G3	V _{CCPLF}
A4	GAB1/IO03RSB0	D4	GAA2/IO67RSB1	G4	GFA0/IO122RSB1
A5	IO11RSB0	D5	GAC0/IO04RSB0	G5	GND
A6	GND	D6	GAC1/IO05RSB0	G6	GND
A7	IO18RSB0	D7	GBC0/IO35RSB0	G7	GND
A8	V _{CC}	D8	GBC1/IO36RSB0	G8	GDC1/IO61RSB0
A9	IO25RSB0	D9	GBB2/IO43RSB0	G9	IO48RSB0
A10	GBA0/IO39RSB0	D10	IO28RSB0	G10	GCC2/IO59RSB0
A11	GBA1/IO40RSB0	D11	IO44RSB0	G11	IO47RSB0
A12	GNDQ	D12	GCB1/IO53RSB0	G12	GCB2/IO58RSB0
B1	GAB2/IO69RSB1	E1	V _{CC}	H1	V _{CC}
B2	GND	E2	GFC0/IO125RSB1	H2	GFB2/IO119RSB1
B3	GAA0/IO00RSB0	E3	GFC1/IO126RSB1	H3	GFC2/IO118RSB1
B4	GAA1/IO01RSB0	E4	V _{CC} B1	H4	GEC1/IO112RSB1
B5	IO08RSB0	E5	IO68RSB1	H5	V _{CC}
B6	IO14RSB0	E6	V _{CC} B0	H6	IO50RSB0
B7	IO19RSB0	E7	V _{CC} B0	H7	IO60RSB0
B8	IO22RSB0	E8	GCC1/IO51RSB0	H8	GDB2/IO71RSB1
B9	GBB0/IO37RSB0	E9	V _{CC} B0	H9	GDC0/IO62RSB0
B10	GBB1/IO38RSB0	E10	V _{CC}	H10	V _{CC} B0
B11	GND	E11	GCA0/IO56RSB0	H11	IO49RSB0
B12	VMV0	E12	IO46RSB0	H12	V _{CC}
C1	IO132RSB1	F1	GFB0/IO123RSB1	J1	GEB1/IO110RSB1
C2	GFA2/IO120RSB1	F2	V _{COMPLF}	J2	IO115RSB1
C3	GAC2/IO131RSB1	F3	GFB1/IO124RSB1	J3	V _{CC} B1
C4	V _{CC}	F4	IO127RSB1	J4	GEC0/IO111RSB1
C5	IO10RSB0	F5	GND	J5	IO116RSB1
C6	IO12RSB0	F6	GND	J6	IO117RSB1
C7	IO21RSB0	F7	GND	J7	V _{CC}
C8	IO24RSB0	F8	GCC0/IO52RSB0	J8	TCK
C9	IO27RSB0	F9	GCB0/IO54RSB0	J9	GDA2/IO70RSB1
C10	GBA2/IO41RSB0	F10	GND	J10	TDO
C11	IO42RSB0	F11	GCA1/IO55RSB0	J11	GDA1/IO65RSB0
C12	GBC2/IO45RSB0	F12	GCA2/IO57RSB0	J12	GDB1/IO63RSB0

Package Pin Assignments

144-Pin FBGA	
Pin Number	A3P125 Function
K1	GEB0/IO109RSB1
K2	GEA1/IO108RSB1
K3	GEA0/IO107RSB1
K4	GEA2/IO106RSB1
K5	IO100RSB1
K6	IO98RSB1
K7	GND
K8	IO73RSB1
K9	GDC2/IO72RSB1
K10	GND
K11	GDA0/IO66RSB0
K12	GDB0/IO64RSB0
L1	GND
L2	VMV1
L3	GEB2/IO105RSB1
L4	IO102RSB1
L5	V _{CC} B1
L6	IO95RSB1
L7	IO85RSB1
L8	IO74RSB1
L9	TMS
L10	V _{JTAG}
L11	VMV1
L12	TRST
M1	GNDQ
M2	GEC2/IO104RSB1
M3	IO103RSB1
M4	IO101RSB1
M5	IO97RSB1
M6	IO94RSB1
M7	IO86RSB1
M8	IO75RSB1
M9	TDI
M10	V _{CC} B1
M11	V _{PUMP}
M12	GNDQ

144-Pin FBGA		144-Pin FBGA		144-Pin FBGA	
Pin Number	A3P250 Function	Pin Number	A3P250 Function	Pin Number	A3P250 Function
A1	GNDQ	D1	IO112NDB3	G1	GFA1/IO108PPB3
A2	VMV0	D2	IO112PDB3	G2	GND
A3	GAB0/IO02RSB0	D3	IO116VDB3	G3	V _{CCPLF}
A4	GAB1/IO03RSB0	D4	GAA2/IO118UPB3	G4	GFA0/IO108NPB3
A5	IO16RSB0	D5	GAC0/IO04RSB0	G5	GND
A6	GND	D6	GAC1/IO05RSB0	G6	GND
A7	IO29RSB0	D7	GBC0/IO35RSB0	G7	GND
A8	V _{CC}	D8	GBC1/IO36RSB0	G8	GDC1/IO58UPB1
A9	IO33RSB0	D9	GBB2/IO42PDB1	G9	IO53NDB1
A10	GBA0/IO39RSB0	D10	IO42NDB1	G10	GCC2/IO53PDB1
A11	GBA1/IO40RSB0	D11	IO43NPB1	G11	IO52NDB1
A12	GNDQ	D12	GCB1/IO49PPB1	G12	GCB2/IO52PDB1
B1	GAB2/IO117UDB3	E1	V _{CC}	H1	V _{CC}
B2	GND	E2	GFC0/IO110NDB3	H2	GFB2/IO106PDB3
B3	GAA0/IO00RSB0	E3	GFC1/IO110PDB3	H3	GFC2/IO105PSB3
B4	GAA1/IO01RSB0	E4	V _{CC} B3	H4	GEC1/IO100PDB3
B5	IO14RSB0	E5	IO118VPB3	H5	V _{CC}
B6	IO19RSB0	E6	V _{CC} B0	H6	IO79RSB2
B7	IO22RSB0	E7	V _{CC} B0	H7	IO65RSB2
B8	IO30RSB0	E8	GCC1/IO48PDB1	H8	GDB2/IO62RSB2
B9	GBB0/IO37RSB0	E9	V _{CC} B1	H9	GDC0/IO58VPB1
B10	GBB1/IO38RSB0	E10	V _{CC}	H10	V _{CC} B1
B11	GND	E11	GCA0/IO50NDB1	H11	IO54PSB1
B12	VMV1	E12	IO51NDB1	H12	V _{CC}
C1	IO117VDB3	F1	GFB0/IO109NPB3	J1	GEB1/IO99PDB3
C2	GFA2/IO107PPB3	F2	V _{COMPLF}	J2	IO106NDB3
C3	GAC2/IO116UDB3	F3	GFB1/IO109PPB3	J3	V _{CC} B3
C4	V _{CC}	F4	IO107NPB3	J4	GEC0/IO100NDB3
C5	IO12RSB0	F5	GND	J5	IO88RSB2
C6	IO17RSB0	F6	GND	J6	IO81RSB2
C7	IO24RSB0	F7	GND	J7	V _{CC}
C8	IO31RSB0	F8	GCC0/IO48NDB1	J8	TCK
C9	IO34RSB0	F9	GCB0/IO49NPB1	J9	GDA2/IO61RSB2
C10	GBA2/IO41PDB1	F10	GND	J10	TDO
C11	IO41NDB1	F11	GCA1/IO50PDB1	J11	GDA1/IO60UDB1
C12	GBC2/IO43PPB1	F12	GCA2/IO51PDB1	J12	GDB1/IO59UDB1

Package Pin Assignments

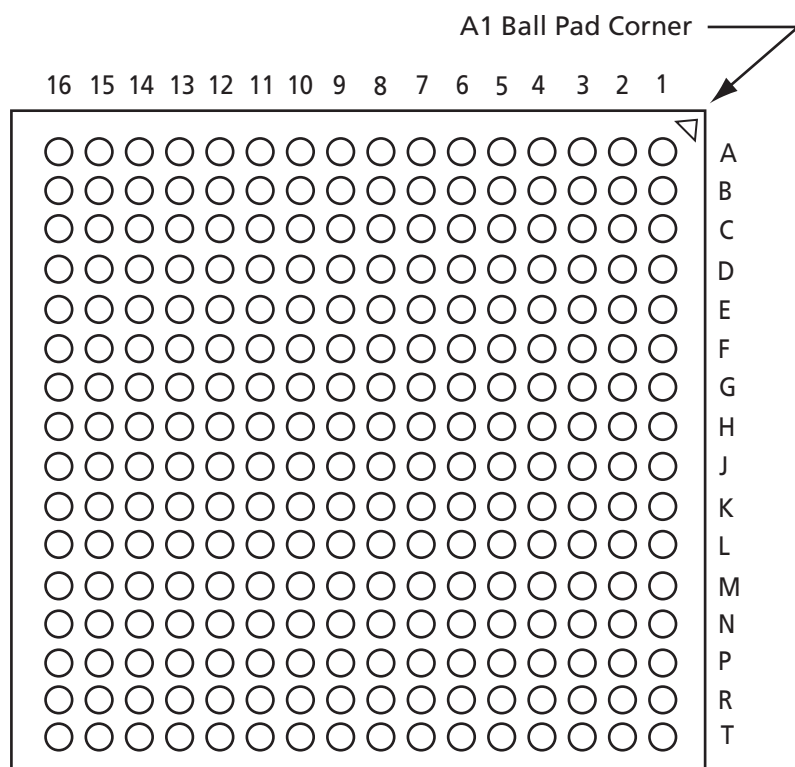
144-Pin FBGA	
Pin Number	A3P250 Function
K1	GEB0/IO99NDB3
K2	GEA1/IO98PDB3
K3	GEA0/IO98NDB3
K4	GEA2/IO97RSB2
K5	IO90RSB2
K6	IO84RSB2
K7	GND
K8	IO66RSB2
K9	GDC2/IO63RSB2
K10	GND
K11	GDA0/IO60VDB1
K12	GDB0/IO59VDB1
L1	GND
L2	VMV3
L3	GEB2/IO96RSB2
L4	IO91RSB2
L5	V _{CC} B2
L6	IO82RSB2
L7	IO80RSB2
L8	IO72RSB2
L9	TMS
L10	V _{JTAG}
L11	VMV2
L12	TRST
M1	GNDQ
M2	GEC2/IO95RSB2
M3	IO92RSB2
M4	IO89RSB2
M5	IO87RSB2
M6	IO85RSB2
M7	IO78RSB2
M8	IO76RSB2
M9	TDI
M10	V _{CC} B2
M11	V _{PUMP}
M12	GNDQ

144-Pin FBGA		144-Pin FBGA		144-Pin FBGA	
Pin Number	A3P1000 Function	Pin Number	A3P1000 Function	Pin Number	A3P1000 Function
A1	GNDQ	D1	IO213PDB3	G1	GFA1/IO207PPB3
A2	VMV0	D2	IO213NDB3	G2	GND
A3	GAB0/IO02RSB0	D3	IO223NDB3	G3	V _{CCPLF}
A4	GAB1/IO03RSB0	D4	GAA2/IO225PPB3	G4	GFA0/IO207NPB3
A5	IO10RSB0	D5	GAC0/IO04RSB0	G5	GND
A6	GND	D6	GAC1/IO05RSB0	G6	GND
A7	IO44RSB0	D7	GBC0/IO72RSB0	G7	GND
A8	V _{CC}	D8	GBC1/IO73RSB0	G8	GDC1/IO111PPB1
A9	IO69RSB0	D9	GBB2/IO79PDB1	G9	IO96NDB1
A10	GBA0/IO76RSB0	D10	IO79NDB1	G10	GCC2/IO96PDB1
A11	GBA1/IO77RSB0	D11	IO80NPB1	G11	IO95NDB1
A12	GNDQ	D12	GCB1/IO92PPB1	G12	GCB2/IO95PDB1
B1	GAB2/IO224PDB3	E1	V _{CC}	H1	V _{CC}
B2	GND	E2	GFC0/IO209NDB3	H2	GFB2/IO205PDB3
B3	GAA0/IO00RSB0	E3	GFC1/IO209PDB3	H3	GFC2/IO204PSB3
B4	GAA1/IO01RSB0	E4	V _{CCIB3}	H4	GEC1/IO190PDB3
B5	IO13RSB0	E5	IO225NPB3	H5	V _{CC}
B6	IO26RSB0	E6	V _{CCIB0}	H6	IO105PDB1
B7	IO35RSB0	E7	V _{CCIB0}	H7	IO105NDB1
B8	IO60RSB0	E8	GCC1/IO91PDB1	H8	GDB2/IO115RSB2
B9	GBB0/IO74RSB0	E9	V _{CCIB1}	H9	GDC0/IO111NPB1
B10	GBB1/IO75RSB0	E10	V _{CC}	H10	V _{CCIB1}
B11	GND	E11	GCA0/IO93NDB1	H11	IO101PSB1
B12	VMV1	E12	IO94NDB1	H12	V _{CC}
C1	IO224NDB3	F1	GFB0/IO208NPB3	J1	GEB1/IO189PDB3
C2	GFA2/IO206PPB3	F2	V _{COMPLF}	J2	IO205NDB3
C3	GAC2/IO223PDB3	F3	GFB1/IO208PPB3	J3	V _{CCIB3}
C4	V _{CC}	F4	IO206NPB3	J4	GEC0/IO190NDB3
C5	IO16RSB0	F5	GND	J5	IO160RSB2
C6	IO29RSB0	F6	GND	J6	IO157RSB2
C7	IO32RSB0	F7	GND	J7	V _{CC}
C8	IO63RSB0	F8	GCC0/IO91NDB1	J8	TCK
C9	IO66RSB0	F9	GCB0/IO92NPB1	J9	GDA2/IO114RSB2
C10	GBA2/IO78PDB1	F10	GND	J10	TDO
C11	IO78NDB1	F11	GCA1/IO93PDB1	J11	GDA1/IO113PDB1
C12	GBC2/IO80PPB1	F12	GCA2/IO94PDB1	J12	GDB1/IO112PDB1

Package Pin Assignments

144-Pin FBGA	
Pin Number	A3P1000 Function
K1	GEB0/IO189NDB3
K2	GEA1/IO188PDB3
K3	GEA0/IO188NDB3
K4	GEA2/IO187RSB2
K5	IO169RSB2
K6	IO152RSB2
K7	GND
K8	IO117RSB2
K9	GDC2/IO116RSB2
K10	GND
K11	GDA0/IO113NDB1
K12	GDB0/IO112NDB1
L1	GND
L2	VMV3
L3	GEB2/IO186RSB2
L4	IO172RSB2
L5	V _{CC} B2
L6	IO153RSB2
L7	IO144RSB2
L8	IO140RSB2
L9	TMS
L10	V _{JTAG}
L11	VMV2
L12	TRST
M1	GNDQ
M2	GEC2/IO185RSB2
M3	IO173RSB2
M4	IO168RSB2
M5	IO161RSB2
M6	IO156RSB2
M7	IO145RSB2
M8	IO141RSB2
M9	TDI
M10	V _{CC} B2
M11	V _{PUMP}
M12	GNDQ

256-Pin FBGA



Note: This is the bottom view of the package.

Note

For Package Manufacturing and Environmental information, visit the Resource Center at <http://www.actel.com/products/solutions/package/docs.aspx>.

Package Pin Assignments

256-Pin FBGA		256-Pin FBGA		256-Pin FBGA	
Pin Number	A3P250 Function	Pin Number	A3P250 Function	Pin Number	A3P250 Function
A1	GND	C5	GAC0/IO04RSB0	E9	IO24RSB0
A2	GAA0/IO00RSB0	C6	GAC1/IO05RSB0	E10	V _{CC} B0
A3	GAA1/IO01RSB0	C7	IO13RSB0	E11	V _{CC} B0
A4	GAB0/IO02RSB0	C8	IO17RSB0	E12	VMV1
A5	IO07RSB0	C9	IO22RSB0	E13	GBC2/IO43PDB1
A6	IO10RSB0	C10	IO27RSB0	E14	IO46RSB1
A7	IO11RSB0	C11	IO31RSB0	E15	NC
A8	IO15RSB0	C12	GBC0/IO35RSB0	E16	IO45PDB1
A9	IO20RSB0	C13	IO34RSB0	F1	IO113NDB3
A10	IO25RSB0	C14	NC	F2	IO112PPB3
A11	IO29RSB0	C15	IO42NPB1	F3	NC
A12	IO33RSB0	C16	IO44PDB1	F4	IO115VDB3
A13	GBB1/IO38RSB0	D1	IO114VDB3	F5	V _{CC} B3
A14	GBA0/IO39RSB0	D2	IO114UDB3	F6	GND
A15	GBA1/IO40RSB0	D3	GAC2/IO116UDB3	F7	V _{CC}
A16	GND	D4	NC	F8	V _{CC}
B1	GAB2/IO117UDB3	D5	GNDQ	F9	V _{CC}
B2	GAA2/IO118UDB3	D6	IO08RSB0	F10	V _{CC}
B3	NC	D7	IO14RSB0	F11	GND
B4	GAB1/IO03RSB0	D8	IO18RSB0	F12	V _{CC} B1
B5	IO06RSB0	D9	IO23RSB0	F13	IO43NDB1
B6	IO09RSB0	D10	IO28RSB0	F14	NC
B7	IO12RSB0	D11	IO32RSB0	F15	IO47PPB1
B8	IO16RSB0	D12	GNDQ	F16	IO45NDB1
B9	IO21RSB0	D13	NC	G1	IO111NDB3
B10	IO26RSB0	D14	GBB2/IO42PPB1	G2	IO111PDB3
B11	IO30RSB0	D15	NC	G3	IO112NPB3
B12	GBC1/IO36RSB0	D16	IO44NDB1	G4	GFC1/IO110PPB3
B13	GBB0/IO37RSB0	E1	IO113PDB3	G5	V _{CC} B3
B14	NC	E2	NC	G6	V _{CC}
B15	GBA2/IO41PDB1	E3	IO116VDB3	G7	GND
B16	IO41NDB1	E4	IO115UDB3	G8	GND
C1	IO117VDB3	E5	VMV0	G9	GND
C2	IO118VDB3	E6	V _{CC} B0	G10	GND
C3	NC	E7	V _{CC} B0	G11	V _{CC}
C4	NC	E8	IO19RSB0	G12	V _{CC} B1

256-Pin FBGA		256-Pin FBGA		256-Pin FBGA	
Pin Number	A3P250 Function	Pin Number	A3P250 Function	Pin Number	A3P250 Function
G13	GCC1/IO48PPB1	K1	GFC2/IO105PDB3	M5	VMV3
G14	IO47NPB1	K2	IO107NPB3	M6	V _{CC} B2
G15	IO54PDB1	K3	IO104PPB3	M7	V _{CC} B2
G16	IO54NDB1	K4	NC	M8	NC
H1	GFB0/IO109NPB3	K5	V _{CC} B3	M9	IO74RSB2
H2	GFA0/IO108NDB3	K6	V _{CC}	M10	V _{CC} B2
H3	GFB1/IO109PPB3	K7	GND	M11	V _{CC} B2
H4	V _{COMPLF}	K8	GND	M12	VMV2
H5	GFC0/IO110NPB3	K9	GND	M13	NC
H6	V _{CC}	K10	GND	M14	GDB1/IO59UPB1
H7	GND	K11	V _{CC}	M15	GDC1/IO58UDB1
H8	GND	K12	V _{CC} B1	M16	IO56NDB1
H9	GND	K13	IO52NPB1	N1	IO103NDB3
H10	GND	K14	IO55RSB1	N2	IO101PPB3
H11	V _{CC}	K15	IO53NPB1	N3	GEC1/IO100PPB3
H12	GCC0/IO48NPB1	K16	IO51NDB1	N4	NC
H13	GCB1/IO49PPB1	L1	IO105NDB3	N5	GNDQ
H14	GCA0/IO50NPB1	L2	IO104NPB3	N6	GEA2/IO97RSB2
H15	NC	L3	NC	N7	IO86RSB2
H16	GCB0/IO49NPB1	L4	IO102RSB3	N8	IO82RSB2
J1	GFA2/IO107PPB3	L5	V _{CC} B3	N9	IO75RSB2
J2	GFA1/IO108PDB3	L6	GND	N10	IO69RSB2
J3	V _{CC} PLF	L7	V _{CC}	N11	IO64RSB2
J4	IO106NDB3	L8	V _{CC}	N12	GNDQ
J5	GFB2/IO106PDB3	L9	V _{CC}	N13	NC
J6	V _{CC}	L10	V _{CC}	N14	V _{JTAG}
J7	GND	L11	GND	N15	GDC0/IO58VDB1
J8	GND	L12	V _{CC} B1	N16	GDA1/IO60UDB1
J9	GND	L13	GDB0/IO59VPB1	P1	GEB1/IO99PDB3
J10	GND	L14	IO57VDB1	P2	GEB0/IO99NDB3
J11	V _{CC}	L15	IO57UDB1	P3	NC
J12	GCB2/IO52PPB1	L16	IO56PDB1	P4	NC
J13	GCA1/IO50PPB1	M1	IO103PDB3	P5	IO92RSB2
J14	GCC2/IO53PPB1	M2	NC	P6	IO89RSB2
J15	NC	M3	IO101NPB3	P7	IO85RSB2
J16	GCA2/IO51PDB1	M4	GEC0/IO100NPB3	P8	IO81RSB2

Package Pin Assignments

256-Pin FBGA	
Pin Number	A3P250 Function
P9	IO76RSB2
P10	IO71RSB2
P11	IO66RSB2
P12	NC
P13	TCK
P14	V _{PUMP}
P15	TRST
P16	GDA0/IO60VDB1
R1	GEA1/IO98PDB3
R2	GEA0/IO98NDB3
R3	NC
R4	GEC2/IO95RSB2
R5	IO91RSB2
R6	IO88RSB2
R7	IO84RSB2
R8	IO80RSB2
R9	IO77RSB2
R10	IO72RSB2
R11	IO68RSB2
R12	IO65RSB2
R13	GDB2/IO62RSB2
R14	TDI
R15	NC
R16	TDO
T1	GND
T2	IO94RSB2
T3	GEB2/IO96RSB2
T4	IO93RSB2
T5	IO90RSB2
T6	IO87RSB2
T7	IO83RSB2
T8	IO79RSB2
T9	IO78RSB2
T10	IO73RSB2
T11	IO70RSB2
T12	GDC2/IO63RSB2

256-Pin FBGA	
Pin Number	A3P250 Function
T13	IO67RSB2
T14	GDA2/IO61RSB2
T15	TMS
T16	GND

256-Pin FBGA		256-Pin FBGA		256-Pin FBGA	
Pin Number	A3P1000 Function	Pin Number	A3P1000 Function	Pin Number	A3P1000 Function
A1	GND	C5	GAC0/IO04RSB0	E9	IO47RSB0
A2	GAA0/IO00RSB0	C6	GAC1/IO05RSB0	E10	V _{CC} B0
A3	GAA1/IO01RSB0	C7	IO25RSB0	E11	V _{CC} B0
A4	GAB0/IO02RSB0	C8	IO36RSB0	E12	VMV1
A5	IO16RSB0	C9	IO42RSB0	E13	GBC2/IO80PDB1
A6	IO22RSB0	C10	IO49RSB0	E14	IO83PPB1
A7	IO28RSB0	C11	IO56RSB0	E15	IO86PPB1
A8	IO35RSB0	C12	GBC0/IO72RSB0	E16	IO87PDB1
A9	IO45RSB0	C13	IO62RSB0	F1	IO217NDB3
A10	IO50RSB0	C14	VMV0	F2	IO218NDB3
A11	IO55RSB0	C15	IO78NDB1	F3	IO216PDB3
A12	IO61RSB0	C16	IO81NDB1	F4	IO216NDB3
A13	GBB1/IO75RSB0	D1	IO222NDB3	F5	V _{CC} B3
A14	GBA0/IO76RSB0	D2	IO222PDB3	F6	GND
A15	GBA1/IO77RSB0	D3	GAC2/IO223PDB3	F7	V _{CC}
A16	GND	D4	IO223NDB3	F8	V _{CC}
B1	GAB2/IO224PDB3	D5	GNDQ	F9	V _{CC}
B2	GAA2/IO225PDB3	D6	IO23RSB0	F10	V _{CC}
B3	GNDQ	D7	IO29RSB0	F11	GND
B4	GAB1/IO03RSB0	D8	IO33RSB0	F12	V _{CC} B1
B5	IO17RSB0	D9	IO46RSB0	F13	IO83NPB1
B6	IO21RSB0	D10	IO52RSB0	F14	IO86NPB1
B7	IO27RSB0	D11	IO60RSB0	F15	IO90PPB1
B8	IO34RSB0	D12	GNDQ	F16	IO87NDB1
B9	IO44RSB0	D13	IO80NDB1	G1	IO210PSB3
B10	IO51RSB0	D14	GBB2/IO79PDB1	G2	IO213NDB3
B11	IO57RSB0	D15	IO79NDB1	G3	IO213PDB3
B12	GBC1/IO73RSB0	D16	IO82NSB1	G4	GFC1/IO209PPB3
B13	GBB0/IO74RSB0	E1	IO217PDB3	G5	V _{CC} B3
B14	IO71RSB0	E2	IO218PDB3	G6	V _{CC}
B15	GBA2/IO78PDB1	E3	IO221NDB3	G7	GND
B16	IO81PDB1	E4	IO221PDB3	G8	GND
C1	IO224NDB3	E5	VMV0	G9	GND
C2	IO225NDB3	E6	V _{CC} B0	G10	GND
C3	VMV3	E7	V _{CC} B0	G11	V _{CC}
C4	IO11RSB0	E8	IO38RSB0	G12	V _{CC} B1

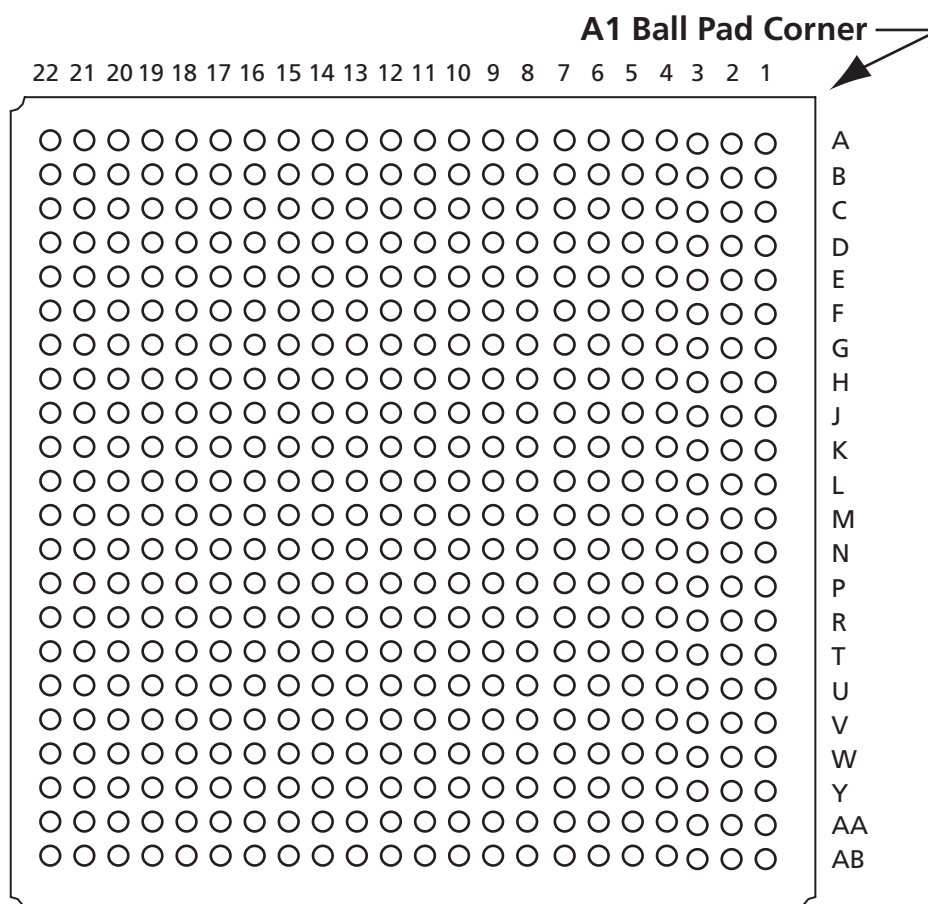
Package Pin Assignments

256-Pin FBGA		256-Pin FBGA		256-Pin FBGA	
Pin Number	A3P1000 Function	Pin Number	A3P1000 Function	Pin Number	A3P1000 Function
G13	GCC1/IO91PPB1	K1	GFC2/IO204PDB3	M5	VMV3
G14	IO90NPB1	K2	IO204NDB3	M6	V _{CC} B2
G15	IO88PDB1	K3	IO203NDB3	M7	V _{CC} B2
G16	IO88NDB1	K4	IO203PDB3	M8	IO147RSB2
H1	GFB0/IO208NPB3	K5	V _{CC} B3	M9	IO136RSB2
H2	GFA0/IO207NDB3	K6	V _{CC}	M10	V _{CC} B2
H3	GFB1/IO208PPB3	K7	GND	M11	V _{CC} B2
H4	V _{COMPLF}	K8	GND	M12	VMV2
H5	GFC0/IO209NPB3	K9	GND	M13	IO110NDB1
H6	V _{CC}	K10	GND	M14	GDB1/IO112PPB1
H7	GND	K11	V _{CC}	M15	GDC1/IO111PDB1
H8	GND	K12	V _{CC} B1	M16	IO107NDB1
H9	GND	K13	IO95NPB1	N1	IO194PSB3
H10	GND	K14	IO100NPB1	N2	IO192PPB3
H11	V _{CC}	K15	IO102NDB1	N3	GEC1/IO190PPB3
H12	GCC0/IO91NPB1	K16	IO102PDB1	N4	IO192NPB3
H13	GCB1/IO92PPB1	L1	IO202NDB3	N5	GNDQ
H14	GCA0/IO93NPB1	L2	IO202PDB3	N6	GEA2/IO187RSB2
H15	IO96NPB1	L3	IO196PPB3	N7	IO161RSB2
H16	GCB0/IO92NPB1	L4	IO193PPB3	N8	IO155RSB2
J1	GFA2/IO206PSB3	L5	V _{CC} B3	N9	IO141RSB2
J2	GFA1/IO207PDB3	L6	GND	N10	IO129RSB2
J3	V _{CC} PLF	L7	V _{CC}	N11	IO124RSB2
J4	IO205NDB3	L8	V _{CC}	N12	GNDQ
J5	GFB2/IO205PDB3	L9	V _{CC}	N13	IO110PDB1
J6	V _{CC}	L10	V _{CC}	N14	V _{JTAG}
J7	GND	L11	GND	N15	GDC0/IO111NDB1
J8	GND	L12	V _{CC} B1	N16	GDA1/IO113PDB1
J9	GND	L13	GDB0/IO112NPB1	P1	GEB1/IO189PDB3
J10	GND	L14	IO106NDB1	P2	GEB0/IO189NDB3
J11	V _{CC}	L15	IO106PDB1	P3	VMV2
J12	GCB2/IO95PPB1	L16	IO107PDB1	P4	IO179RSB2
J13	GCA1/IO93PPB1	M1	IO197NSB3	P5	IO171RSB2
J14	GCC2/IO96PPB1	M2	IO196NPB3	P6	IO165RSB2
J15	IO100PPB1	M3	IO193NPB3	P7	IO159RSB2
J16	GCA2/IO94PSB1	M4	GEC0/IO190NPB3	P8	IO151RSB2

256-Pin FBGA	
Pin Number	A3P1000 Function
P9	IO137RSB2
P10	IO134RSB2
P11	IO128RSB2
P12	VMV1
P13	TCK
P14	V _{PUMP}
P15	TRST
P16	GDA0/IO113NDB1
R1	GEA1/IO188PDB3
R2	GEA0/IO188NDB3
R3	IO184RSB2
R4	GEC2/IO185RSB2
R5	IO168RSB2
R6	IO163RSB2
R7	IO157RSB2
R8	IO149RSB2
R9	IO143RSB2
R10	IO138RSB2
R11	IO131RSB2
R12	IO125RSB2
R13	GDB2/IO115RSB2
R14	TDI
R15	GNDQ
R16	TDO
T1	GND
T2	IO183RSB2
T3	GEB2/IO186RSB2
T4	IO172RSB2
T5	IO170RSB2
T6	IO164RSB2
T7	IO158RSB2
T8	IO153RSB2
T9	IO142RSB2
T10	IO135RSB2
T11	IO130RSB2
T12	GDC2/IO116RSB2

256-Pin FBGA	
Pin Number	A3P1000 Function
T13	IO120RSB2
T14	GDA2/IO114RSB2
T15	TMS
T16	GND

484-Pin FBGA



Note: This is the bottom view of the package.

Note

For Package Manufacturing and Environmental information, visit the Resource Center at <http://www.actel.com/products/solutions/package/docs.aspx>.

484-Pin FBGA*		484-Pin FBGA*		484-Pin FBGA*	
Pin Number	A3P1000 Function	Pin Number	A3P1000 Function	Pin Number	A3P1000 Function
A1	GND	B15	IO63RSB0	D7	GAB0/IO02RSB0
A2	GND	B16	IO66RSB0	D8	IO16RSB0
A3	V _{CC} B0	B17	IO68RSB0	D9	IO22RSB0
A4	IO07RSB0	B18	IO70RSB0	D10	IO28RSB0
A5	IO09RSB0	B19	NC	D11	IO35RSB0
A6	IO13RSB0	B20	NC	D12	IO45RSB0
A7	IO18RSB0	B21	V _{CC} B1	D13	IO50RSB0
A8	IO20RSB0	B22	GND	D14	IO55RSB0
A9	IO26RSB0	C1	V _{CC} B3	D15	IO61RSB0
A10	IO32RSB0	C2	IO220PDB3	D16	GBB1/IO75RSB0
A11	IO40RSB0	C3	NC	D17	GBA0/IO76RSB0
A12	IO41RSB0	C4	NC	D18	GBA1/IO77RSB0
A13	IO53RSB0	C5	GND	D19	GND
A14	IO59RSB0	C6	IO10RSB0	D20	NC
A15	IO64RSB0	C7	IO14RSB0	D21	NC
A16	IO65RSB0	C8	V _{CC}	D22	NC
A17	IO67RSB0	C9	V _{CC}	E1	IO219NDB3
A18	IO69RSB0	C10	IO30RSB0	E2	NC
A19	NC	C11	IO37RSB0	E3	GND
A20	V _{CC} B0	C12	IO43RSB0	E4	GAB2/IO224PDB3
A21	GND	C13	NC	E5	GAA2/IO225PDB3
A22	GND	C14	V _{CC}	E6	GNDQ
B1	GND	C15	V _{CC}	E7	GAB1/IO03RSB0
B2	V _{CC} B3	C16	NC	E8	IO17RSB0
B3	NC	C17	NC	E9	IO21RSB0
B4	IO06RSB0	C18	GND	E10	IO27RSB0
B5	IO08RSB0	C19	NC	E11	IO34RSB0
B6	IO12RSB0	C20	NC	E12	IO44RSB0
B7	IO15RSB0	C21	NC	E13	IO51RSB0
B8	IO19RSB0	C22	V _{CC} B1	E14	IO57RSB0
B9	IO24RSB0	D1	IO219PDB3	E15	GBC1/IO73RSB0
B10	IO31RSB0	D2	IO220NDB3	E16	GBB0/IO74RSB0
B11	IO39RSB0	D3	NC	E17	IO71RSB0
B12	IO48RSB0	D4	GND	E18	GBA2/IO78PDB1
B13	IO54RSB0	D5	GAA0/IO00RSB0	E19	IO81PDB1
B14	IO58RSB0	D6	GAA1/IO01RSB0	E20	GND

Package Pin Assignments

484-Pin FBGA*		484-Pin FBGA*		484-Pin FBGA*	
Pin Number	A3P1000 Function	Pin Number	A3P1000 Function	Pin Number	A3P1000 Function
E21	NC	G13	IO52RSB0	J5	IO218NDB3
E22	IO84PDB1	G14	IO60RSB0	J6	IO216PDB3
F1	NC	G15	GNDQ	J7	IO216NDB3
F2	IO215PDB3	G16	IO80NDB1	J8	V _{CC} B3
F3	IO215NDB3	G17	GBB2/IO79PDB1	J9	GND
F4	IO224NDB3	G18	IO79NDB1	J10	V _{CC}
F5	IO225NDB3	G19	IO82NPB1	J11	V _{CC}
F6	VMV3	G20	IO85PDB1	J12	V _{CC}
F7	IO11RSB0	G21	IO85NDB1	J13	V _{CC}
F8	GAC0/IO04RSB0	G22	NC	J14	GND
F9	GAC1/IO05RSB0	H1	NC	J15	V _{CC} B1
F10	IO25RSB0	H2	NC	J16	IO83NPB1
F11	IO36RSB0	H3	V _{CC}	J17	IO86NPB1
F12	IO42RSB0	H4	IO217PDB3	J18	IO90PPB1
F13	IO49RSB0	H5	IO218PDB3	J19	IO87NDB1
F14	IO56RSB0	H6	IO221NDB3	J20	NC
F15	GBC0/IO72RSB0	H7	IO221PDB3	J21	IO89PDB1
F16	IO62RSB0	H8	VMV0	J22	IO89NDB1
F17	VMV0	H9	V _{CC} B0	K1	IO211PDB3
F18	IO78NDB1	H10	V _{CC} B0	K2	IO211NDB3
F19	IO81NDB1	H11	IO38RSB0	K3	NC
F20	IO82PPB1	H12	IO47RSB0	K4	IO210PPB3
F21	NC	H13	V _{CC} B0	K5	IO213NDB3
F22	IO84NDB1	H14	V _{CC} B0	K6	IO213PDB3
G1	IO214NDB3	H15	VMV1	K7	GFC1/IO209PPB3
G2	IO214PDB3	H16	GBC2/IO80PDB1	K8	V _{CC} B3
G3	NC	H17	IO83PPB1	K9	V _{CC}
G4	IO222NDB3	H18	IO86PPB1	K10	GND
G5	IO222PDB3	H19	IO87PDB1	K11	GND
G6	GAC2/IO223PDB3	H20	V _{CC}	K12	GND
G7	IO223NDB3	H21	NC	K13	GND
G8	GNDQ	H22	NC	K14	V _{CC}
G9	IO23RSB0	J1	IO212NDB3	K15	V _{CC} B1
G10	IO29RSB0	J2	IO212PDB3	K16	GCC1/IO91PPB1
G11	IO33RSB0	J3	NC	K17	IO90NPB1
G12	IO46RSB0	J4	IO217NDB3	K18	IO88PDB1

484-Pin FBGA*		484-Pin FBGA*		484-Pin FBGA*	
Pin Number	A3P1000 Function	Pin Number	A3P1000 Function	Pin Number	A3P1000 Function
K19	IO88NDB1	M11	GND	P3	IO199NDB3
K20	IO94NPB1	M12	GND	P4	IO202NDB3
K21	IO98NDB1	M13	GND	P5	IO202PDB3
K22	IO98PDB1	M14	V _{CC}	P6	IO196PPB3
L1	NC	M15	GCB2/IO95PPB1	P7	IO193PPB3
L2	IO200PDB3	M16	GCA1/IO93PPB1	P8	V _{CCI} B3
L3	IO210NPB3	M17	GCC2/IO96PPB1	P9	GND
L4	GFB0/IO208NPB3	M18	IO100PPB1	P10	V _{CC}
L5	GFA0/IO207NDB3	M19	GCA2/IO94PPB1	P11	V _{CC}
L6	GFB1/IO208PPB3	M20	IO101PPB1	P12	V _{CC}
L7	V _{COMPLF}	M21	IO99PPB1	P13	V _{CC}
L8	GFC0/IO209NPB3	M22	NC	P14	GND
L9	V _{CC}	N1	IO201NDB3	P15	V _{CCI} B1
L10	GND	N2	IO201PDB3	P16	GDB0/IO112NPB1
L11	GND	N3	NC	P17	IO106NDB1
L12	GND	N4	GFC2/IO204PDB3	P18	IO106PDB1
L13	GND	N5	IO204NDB3	P19	IO107PDB1
L14	V _{CC}	N6	IO203NDB3	P20	NC
L15	GCC0/IO91NPB1	N7	IO203PDB3	P21	IO104PDB1
L16	GCB1/IO92PPB1	N8	V _{CCI} B3	P22	IO103NDB1
L17	GCA0/IO93NPB1	N9	V _{CC}	R1	NC
L18	IO96NPB1	N10	GND	R2	IO197PPB3
L19	GCB0/IO92NPB1	N11	GND	R3	V _{CC}
L20	IO97PDB1	N12	GND	R4	IO197NPB3
L21	IO97NDB1	N13	GND	R5	IO196NPB3
L22	IO99NPB1	N14	V _{CC}	R6	IO193NPB3
M1	NC	N15	V _{CCI} B1	R7	GEC0/IO190NPB3
M2	IO200NDB3	N16	IO95NPB1	R8	VMV3
M3	IO206NDB3	N17	IO100NPB1	R9	V _{CCI} B2
M4	GFA2/IO206PDB3	N18	IO102NDB1	R10	V _{CCI} B2
M5	GFA1/IO207PDB3	N19	IO102PDB1	R11	IO147RSB2
M6	V _{CCPLF}	N20	NC	R12	IO136RSB2
M7	IO205NDB3	N21	IO101NPB1	R13	V _{CCI} B2
M8	GFB2/IO205PDB3	N22	IO103PDB1	R14	V _{CCI} B2
M9	V _{CC}	P1	NC	R15	VMV2
M10	GND	P2	IO199PDB3	R16	IO110NDB1

Package Pin Assignments

484-Pin FBGA*		484-Pin FBGA*		484-Pin FBGA*	
Pin Number	A3P1000 Function	Pin Number	A3P1000 Function	Pin Number	A3P1000 Function
R17	GDB1/IO112PPB1	U9	IO165RSB2	W1	NC
R18	GDC1/IO111PDB1	U10	IO159RSB2	W2	IO191PDB3
R19	IO107NDB1	U11	IO151RSB2	W3	NC
R20	V _{CC}	U12	IO137RSB2	W4	GND
R21	IO104NDB1	U13	IO134RSB2	W5	IO183RSB2
R22	IO105PDB1	U14	IO128RSB2	W6	GEB2/IO186RSB2
T1	IO198PDB3	U15	VMV1	W7	IO172RSB2
T2	IO198NDB3	U16	TCK	W8	IO170RSB2
T3	NC	U17	V _{PUMP}	W9	IO164RSB2
T4	IO194PPB3	U18	TRST	W10	IO158RSB2
T5	IO192PPB3	U19	GDA0/IO113NDB1	W11	IO153RSB2
T6	GEC1/IO190PPB3	U20	NC	W12	IO142RSB2
T7	IO192NPB3	U21	IO108NDB1	W13	IO135RSB2
T8	GNDQ	U22	IO109PDB1	W14	IO130RSB2
T9	GEA2/IO187RSB2	V1	NC	W15	GDC2/IO116RSB2
T10	IO161RSB2	V2	NC	W16	IO120RSB2
T11	IO155RSB2	V3	GND	W17	GDA2/IO114RSB2
T12	IO141RSB2	V4	GEA1/IO188PDB3	W18	TMS
T13	IO129RSB2	V5	GEA0/IO188NDB3	W19	GND
T14	IO124RSB2	V6	IO184RSB2	W20	NC
T15	GNDQ	V7	GEC2/IO185RSB2	W21	NC
T16	IO110PDB1	V8	IO168RSB2	W22	NC
T17	V _{JTAG}	V9	IO163RSB2	Y1	V _{CC} B3
T18	GDC0/IO111NDB1	V10	IO157RSB2	Y2	IO191NDB3
T19	GDA1/IO113PDB1	V11	IO149RSB2	Y3	NC
T20	NC	V12	IO143RSB2	Y4	IO182RSB2
T21	IO108PDB1	V13	IO138RSB2	Y5	GND
T22	IO105NDB1	V14	IO131RSB2	Y6	IO177RSB2
U1	IO195PDB3	V15	IO125RSB2	Y7	IO174RSB2
U2	IO195NDB3	V16	GDB2/IO115RSB2	Y8	V _{CC}
U3	IO194NPB3	V17	TDI	Y9	V _{CC}
U4	GEB1/IO189PDB3	V18	GNDQ	Y10	IO154RSB2
U5	GEB0/IO189NDB3	V19	TDO	Y11	IO148RSB2
U6	VMV2	V20	GND	Y12	IO140RSB2
U7	IO179RSB2	V21	NC	Y13	NC
U8	IO171RSB2	V22	IO109NDB1	Y14	V _{CC}

484-Pin FBGA*		484-Pin FBGA*	
Pin Number	A3P1000 Function	Pin Number	A3P1000 Function
Y15	V _{CC}	AB7	IO167RSB2
Y16	NC	AB8	IO162RSB2
Y17	NC	AB9	IO156RSB2
Y18	GND	AB10	IO150RSB2
Y19	NC	AB11	IO145RSB2
Y20	NC	AB12	IO144RSB2
Y21	NC	AB13	IO132RSB2
Y22	V _{CC} B1	AB14	IO127RSB2
AA1	GND	AB15	IO126RSB2
AA2	V _{CC} B3	AB16	IO123RSB2
AA3	NC	AB17	IO121RSB2
AA4	IO181RSB2	AB18	IO118RSB2
AA5	IO178RSB2	AB19	NC
AA6	IO175RSB2	AB20	V _{CC} B2
AA7	IO169RSB2	AB21	GND
AA8	IO166RSB2	AB22	GND
AA9	IO160RSB2		
AA10	IO152RSB2		
AA11	IO146RSB2		
AA12	IO139RSB2		
AA13	IO133RSB2		
AA14	NC		
AA15	NC		
AA16	IO122RSB2		
AA17	IO119RSB2		
AA18	IO117RSB2		
AA19	NC		
AA20	NC		
AA21	V _{CC} B1		
AA22	GND		
AB1	GND		
AB2	GND		
AB3	V _{CC} B2		
AB4	IO180RSB2		
AB5	IO176RSB2		
AB6	IO173RSB2		

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Datasheet Categories

Categories

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