REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

查询"5962-9857801QXA"供应商

REV																				
SHEET	35	36	37	38	39	40	41	42	43	44	45	46	47							
REV																				
SHEET	15	16	17	18	19	20	21	22	23	24	25	26	27	28	29	30	31	32	33	34

REV STATUS	REV													
OF SHEETS	SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14

PMIC N/A

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DRAWING APPROVAL DATE
00-01-31

REVISION LEVEL

DEFENSE SUPPLY CENTER COLUMBUS
COLUMBUS, OHIO 43216

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

MICROCIRCUIT, DIGITAL, DIGITAL SIGNAL PROCESSORS, MONOLITHIC SILICON

SIZE	CAGE CODE	
A	67268	5962-98578

SHEET 1 OF 47

DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

1. SCOPE

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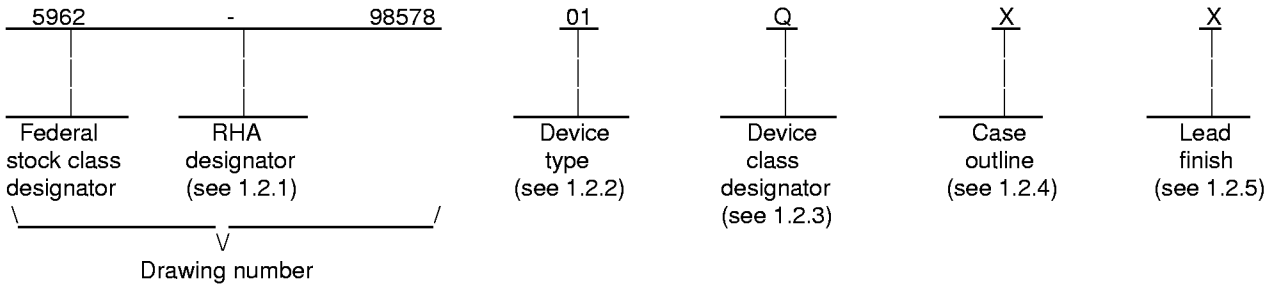
1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:



1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

Device type	Generic number	Circuit function
01	320C6201B	Digital signal processors

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

Device class	Device requirements documentation
M	Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A
Q or V	Certification and qualification to MIL-PRF-38535

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	See figure 1	429	Ball grid array

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

1.3 Absolute maximum ratings. 1/ 2/

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Supply voltage range (CV_{DD})	-0.3 V dc to +2.3 V dc
Supply voltage range (DV_{DD})	-0.3 V dc to +4.0 V dc
Input voltage range (V_{IN})	-0.3 V dc to +4.0 V dc
Output voltage range (V_{OUT})	-0.3 V dc to +4.0 V dc
Storage temperature range	-55°C to +150°C
Maximum junction temperature (T_J)	+119°C at 150 MHz
Thermal resistance, junction-to-case (θ_{JC})	3.00°C/W
Solder ball reflow condition (Peak temperature)	+220°C ±10°C

1.4 Recommended operating conditions.

Supply voltage range (CV_{DD})	+1.71 V dc to +1.89 V dc
Supply voltage range (DV_{DD})	+3.14 V dc to +3.46 V dc
Supply ground (V_{SS})	+0.0 V dc to +0.0 V dc
High level input voltage (V_{IH})	2.0 V
Low level input voltage (V_{IL})	0.8 V
High level output current (I_{OH})	-12 mA
Low level output current (I_{OL})	12 mA
Case operating temperature range (T_C)	-55°C to +115°C

1.5 Digital logic testing for device classes N, Q, and V.

Fault coverage measurement of manufacturing logic tests (MIL-STD-883, test method 5012)	XX percent 3/

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

DEPARTMENT OF DEFENSE

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

DEPARTMENT OF DEFENSE

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-973 - Configuration Management.
MIL-STD-1835 - Interface Standard For Microcircuit Case Outlines.

HANDBOOKS

DEPARTMENT OF DEFENSE

MIL-HDBK-103 - List of Standard Microcircuit Drawings (SMD's).
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, and handbooks are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2/ All voltage values are with respect to V_{SS}.
3/ Values will be added when they become available.

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

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3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Case outline. The case outline shall be in accordance with 1.2.4 herein and figure 1.

3.2.2 Terminal connections. The terminal connections shall be as specified on figure 2.

3.2.3 Block diagram. The block diagram shall be as specified on figure 3.

3.2.4 Timing waveforms. The timing waveforms shall be as specified on figure 4.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-HDBK-103. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DSCC-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-973.

3.9 Verification and review for device class M. For device class M, DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 105 (see MIL-PRF-38535, appendix A).

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TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions $-55°C \le T_C \le +115°C$ unless otherwise specified 1/	Group A subgroups	Device type	Limits		Unit
					Min	Max	
Low level output voltage	V_{OL} 2/	DV_{DD} = 3.14 V I_{OL} = 12 mA	1, 2, 3	All		0.6	V
High level output voltage	V_{OH} 2/	DV_{DD} = 3.14 V I_{OH} = -12 mA	1, 2, 3	All	2.4		V
Input current	I_{IN} 3/ 2/	V_{IN} = V_{SS} to DV_{DD}	1, 2, 3	All		±10	µA
OFF- state output leakage current	I_{OZH} I_{OZL} 2/	V_{OUT} = DV_{DD} or 0 V	1, 2, 3	All		±10	µA
Input capacitance	C_{IN}	f = 1 MHz at 0 V See 4.4.1b	4	All	10	15	pF
Output capacitance	C_{OUT}	f = 1 MHz at 0 V See 4.4.1b	4	All	10	15	pF
Functional tests	2/	CV_{DD} = 1.71 V to 1.89 V DV_{DD} = 3.14 V to 3.46 V See 4.4.1c	7,8	All			

See footnotes at end of table.

TABLE I. Electrical performance characteristics. - Continued

查询"5962-9857801QXA"供应商

Test	Symbol	Conditions -55°C ≤ T_C ≤+115°C unless otherwise specified 1/		Group A subgroups	Device type	Limits Min	Limits Max	Unit
CLKIN TIMINGS								
Cycle time, CLKIN	1	See figure 4	CLKMODE=x4	9, 10, 11	All	26.7		ns
			CLKMODE=x1			6.67 4/		ns
Pulse duration, CLKIN high	2		CLKMODE=x4	9, 10, 11	All	9.8		ns
			CLKMODE=x1			2.7		ns
Pulse duration, CLKIN low	3		CLKMODE=x4	9, 10, 11	All	9.8		ns
			CLKMODE=x1			2.7		ns
Transition time, CLKIN	4		CLKMODE=x4	9, 10, 11	All		5	ns
			CLKMODE=x1				0.6	ns
CLKOUT1 TIMINGS 4/ 5/								
Cycle time, CLKOUT1	1	See figure 4	CLKMODE=x4	9, 10, 11	All	P – 0.7	P + 0.7	ns
			CLKMODE=x1			P – 0.7	P + 0.7	ns
Pulse duration, CLKOUT1 high	2		CLKMODE=x4	9, 10 ,11	All	(P/2) - 0.5	(P/2) + 0.5	ns
			CLKMODE=x1			PH - 0.5	PH + 0.5	ns
Pulse duration, CLKOUT1 low	3		CLKMODE=x4	9, 10, 11	All	(P/2) - 0.5	(P/2) + 0.5	ns
			CLKMODE=x1			PL - 0.5	PL + 0.5	ns
Transition time, CLKOUT1	4		CLKMODE=x4	9, 10, 11	All		0.6	ns
			CLKMODE=x1				0.6	ns
CLKOUT2 TIMINGS 5/								
Cycle time, CLKOUT2	1	See figure 4		9, 10, 11	All	2P - 0.7	2P + 0.7	ns
Pulse duration, CLKOUT2 high	2			9, 10, 11	All	P – 0.9	P + 0.7	ns
Pulse duration, CLKOUT2 low	3			9, 10, 11	All	P – 0.7	P + 0.9	ns
Transition time, CLKOUT2	4			9, 10, 11	All		0.6	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics. - Continued

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Test	Symbol	Conditions -55°C ≤ T_C ≤+115°C unless otherwise specified 1/	Group A Subgroups	Device Type	Limits Min	Limits Max	Unit
SSCLK, SDCLK, and CLKOUT2 to CLKOUT1 5/							
Delay time, CLKOUT1 edge to SSCLK edge	1 2/	See figure 4	9, 10, 11	All	(P/2) + 0.2	(P/2) + 4.2	ns
Delay time, CLKOUT1 edge to SSCLK edge (1/2 clockrate)	2 2/		9, 10, 11	All	(P/2) - 1.0	(P/2) + 2.4	ns
Delay time, CLKOUT1 edge to CLKOUT2 edge	3		9, 10, 11	All	(P/2) - 1.0	(P/2) + 2.4	ns
Delay time, CLKOUT1 edge to SDCLK edge	4 2/		9, 10, 11	All	(P/2) - 1.0	(P/2) + 2.4	ns
ASYNCHRONOUS MEMORY READ and WRITE TIMING 6/ 7/							
Delay time, CLKOUT1 high to CEx valid	1 2/	See figure 4	9, 10, 11	All	-0.2	4.0	ns
Delay time, CLKOUT1 high to BEx valid	2 2/		9, 10, 11	All		4.0	ns
Delay time, CLKOUT1 high to BEx invalid	3		9, 10, 11	All	-0.2		ns
Delay time, CLKOUT1 high to EAx valid	4 2/		9, 10, 11	All		4.0	ns
Delay time, CLKOUT1 high to EAx invalid	5		9, 10, 11	All	-0.2		ns
Setup time, read EDx valid before CLKOUT1 high	6 2/		9, 10, 11	All	4.0		ns
Hold time, read EDx valid after CLKOUT1 high	7 2/		9, 10, 11	All	0.8		ns
Delay time, CLKOUT1 high to $\overline{AOE}$ valid	8 2/		9, 10, 11	All	-0.2	4.0	ns
Delay time, CLKOUT1 high to $\overline{ARE}$ valid	9 2/		9, 10, 11	All	-0.2	4.0	ns
Setup time, ARDY valid before CLKOUT1 high	10 2/		9, 10, 11	All	3.0		ns
Hold time, ARDY valid after CLKOUT1 high	11 2/		9, 10, 11	All	1.8		ns
Delay time, CLKOUT1 high to EDx valid	12 2/		9, 10, 11	All		4.0	ns
Delay time, CLKOUT1 high to EDx invalid	13		9, 10, 11	All	-0.2		ns
Delay time, CLKOUT1 high to AWE valid	14 2/		9, 10, 11	All	-0.2	4.0	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics. - Continued

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Test	Symbol	Conditions -55°C ≤ T_C ≤+115°C unless otherwise specified 1/	Group A subgroups	Device type	Limits Min	Limits Max	Unit
SBSRAM READ and WRITE TIMING (Full-Rate SSCLK) 8/							
Output setup time, $\overline{CEx}$ valid before SSCLK high	1 2/	See figure 4	9, 10, 11	All	0.5P-1.3		ns
Output hold time, $\overline{CEx}$ valid after SSCLK high	2 2/		9, 10, 11	All	0.5P-2.3		ns
Output setup time, $\overline{BEx}$ valid before SSCLK high	3 2/		9, 10, 11	All	0.5P-1.3		ns
Output hold time, $\overline{BEx}$ invalid after SSCLK high	4		9, 10, 11	All	0.5P-2.3		ns
Output setup time, EAx valid before SSCLK high	5 2/		9, 10, 11	All	0.5P-1.3		ns
Output hold time, EAx invalid after SSCLK high	6		9, 10, 11	All	0.5P-2.3		ns
Setup time, read EDx valid before SSCLK high	7 2/		9, 10, 11	All	1.7		ns
Hold time, read EDx valid after SSCLK high	8 2/		9, 10, 11	All	1.5		ns
Output setup time, $\overline{SSADS}$ valid before SSCLK high	9 2/		9, 10, 11	All	0.5P-1.3		ns
Output hold time, $\overline{SSADS}$ valid after SSCLK high	10 2/		9, 10, 11	All	0.5P-2.3		ns
Output setup time, $\overline{SSOE}$ valid before SSCLK high	11 2/		9, 10, 11	All	0.5P-1.3		ns
Output hold time, $\overline{SSOE}$ valid after SSCLK high	12 2/		9, 10, 11	All	0.5P-2.3		ns
Output setup time, EDx valid before SSCLK high	13 2/		9, 10, 11	All	0.5P-1.3		ns
Output hold time, EDx invalid after SSCLK high	14		9, 10, 11	All	0.5P-2.3		ns
Output setup time, $\overline{SSWE}$ valid before SSCLK high	15 2/		9, 10, 11	All	0.5P-1.3		ns
Output hold time, $\overline{SSWE}$ valid after SSCLK high	16 2/		9, 10, 11	All	0.5P-2.3		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics. - Continued

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Test	Symbol	Conditions -55°C ≤ T_C ≤+115°C unless otherwise specified 1/	Group A subgroups	Device type	Limits Min	Limits Max	Unit
SBSRAM READ and WRITE TIMING (Half-Rate SSCLK) 9/							
Output setup time, $\overline{CEx}$ valid before SSCLK high	1 2/	See figure 4	9, 10, 11	All	1.5P-3.0		ns
Output hold time, $\overline{CEx}$ valid after SSCLK high	2 2/		9, 10, 11	All	0.5P-1.5		ns
Output setup time, $\overline{BEx}$ valid before SSCLK high	3 2/		9, 10, 11	All	1.5P-3.0		ns
Output hold time, $\overline{BEx}$ invalid after SSCLK high	4		9, 10, 11	All	0.5P-1.5		ns
Output setup time, EAx valid before SSCLK high	5 2/		9, 10, 11	All	1.5P-3.0		ns
Output hold time, EAx invalid after SSCLK high	6		9, 10, 11	All	0.5P-1.5		ns
Setup time, read EDx valid before SSCLK high	7 2/		9, 10, 11	All	2.5		ns
Hold time, read EDx valid after SSCLK high	8 2/		9, 10, 11	All	1.5		ns
Output setup time, $\overline{SSADS}$ valid before SSCLK high	9 2/		9, 10, 11	All	1.5P-3.0		ns
Output hold time, $\overline{SSADS}$ valid after SSCLK high	10 2/		9, 10,11	All	0.5P-1.5		ns
Output setup time, $\overline{SSOE}$ valid before SSCLK high	11 2/		9,10, 11	All	1.5P-3.0		ns
Output hold time, $\overline{SSOE}$ valid after SSCLK high	12 2/		9, 10, 11	All	0.5P-1.5		ns
Output setup time, EDx valid before SSCLK high	13 2/		9, 10, 11	All	1.5P-3.0		ns
Output hold time, EDx invalid after SSCLK high	14		9, 10, 11	All	0.5P-1.5		ns
Output setup time, $\overline{SSWE}$ valid before SSCLK high	15 2/		9, 10, 11	All	1.5P-3.0		ns
Output hold time, $\overline{SSWE}$ valid after SSCLK high	16 2/		9, 10, 11	All	0.5P-1.5		ns

See footnote at end of table.

TABLE I. Electrical performance characteristics. - Continued

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Test	Symbol	Conditions -55°C ≤ T_C ≤+115°C unless otherwise specified 1/	Group A subgroups	Device type	Limits Min	Limits Max	Unit
SYNCHRONOUS DRAM TIMING 9/							
Output setup time, $\overline{CEx}$ valid before SDCLK high	1 2/	See figure 4	9, 10, 11	All	1.5P-3.5		ns
Output hold time, $\overline{CEx}$ valid after SDCLK high	2 2/		9, 10, 11	All	0.5P-1.0		ns
Output setup time $\overline{BEx}$ valid before SDCLK high	3 2/		9, 10, 11	All	1.5P-3.5		ns
Output hold time, $\overline{BEx}$ invalid after SDCLK high	4		9, 10, 11	All	0.5P-1.0		ns
Output setup time, EAx valid before SDCLK high	5 2/		9, 10, 11	All	1.5P-3.5		ns
Output hold time, EAx invalid after SDCLK high	6		9, 10, 11	All	0.5P-1.0		ns
Setup time, read EDx valid before SDCLK high	7 2/		9, 10, 11	All	0.5		ns
Hold time, read EDx valid after SDCLK high	8 2/		9, 10, 11	All	3.0		ns
Output setup time, $\overline{SDCAS}$ valid before SDCLK high	9 2/		9, 10, 11	All	1.5P-3.5		ns
Output hold time, $\overline{SDCAS}$ valid after SDCLK high	10 2/		9, 10, 11	All	0.5P-1.0		ns
Output setup time, EDx valid before SDCLK high	11 2/		9, 10, 11	All	1.5P-3.5		ns
Output hold time, EDx invalid after SDCLK high	12		9, 10, 11	All	0.5P-1.0		ns
Output setup time, $\overline{SDWE}$ valid before SDCLK high	13 2/		9, 10, 11	All	1.5P-3.5		ns
Output hold time, $\overline{SDWE}$ valid after SDCLK high	14 2/		9, 10, 11	All	0.5P-1.0		ns
Output setup time, SDA10 valid before SDCLK high	15 2/		9, 10, 11	All	1.5P-3.5		ns
Output hold time, SDA10 invalid after SDCLK high	16		9, 10, 11	All	0.5P-1.0		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics. - Continued

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Test	Symbol	Conditions -55°C ≤ T_C ≤+125°C unless otherwise specified 1/	Group A subgroups	Device type	Limits Min	Limits Max	Unit
SYNCHRONOUS DRAM TIMING-Continued 9/							
Output setup time, $\overline{SDRAS}$ valid before SDCLK high	17 2/	See figure 4	9, 10, 11	All	1.5P-3.5		ns
Output hold time, $\overline{SDRAS}$ valid after SDCLK high	18 2/		9, 10, 11	All	0.5P-1.0		ns
$\overline{HOLD}$/$\overline{HOLDA}$ TIMING 10/ 11/							
Setup time, $\overline{HOLD}$ high before CLKOUT1 high	1	See figure 4	9, 10, 11	All	1.0		ns
Hold time, $\overline{HOLD}$ low after CLKOUT1 high	2		9, 10, 11	All	4.0		ns
Response time, $\overline{HOLD}$ low to EMIF Bus high impedance	3		9, 10, 11	All	4P		ns
Response time, EMIF Bus high impedance to $\overline{HOLDA}$ low	4		9, 10, 11	All	P	2P	ns
Response time, $\overline{HOLD}$ high to $\overline{HOLDA}$ high	5		9, 10, 11	All	4P	7P	ns
Delay time, CLKOUT1 high to $\overline{HOLDA}$ valid	6		9, 10, 11	All	1.0	4/ 8.0	ns
Delay time, CLKOUT1 high to EMIF Bus high impedance	7		9, 10, 11	All	3.0	11.0	ns
Delay time, CLKOUT1 high to EMIF Bus low impedance	8		9, 10, 11	All	3.0	11.0	ns
Response time, $\overline{HOLD}$ high to EMIF Bus low impedance	9		9, 10, 11	All	3P	6P	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics. - Continued

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Test	Symbol	Conditions -55°C ≤ T_C ≤+115°C unless otherwise specified 1/	Group A subgroups	Device type	Limits Min	Limits Max	Unit
RESET TIMING							
Width of the $\overline{\text{RESET}}$ pulse (PLL stable) 12/	1	See figure 4	9, 10, 11	All	10		CLKOUT1 cycles
Width of the $\overline{\text{RESET}}$ pulse (PLL needs to sync up) 2/ 13/					250		µs
Response time to change of value in $\overline{\text{RESET}}$ signal	2 2/		9, 10, 11	All	2		CLKOUT1 cycles
Delay time, CLKOUT1 high to CLKOUT2 invalid	3		9, 10, 11	All	-1.0		ns
Delay time, CLKOUT1 high to CLKOUT2 valid	4 2/		9, 10, 11	All		10	ns
Delay time, CLKOUT1 high to SDCLK invalid	5		9, 10, 11	All	-1.0		ns
Delay time, CLKOUT1 high to SDCLK valid	6 2/		9, 10, 11	All		10	ns
Delay time, CLKOUT1 high to SSCLK invalid	7		9, 10, 11	All	-1.0		ns
Delay time, CLKOUT1 high to SSCLK valid	8 2/		9, 10, 11	All		10	ns
Delay time, CLKOUT1 high to low group invalid	9		9, 10, 11	All	-1.0		ns
Delay time, CLKOUT1 high to low group valid	10		9, 10, 11	All		10	ns
Delay time, CLKOUT1 high to high group invalid	11		9, 10, 11	All	-1.0		ns
Delay time, CLKOUT1 high to high group valid	12		9, 10, 11	All		10	ns
Delay time, CLKOUT1 high to Z group high impedance	13		9, 10, 11	All	-1.0		ns
Delay time, CLKOUT1 high to Z group valid	14		9, 10, 11	All		10	ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics. - Continued

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Test	Symbol	Conditions -55°C ≤ T_C ≤+115°C unless otherwise specified 1/	Group A subgroups	Device type	Limits Min	Limits Max	Unit
INTERRUPT TIMING 14/ 15/ 16/							
Response time, EXT_INTx high to IACK high	1	See figure 4	9, 10, 11	All	9P		ns
Width of the interrupt pulse low	2		9, 10, 11	All	2P		ns
Width of the interrupt pulse high	3		9, 10, 11	All	2P		ns
Delay time, CLKOUT2 low to IACK valid.	4		9, 10, 11	All	-4.0	6.0 4/	ns
Delay time, CLKOUT2 low to INUMx valid	5 2/		9, 10, 11	All		6.0	ns
Delay time, CLKOUT2 low to INUMx invalid	6		9, 10, 11	All	-4.0		ns
HOST-PORT INTERFACE (HPI) READ and WRITE TIMING 17/ 18/ 19/ 20/ 21/							
Setup time, select signals valid before HSTROBE low	1 2/	See figure 4	9, 10, 11	All	4.0		
Hold time, select signals valid after HSTROBE low	2 2/		9, 10, 11	All	2.0		
Pulse duration $\overline{\text{HSTROBE}}$ low	3 2/		9, 10, 11	All	2P		
Pulse duration $\overline{\text{HSTROBE}}$ high between consecutive accesses	4		9, 10, 11	All	2P		
Delay time, $\overline{\text{HCS}}$ to $\overline{\text{HRDY}}$	5		9, 10, 11	All	1.0	4/ 9.0	
Delay time, $\overline{\text{HSTROBE}}$ low to HRDY high	6		9, 10, 11	All	3.0	4/ 12.0	
Output hold time, HD low impedance after HSTROBE low for an HPI read	7		9, 10, 11	All	4.0		
Delay time, HD valid HRDY low	8		9, 10, 11	All	P-3	P+3	
Output hold time, HD valid after HSTROBE high	9		9, 10, 11	All	1.0	12.0	
Setup time, select signals valid before HAS low	10 2/		9, 10, 11	All	4.0		

See footnotes at end of table.

TABLE I. Electrical performance characteristics. - Continued

查询"5962-9857801QXA"供应商

Test	Symbol	Conditions -55°C ≤ T_C ≤+115°C unless otherwise specified 1/	Group A subgroups	Device type	Limits Min	Limits Max	Unit
HOST-PORT INTERFACE (HPI) READ and WRITE TIMING 17/ 18/ 19/ 20/ 21/ – Continued							
Hold time, select signals valid after HAS low	11 2/	See figure 4	9, 10, 11	All	2.0		ns
Setup time, host data valid before HSTROBE high	12 2/		9, 10, 11	All	4.0		ns
Hold time, host data valid after HSTROBE high	13 2/		9, 10, 11	All	2.0		ns
Hold time, $\overline{\text{HSTROBE}}$ low after HRDY low. HSTROBE should not be inactivated until HRDY is active (low): otherwise, HPI writes will not complete properly.	14		9, 10, 11	All	1.0		ns
Delay time, $\overline{\text{HSTROBE}}$ high to HD high impedance	15		9, 10, 11	All	3.0	12.0	ns
Delay time, $\overline{\text{HSTROBE}}$ low to HD valid	16		9, 10, 11	All	2.0	12.0	ns
Delay time, $\overline{\text{HSTROBE}}$ high to HRDY high	17		9, 10, 11	All	3.0	4/ 12.0	ns
Setup time, $\overline{\text{HAS}}$ low before HSTROBE low	18		9, 10, 11	All	2.0		ns
Hold time, $\overline{\text{HAS}}$ low after HSTROBE low	19		9, 10, 11	All	2.0		ns

See footnotes at end of table.

TABLE I. Electrical performance characteristics. - Continued

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Test	Symbol	Conditions -55°C ≤ T_C ≤+115°C unless otherwise specified 1/		Group A subgroups	Device type	Limits Min	Limits Max	Unit
MULTICHANNEL BUFFERED SERIAL PORT (McBSP) TIMING 22/ 23/								
Delay time, CLKS high to CLKR/X high for internal CLKR/X generated from CLKS input	1 2/	See figure 4		9, 10, 11	All	3.0	10.0	ns
Cycle time, CLKR/X	2 2/		CLKR/X (INT)	9, 10, 11	All	2P		ns
			CLKR/X (EXT)			2P		
Pulse duration, CLKR/X high or CLKR/X low	3		CLKR/X (INT)	9, 10, 11	All	C-1.6	C+1	ns
			CLKR/X (EXT)			P-1		
Delay time, CLKR high to internal FSR valid	4		CLKR (INT)	9, 10, 11	All	-2.5	3.0 4/	ns
Setup time, external FSR high before CLKR low	5 2/		CLKR (INT)	9, 10, 11	All	9.0		ns
			CLKR (EXT)			2.0		
Hold time, external FSR high after CLKR low	6 2/		CLKR (INT)	9, 10, 11	All	6.0		ns
			CLKR (EXT)			3.0		
Setup time, DR valid before CLKR low	7 2/		CLKR (INT)	9, 10, 11	All	8.0		ns
			CLKR (EXT)			1.0		
Hold time, DR valid after CLKR low	8 2/		CLKR (INT)	9, 10, 11	All	3.0		ns
			CLKR (EXT)			4.0		
Delay time, CLKX high to internal FSX valid	9 2/		CLKX (INT)	9, 10, 11	All	-2.0	3.0 4/	ns
			CLKX (EXT)			3.0	9.0	
Setup time, external FSX high before CLKX low	10 2/		CLKX (INT)	9, 10, 11	All	9.0		ns
			CLKX (EXT)			2.0		
Hold time external FSX high after CLKX low	11 2/		CLKX (INT)	9, 10, 11	All	6.0		ns
			CLKX (EXT)			3.0		
Disable time, DX high impedance following last data bit from CLKX high	12		CLKX (INT)	9, 10, 11	All	-1.0	4.0	ns
			CLKX (EXT)			3.0	9.0	
Delay time, CLKX high to DX valid	13		CLKX (INT)	9, 10, 11	All	-1.0	4.0	ns
			CLKX (EXT)			3.0	9.0	
Delay time, FSX high to DX valid ONLY applies when in data delay 0 (XDATDLY = 00b) mode	14		FSX (INT)	9, 10, 11	All	-1.0	3.0	ns
			FSX (EXT)			3.0	9.0	

TABLE I. Electrical performance characteristics. - Continued

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Test	Symbol	Conditions -55°C ≤ T_C ≤+115°C unless otherwise specified 1/		Group A subgroups	Device type	Limits Min	Limits Max	Unit
FSR TIMING When GSYNC = 1								
Setup time, FSR high before CLKS high	1 2/	See figure 4		9, 10, 11	All	4.0		ns
Hold time, FSR high after CLKS high	2 2/			9, 10, 11	All	4.0		ns
McBSP TIMING as SPI MASTER or SLAVE: CLKSTP = 10b, CLKXP = 0 24/								
Hold time, FSX low after CLKX low	1 25/	See figure 4	Master 27/	9, 10, 11	All	T-2 4/	T+3	ns
			Slave					
Delay time, FSX low to CLKX high	2 26/		Master 27/	9, 10, 11	All	L-2	L+3 2/	ns
			Slave					
Delay time, CLKX high to DX valid	3		Master 27/	9, 10, 11	All	-2.0	4.0 2/	ns
			Slave			3P+4	5P+17 2/	
Setup time, DR valid before CLKX low	4 2/		Master	9, 10, 11	All	12.0		ns
			Slave			2-3P		
Hold time, DR valid after CLKX low	5 2/		Master	9, 10, 11	All	4.0		ns
			Slave			5+6P		
Disable time, DX high impedance following last data bit from CLKX low	6		Master 27/	9, 10, 11	All	L-2	L+3	ns
			Slave					
Disable time, DX high impedance following last data bit from FSX high	7		Master 27/	9, 10, 11	All			ns
			Slave			P+3	3P+17	
Delay time, FSX low to DX valid	8		Master 27/	9, 10, 11	All			ns
			Slave			2P+2	4P+17 2/	

See footnotes at end of table.

TABLE I. Electrical performance characteristics. - Continued

查询"5962-9857801QXA"供应商

Test	Symbol	Conditions -55°C ≤ T_C ≤+115°C unless otherwise specified 1/		Group A subgroups	Device type	Limits		Unit
						Min	Max	
McBSP TIMING as SPI MASTER or SLAVE: CLKSTP = 11b, CLKXP = 0 24/								
Hold time, FSX low after CLKX low	1 25/	See figure 4	Master 27/	9, 10, 11	All	L-2 4/	L+3	ns
			Slave					
Delay time, FSX low to CLKX high	2 26/		Master 27/	9, 10, 11	All	T-2	T+3 2/	ns
			Slave					
Delay time, CLKX low to DX valid	3		Master 27/	9, 10, 11	All	-2.0	4.0	ns
			Slave			3P+4	5P+17 2/	
Setup time, DR valid before CLKX high	4 2/		Master	9, 10, 11	All	12.0		ns
			Slave			2-3P		
Hold time, DR valid after CLKX high	5 2/		Master	9, 10, 11	All	4.0		ns
			Slave			5+6P		
Disable time, DX high impedance following last data bit from CLKX low	6		Master 27/	9, 10, 11	All	2.0	4.0	ns
			Slave			3P+3	5P+17	
Delay time, FSX low to DX valid	7		Master 27/	9, 10, 11	All	H-2	H+4 2/	ns
			Slave			2P+2	4P+17 2/	
McBSP TIMING as SPI MASTER or SLAVE: CLKSTP = 10b, CLKXP = 1 24/								
Hold time, FSX low after CLKX high	1 25/	See figure 4	Master 27/	9, 10, 11	All	T-2 4/	T+3	ns
			Slave					
Delay time, FSX low to CLKX low	2 26/		Master 27/	9, 10, 11	All	H-2	H+3 2/	ns
			Slave					
Delay time, CLKX low to DX valid	3		Master 27/	9, 10, 11	All	-2.0	4.0 2/	ns
			Slave			3P+4	5P+17 4/	
Setup time, DR valid before CLKX high	4 2/		Master	9, 10, 11	All	12.0		ns
			Slave			2-3P		
Hold time, DR valid after CLKX high	5 2/		Master	9, 10, 11	All	4.0		ns
			Slave			5+6P		
Disable time, DX high impedance following last data bit from CLKX high	6		Master 27/	9, 10, 11	All	H-2	H+3	ns
			Slave					
Disable time, DX high impedance following last data bit from FSX high	7		Master 27/	9, 10, 11	All			ns
			Slave			P+3	3P+17	
Delay time, FSX low to DX valid	8		Master 27/	9, 10, 11	All			ns
			Slave			2P+2	4P+17 2/	

See footnotes at end of table.

TABLE I. Electrical performance characteristics. - Continued

查询"5962-9857801QXA"供应商

Test	Symbol	Conditions -55°C ≤ T_C ≤+115°C unless otherwise specified 1/		Group A subgroups	Device type	Limits Min	Limits Max	Unit
McBSP TIMING as SPI MASTER or SLAVE: CLKSTP = 11b, CLKXP = 1 24/								
Hold time, FSX low after CLKX high	1 25/	See figure 4	Master 27/	9, 10, 11	All	H-2 4/	H+3	ns
			Slave					
Delay time, FSX low to CLKX low	2 26/		Master 27/	9, 10, 11	All	T-2	T+1 2/	ns
			Slave					
Delay time, CLKX high to DX valid	3		Master 27/	9, 10, 11	All	-2.0	4.0 2/	ns
			Slave			3P+3 4/	5P+17	
Setup time, DR valid before CLKX low	4 2/		Master	9, 10, 11	All	12.0		ns
			Slave			2-3P		
Hold time, DR valid after CLKX low	5 2/		Master	9, 10, 11	All	4.0		ns
			Slave			5+6P		
Disable time, DX high impedance following last data bit from CLKX high	6		Master 27/	9, 10, 11	All	-2.0	4.0	ns
			Slave			3P+3	5P+17	
Delay time, FSX low to DX valid	7		Master 27/	9, 10, 11	All	L-2	L+4 2/	ns
			Slave			2P+2	4P+17 2/	
DMAC TIMING								
Delay time, CLKOUT1 high to DMAC valid	1	See figure 4		9, 10, 11	All	2.0	10.0 2/	ns
TIMER TIMING								
Pulse duration, TINP high or low	1	See figure 4		9, 10, 11	All	2P		ns
Delay time, CLKOUT1 high to TOUT valid	2			9, 10, 11	All	2.0	9.0 2/	ns
POWER-DOWN TIMING								
Delay time, CLKOUT1 high to PD valid	1	See figure 4		9, 10, 11	All	2.0	9.0 2/	ns
JTAG TEST-PORT TIMING								
Cycle time, TCK	1	See figure 4		9, 10, 11	All	50		ns
Delay time, TCK low to TDO valid	2			9, 10, 11	All	0	15.0	ns
Setup time, TDI/TMS/ TRST valid before TCK high	3			9, 10, 11	All	10.0		ns
Hold time, TDI/TMS/ TRST valid after TCK high	4			9, 10, 11	All	5.0		ns

See footnotes on next page.

TABLE I. Electrical performance characteristics. – Continued

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1/ Each input/output, as applicable, shall be tested at the specified temperature, for the specified limits, to the tests in table I herein. Output terminals not designated shall be high level logic, low level logic, or open.

2/ Tested parameters.

3/ TMS and TDI are not included due to internal pullups.

4/ PH is the high period of CLKIN in ns and PL is the low period of CLKIN in ns.

5/ P = 1/CPU clock frequency in ns. When running parts at 150 MHz, use P = 6.67 ns.

6/ To ensure data setup time, simply program the strobe width wide enough. ARDY is internally synchronized. If ARDY does meet setup or hold time, it may be recognized in the current cycle or the next cycle. Thus, ARDY can be an asynchronous input.

7/ The minimum delay is also the minimum output hold after CLKOUT1 high.

8/ When the PLL is used (CLKMODEx4), P = 1/CPU clock frequency, when running parts at 150 MHz, use P = 6.67 ns. For CLKMODEx1, 0.5P is defined as PH (pulse duration of CLKIN high) for all output setup times; 0.5P is defined as PL (pulse duration of CLKIN low) for all output hold times.

9/ For CLKMODEx1:
1.5P = P + PH, where P=1/CPU clock frequency, and PH = pulse duration of CLKIN high.
0.5P = PL, where PL = pulse duration of CLKIN low.

10/ $\overline{\text{HOLD}}$ is synchronized internally. If setup and hold times are not met, it will either be recognized in the current cycle or in the next cycle. $\overline{\text{HOLD}}$ can be an asynchronous input.

11/ All pending EMIF transactions are allowed to complete before $\overline{\text{HOLDA}}$ is asserted. The worst cases for this is an asynchronous read or write with external ARDY used or a minimum of eight consecutive SDRAM reads or writes when RBTR8 = 1. If no bus transactions are occurring, then the minimum delay time can be achieved. The bus hold can be indefinitely delayed by setting NOHOLD = 1.

12/ This parameter applies to CLKMODEx1 when CLKIN is stable and applies to CLKMODEx4 when CLKIN and PLL are stable.

13/ This parameter only applies to CLKMODEx4. The $\overline{\text{RESET}}$ signal is not connected internally to the clock PLL circuit. The PLL, however, may need up to 250 µs to stabilize following device power up or after PLL configuration has been changed. During that time, $\overline{\text{RESET}}$ must be asserted to ensure proper device operation.

14/ Interrupt signals are synchronized internally and are potentially recognized one cycle later if setup and hold time are violated. Also they can be connected to asynchronous inputs.

15/ When the PLL is used (CLKMODEx4), 0.5P = 1/(2x CPU clock frequency).

16/ For CLKMODEx1:0.5P = PH, where PH is the high period of CLKIN.

17/ $\overline{\text{HSTROBE}}$ refers to the following logical operation on $\overline{\text{HCS}}$, $\overline{\text{HDS1}}$, and $\overline{\text{HDS2}}$: [NOT($\overline{\text{HDS1}}$ XOR $\overline{\text{HDS2}}$)] OR $\overline{\text{HCS}}$.

18/ $\overline{\text{HCS}}$ enables $\overline{\text{HRDY}}$, and $\overline{\text{HRDY}}$ is always low when $\overline{\text{HCS}}$ is high. The case where $\overline{\text{HRDY}}$ goes high when $\overline{\text{HCS}}$ falls indicates that HPI is busy completing a previous HPID WRITE or READ autoincrement.

19/ The effects of internal clock jitter are included at test. There is no need to adjust timing numbers for internal clock jitter.

20/ This parameter is used during an HPID read. At the beginning of the first half -word transfer on the falling edge of $\overline{\text{HSTROBE}}$, the HPI sends the request to the DMA auxiliary channel, and $\overline{\text{HRDY}}$ remains high until the DMA auxiliary channel loads the requested data into HPID.

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21/ This parameter is used after the second half-word of an HPID write autoincrement read. $\overline{HRDY}$ remains low if the access is not an HPID write or autoincrement read. Reading or writing to HPIC or HPIA does not affect the $\overline{HRDY}$ signal.

22/ CLKRP = CLKXP =FSRP = FSXP = 0. If polarity of any of the signals is inverted, then the timing references of that signal are also inverted.

23/ Minimum delay times also represent minimum output hold times.

24/ For all SPI slave modes, CLKG is programmed as 1/2 of the CPU clock by setting CLKSM = CLKGDV = 1.

25/ FSRP = FSXP = 1. As a SPI master, FSX is inverted to provide active-low slave enable output. As a slave, the active-low signal input on FSX and FSR is inverted before being used internally.
CLKXM = FSXM = 1, CLKRM = FSRM = 0 for master McBSP.
CLKXM = CLKRM = FSXM = FSRM = 0 for slave McBSP.

26/ FSX should be low before the rising edge of clock to enable slave devices and then begin a SPI transfer at the rising edge of the master clock (CLKX).

27/ S = sample rate generator input clock = P if CLKSM = 1 (P = 1/CPU clock frequency)
= sample rate generator input clock = P_clks if CLKSM = 0(P_clks = CLKS period).
T = CLKX period = (1 + CLKGDV)*S
H = CLKX high pulse width = (CLKGDV/2 + 1)*S if CLKGDV is even.
= (CLKGDV + 1)2* S if CLKGDV is odd or zero.
L = CLKX low pulse width = (CLKGDV/2)*S if CLKGDV is even.
= (CLKGDV + 1)/2 * S if CLKGDV is odd or zero.

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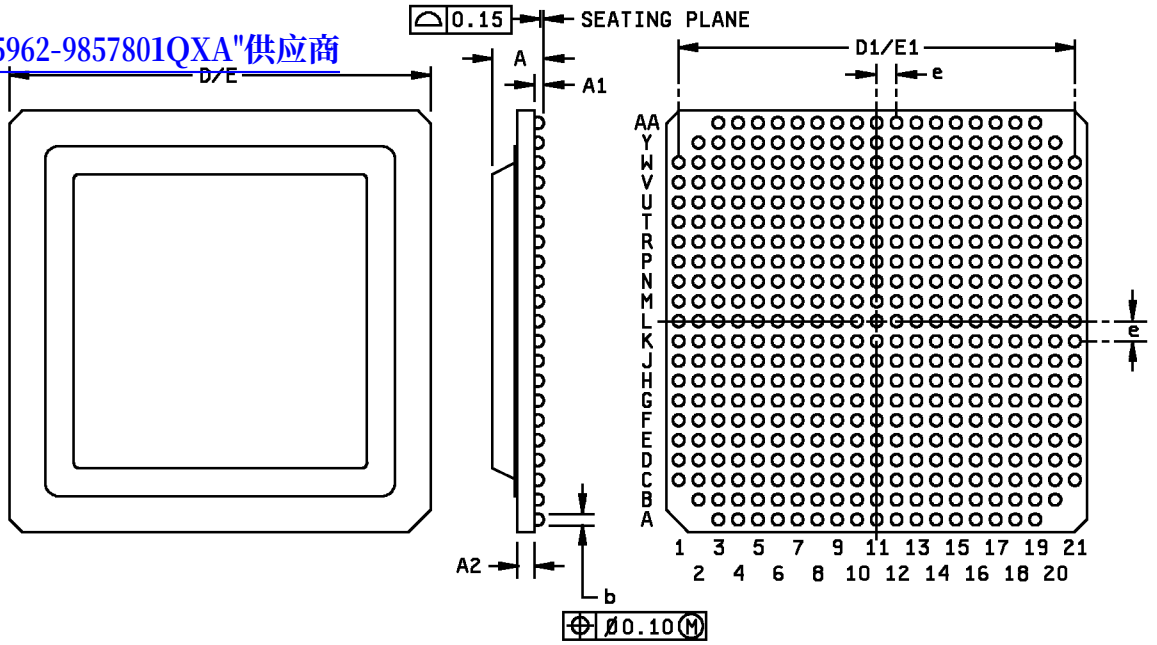

Case outline	X	
Symbol	Millimeters	
	Min	Max
A		3.30
A1	0.50	0.70
A2	1.00	1.22
b	0.60	0.90
D/E	26.80	27.20
D1/E1	25.40 BSC	25.40 BSC
e	1.27 BSC	1.27 BSC

NOTE: All dimensions are in Millimeters.

FIGURE 1. Case outline.

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Case outline	X				
Symbol number	Pin Symbol	Type	Symbol number	Pin Symbol	Type
A14	CLKIN	I	D8	HD2	I/O/Z
Y6	CLKOUT1	O	B7	HD1	I/O/Z
V9	CLKOUT2	O	C7	HD0	I/O/Z
B17	CLKMODE1	I	L6	HAS	I
C17	CLKMODE0	I	C5	HCS	I
C13	PLLFREQ3	I	C4	HDS1	I
G11	PLLFREQ2	I	K6	HDS2	I
F11	PLLFREQ1	I	H3	HRDY	O
D12	PLLV	A	B16	BOOTMODE4	I
G10	PLLG	A	G14	BOOTMODE3	I
C12	PLLF	A	F15	BOOTMODE2	I
K19	TMS	I	C18	BOOTMODE1	I
R12	TDO	O/Z	D17	BOOTMODE0	I
R13	TDI	I	Y5	CE3	O/Z
M20	TCK	I	V3	CE2	O/Z
N18	TRST	I	T6	CE1	O/Z
R20	EMU1	I/O/Z	U2	CE0	O/Z
T18	EMU0	I/O/Z	R8	BE3	O/Z
J20	RESET	I/O/Z	T3	BE2	O/Z
K21	NMI	I	T2	BE1	O/Z
R16	EXT_INT7	I	R2	BE0	O/Z
P20	EXT_INT6	I	L4	EA21	O/Z
R15	EXT_INT5	I	L3	EA20	O/Z
R18	EXT_INT4	I	J2	EA19	O/Z
R11	IACK	O	J1	EA18	O/Z
T19	INUM3	O	K1	EA17	O/Z
T20	INUM2	O	K2	EA16	O/Z
T14	INUM1	O	L2	EA15	O/Z
T16	INUM0	O	L1	EA14	O/Z
G20	LENDIAN	I	M1	EA13	O/Z
D19	PD	O	M2	EA12	O/Z
H2	HINT	O/Z	M6	EA11	O/Z
J6	HCNTL1	I	N4	EA10	O/Z
H6	HCNTL0	I	N1	EA9	O/Z
E4	HHWIL	I	N2	EA8	O/Z
G6	HBE1	I	N6	EA7	O/Z
F6	HBE0	I	P4	EA6	O/Z
D4	HR/W	I	P3	EA5	O/Z
D11	HD15	I/OZ	P2	EA4	O/Z
B11	HD14	I/O/Z	P1	EA3	O/Z
A11	HD13	I/O/Z	P6	EA2	O/Z
G9	HD12	I/O/Z	U18	ED31	I/O/Z
D10	HD11	I/O/Z	U20	ED30	I/O/Z
A10	HD10	I/O/Z	T15	ED29	I/O/Z
C10	HD9	I/O/Z	V18	ED28	I/O/Z
B9	HD8	I/O/Z	V17	ED27	I/O/Z
F9	HD7	I/O/Z	V16	ED26	I/O/Z
C9	HD6	I/O/Z	T12	ED25	I/O/Z
A9	HD5	I/O/Z	W17	ED24	I/O/Z
B8	HD4	I/O/Z	T13	ED23	I/O/Z
D9	HD3	I/O/Z	Y17	ED22	I/O/Z

I = Input, O = Output, Z = High Impedance, S = Supply voltage, GND = Ground.
PPLV and PLLG signals are not part of external voltage supply or ground. See the CLOCK/PLL documentation for information on how to connect those pins. A = Analog Signal (PLL Filter).

FIGURE 2. Terminal connections.

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Case outline	X				
Symbol number	Pin Symbol	Type	Symbol number	Pin Symbol	Type
T11	ED21	I/O/Z	F4	CLKS1	I
Y16	ED20	I/O/Z	H4	CLKR1	I/O/Z
W15	ED19	I/OZ	J4	CLKX1	I/O/Z
V14	ED18	I/O/Z	E2	DR1	I
Y15	ED17	I/O/Z	G4	DX1	O/Z
R9	ED16	I/O/Z	F3	FSR1	I/O/Z
Y14	ED15	I/O/Z	F2	FSX1	I/O/Z
V13	ED14	I/O/Z	K18	CLKS0	I
AA13	ED13	I/O/Z	L21	CLKR0	I/O/Z
T10	ED12	I/O/Z	K20	CLKX0	I/O/Z
Y13	ED11	I/O/Z	J21	DR0	I
W12	ED10	I/O/Z	M21	DX0	O/Z
Y12	ED9	I/O/Z	P16	FSR0	I/O/Z
Y11	ED8	I/O/Z	N16	FSX0	I/O/Z
V10	ED7	I/O/Z	N21	RSV0	I
AA10	ED6	I/O/Z	K16	RSV1	I
Y10	ED5	I/O/Z	B13	RSV2	I
W10	ED4	I/O/Z	B14	RSV3	I
Y9	ED3	I/O/Z	F13	RSV4	I
AA9	ED2	I/O/Z	C15	RSV5	O
Y8	ED1	I/O/Z	F7	RSV6	I
W9	$\overline{ED0}$	I/O/Z	D7	RSV7	I
R7	$\overline{ARE}$	O/Z	B5	RSV8	I
T7	$\overline{AOE}$	O/Z	C14	RSV9	O
V5	AWE	O/Z	C8	DV_{DD}	S
R4	$\overline{ARDY}$	I	E19	DV_{DD}	S
V8	$\overline{SSADS}$	O/Z	E3	DV_{DD}	S
W7	$\overline{SSOE}$	O/Z	H11	DV_{DD}	S
Y7	SSWE	O/Z	H13	DV_{DD}	S
AA8	SSCLK	O/Z	H9	DV_{DD}	S
V7	$\overline{SDA10}$	O/Z	J10	DV_{DD}	S
V6	$\overline{SDRAS}$	O/Z	J12	DV_{DD}	S
W5	$\overline{SDCAS}$	O/Z	J14	DV_{DD}	S
T8	SDWE	O/Z	J19	DV_{DD}	S
T9	SDCLK	O/Z	J3	DV_{DD}	S
R6	$\overline{HOLD}$	I	J8	DV_{DD}	S
B15	HOLDA	O	K11	DV_{DD}	S
G2	TOUT1	O/Z	K13	DV_{DD}	S
K3	TINP1	I	K15	DV_{DD}	S
M18	TOUT0	O/Z	K7	DV_{DD}	S
J18	TINP0	I	K9	DV_{DD}	S
E18	DMAC3	O	L10	DV_{DD}	S
F19	DMAC2	O	L12	DV_{DD}	S
E20	DMAC1	O	L14	DV_{DD}	S
G16	DMAC0	O	L8	DV_{DD}	S
				DV_{DD}	S

I = Input, O = Output, Z = High Impedance, S = Supply Voltage, GND = Ground
DV_{DD} = 3.3 V supply voltage

FIGURE 2. Terminal connections. - Continued.

查询"5962-9857801QXA"供应商

Case outline	X				
Symbol number	Pin Symbol	Type	Symbol number	Pin Symbol	Type
M11	DV_{DD}	S	C3	CV_{DD}	S
M13	DV_{DD}	S	C20	CV_{DD}	S
M15	DV_{DD}	S	D2	CV_{DD}	S
M7	DV_{DD}	S	D21	CV_{DD}	S
M9	DV_{DD}	S	E1	CV_{DD}	S
N0	DV_{DD}	S	E6	CV_{DD}	S
N12	DV_{DD}	S	E8	CV_{DD}	S
N14	DV_{DD}	S	E10	CV_{DD}	S
N19	DV_{DD}	S	E12	CV_{DD}	S
N3	DV_{DD}	S	E14	CV_{DD}	S
N8	DV_{DD}	S	E16	CV_{DD}	S
P11	DV_{DD}	S	F5	CV_{DD}	S
P13	DV_{DD}	S	F17	CV_{DD}	S
P9	DV_{DD}	S	F21	CV_{DD}	S
U19	DV_{DD}	S	G1	CV_{DD}	S
U3	DV_{DD}	S	H5	CV_{DD}	S
W14	DV_{DD}	S	H17	CV_{DD}	S
W8	DV_{DD}	S	K5	CV_{DD}	S
A12	CV_{DD}	S	K17	CV_{DD}	S
A13	CV_{DD}	S	M5	CV_{DD}	S
B10	CV_{DD}	S	M17	CV_{DD}	S
B12	CV_{DD}	S	P5	CV_{DD}	S
B6	CV_{DD}	S	P17	CV_{DD}	S
D15	CV_{DD}	S	R21	CV_{DD}	S
D16	CV_{DD}	S	T1	CV_{DD}	S
F10	CV_{DD}	S	T5	CV_{DD}	S
F14	CV_{DD}	S	T17	CV_{DD}	S
F8	CV_{DD}	S	U6	CV_{DD}	S
G13	CV_{DD}	S	U8	CV_{DD}	S
G7	CV_{DD}	S	U10	CV_{DD}	S
G8	CV_{DD}	S	U12	CV_{DD}	S
K4	CV_{DD}	S	U14	CV_{DD}	S
M3	CV_{DD}	S	U16	CV_{DD}	S
M4	CV_{DD}	S	U21	CV_{DD}	S
A3	CV_{DD}	S	V1	CV_{DD}	S
A5	CV_{DD}	S	V20	CV_{DD}	S
A7	CV_{DD}	S	W2	CV_{DD}	S
A16	CV_{DD}	S	W19	CV_{DD}	S
A18	CV_{DD}	S	W21	CV_{DD}	S
AA4	CV_{DD}	S	Y3	CV_{DD}	S
AA6	CV_{DD}	S	Y18	CV_{DD}	S
AA15	CV_{DD}	S	Y20	CV_{DD}	S
AA17	CV_{DD}	S	AA11	CV_{DD}	S
AA19	CV_{DD}	S	AA12	CV_{DD}	S
B2	CV_{DD}	S	F20	CV_{DD}	S
B4	CV_{DD}	S	G18	CV_{DD}	S
B19	CV_{DD}	S	H16	CV_{DD}	S
C1	CV_{DD}	S			

I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground
DV_{DD} = 3.3 V supply voltage, CV_{DD} = 1.8 V supply voltage

FIGURE 2. Terminal connections - Continued

查询"5962-9857801QXA"供应商

Case outline	X				
Symbol number	Pin Symbol	Type	Symbol number	Pin Symbol	Type
H18	CV_{DD}	S	AA18	V_{SS}	GND
L18	CV_{DD}	S	B3	V_{SS}	GND
L19	CV_{DD}	S	B18	V_{SS}	GND
L20	CV_{DD}	S	B20	V_{SS}	GND
N20	CV_{DD}	S	C2	V_{SS}	GND
P18	CV_{DD}	S	C19	V_{SS}	GND
P19	CV_{DD}	S	C21	V_{SS}	GND
R10	CV_{DD}	S	D1	V_{SS}	GND
R14	CV_{DD}	S	D20	V_{SS}	GND
U4	CV_{DD}	S	E5	V_{SS}	GND
V11	CV_{DD}	S	E7	V_{SS}	GND
V12	CV_{DD}	S	E9	V_{SS}	GND
V15	CV_{DD}	S	E11	V_{SS}	GND
W13	CV_{DD}	S	E13	V_{SS}	GND
C11	V_{SS}	GND	E15	V_{SS}	GND
C16	V_{SS}	GND	E17	V_{SS}	GND
C6	V_{SS}	GND	E21	V_{SS}	GND
D5	V_{SS}	GND	F1	V_{SS}	GND
G3	V_{SS}	GND	G5	V_{SS}	GND
H10	V_{SS}	GND	G17	V_{SS}	GND
H12	V_{SS}	GND	G21	V_{SS}	GND
H14	V_{SS}	GND	H1	V_{SS}	GND
H7	V_{SS}	GND	J5	V_{SS}	GND
H8	V_{SS}	GND	J17	V_{SS}	GND
J11	V_{SS}	GND	L5	V_{SS}	GND
J13	V_{SS}	GND	L17	V_{SS}	GND
J7	V_{SS}	GND	N5	V_{SS}	GND
J9	V_{SS}	GND	N17	V_{SS}	GND
K8	V_{SS}	GND	P21	V_{SS}	GND
L7	V_{SS}	GND	R1	V_{SS}	GND
L9	V_{SS}	GND	R5	V_{SS}	GND
M8	V_{SS}	GND	R17	V_{SS}	GND
N7	V_{SS}	GND	T21	V_{SS}	GND
R3	V_{SS}	GND	U1	V_{SS}	GND
A4	V_{SS}	GND	U5	V_{SS}	GND
A6	V_{SS}	GND	U7	V_{SS}	GND
A8	V_{SS}	GND	U9	V_{SS}	GND
A15	V_{SS}	GND	U11	V_{SS}	GND
A17	V_{SS}	GND	U13	V_{SS}	GND
A19	V_{SS}	GND	U15	V_{SS}	GND
AA3	V_{SS}	GND	U17	V_{SS}	GND
AA5	V_{SS}	GND	V2	V_{SS}	GND
AA7	V_{SS}	GND	V21	V_{SS}	GND
AA14	V_{SS}	GND	W1	V_{SS}	GND
AA16	V_{SS}	GND	W3	V_{SS}	GND
			W20	V_{SS}	GND
			Y2	V_{SS}	GND
			Y4	V_{SS}	GND
			Y19	V_{SS}	GND

I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground
CV_{DD} = 1.8 V supply voltage

FIGURE 2. Terminal connections - Continued

查询"5962-9857801QXA"供应商

Case outline	X				
Symbol number	Pin Symbol	Type	Symbol number	Pin Symbol	Type
F18	V_{SS}	GND	D13	NC	
G19	V_{SS}	GND	D14	NC	
H15	V_{SS}	GND	D18	NC	
J15	V_{SS}	GND	D3	NC	
J16	V_{SS}	GND	D6	NC	
K10	V_{SS}	GND	F12	NC	
K12	V_{SS}	GND	G12	NC	
K14	V_{SS}	GND	G15	NC	
L11	V_{SS}	GND	H19	NC	
L13	V_{SS}	GND	H20	NC	
L15	V_{SS}	GND	H21	NC	
M10	V_{SS}	GND	L16	NC	
M12	V_{SS}	GND	M16	NC	
M14	V_{SS}	GND	M19	NC	
N11	V_{SS}	GND	V19	NC	
N13	V_{SS}	GND	V4	NC	
N15	V_{SS}	GND	W18	NC	
N9	V_{SS}	GND	W4	NC	
P10	V_{SS}	GND			
P12	V_{SS}	GND			
P14	V_{SS}	GND			
P15	V_{SS}	GND			
P7	V_{SS}	GND			
P8	V_{SS}	GND			
R19	V_{SS}	GND			
T4	V_{SS}	GND			
W11	V_{SS}	GND			
W16	V_{SS}	GND			
W6	V_{SS}				

I = Input, O = Output, Z = High impedance, S = Supply voltage, GND = Ground. NC = No connection

FIGURE 2. Terminal connections - Continued

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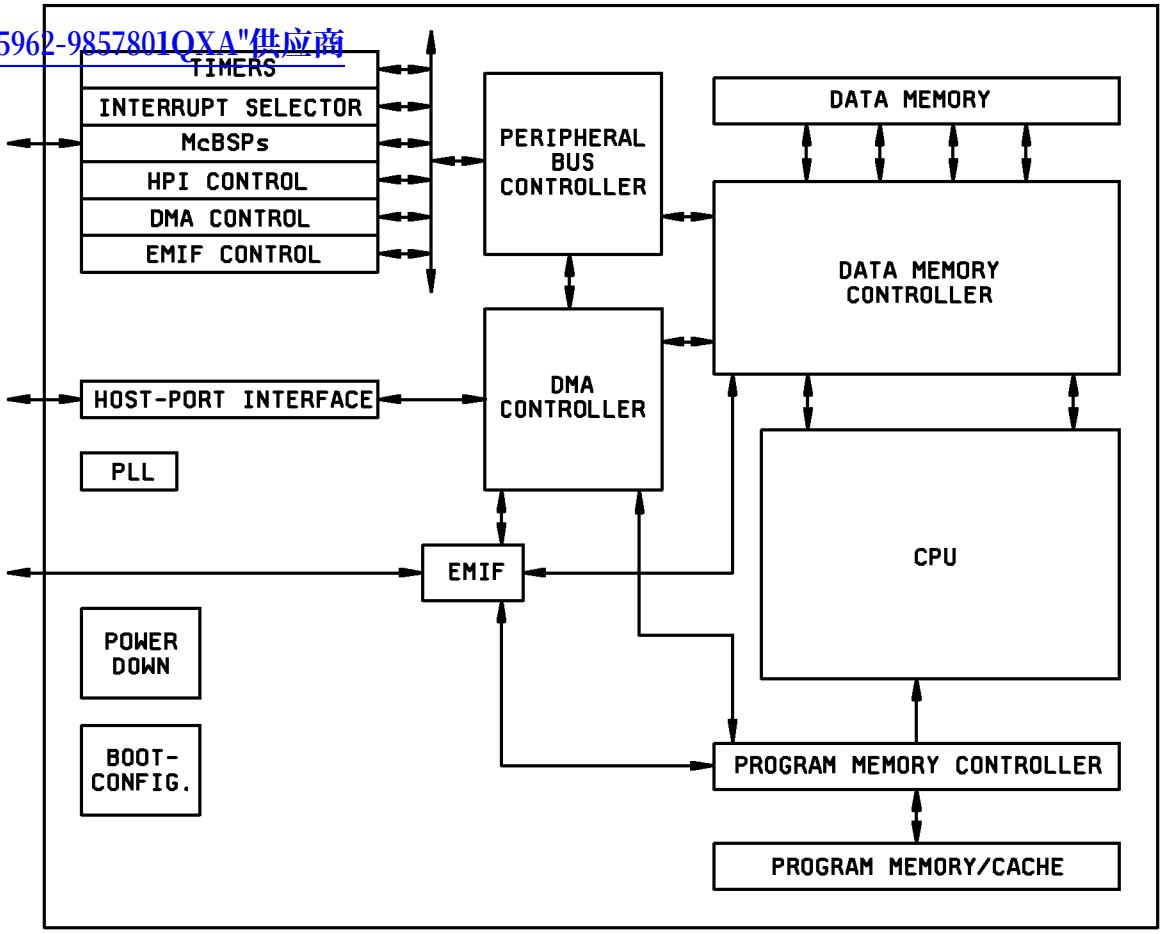

FIGURE 3. Block diagram.

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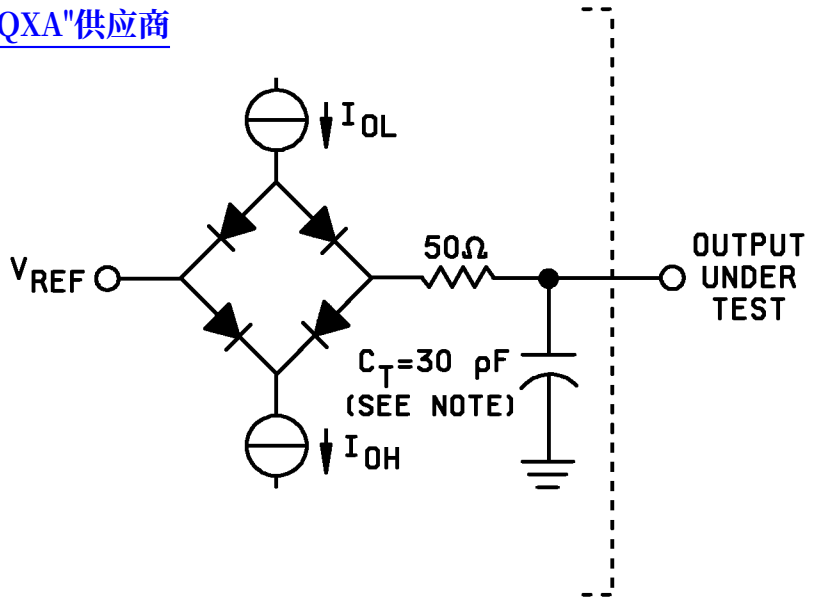
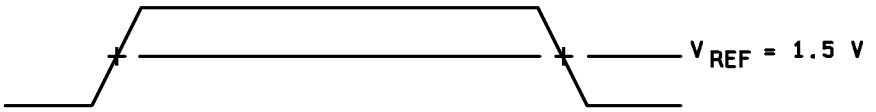
Tester Pin Electronics



TTL-LEVEL OUTPUTS

NOTE:

All input and output timing parameters are referenced to 1.5 V for both “0” and “1” logic levels.



INPUT AND OUTPUT VOLTAGE REFERENCE LEVELS FOR AC TIMING MEASUREMENTS

FIGURE 4. Timing waveforms.

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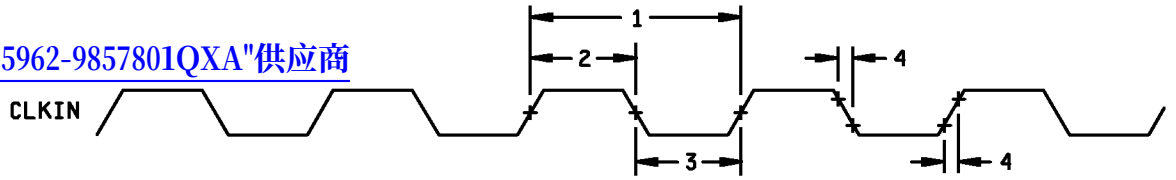
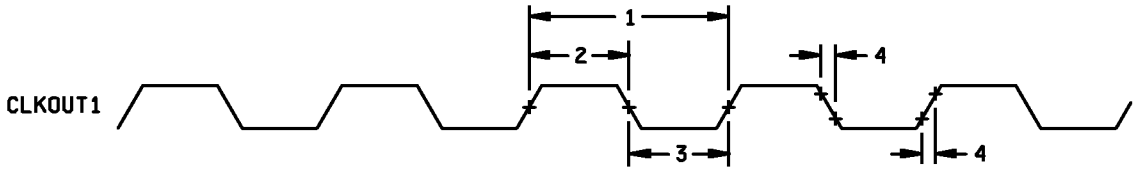
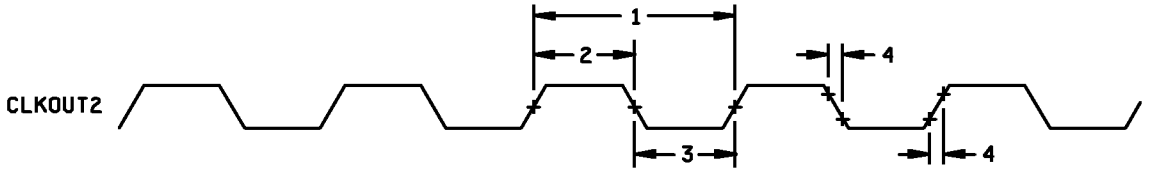


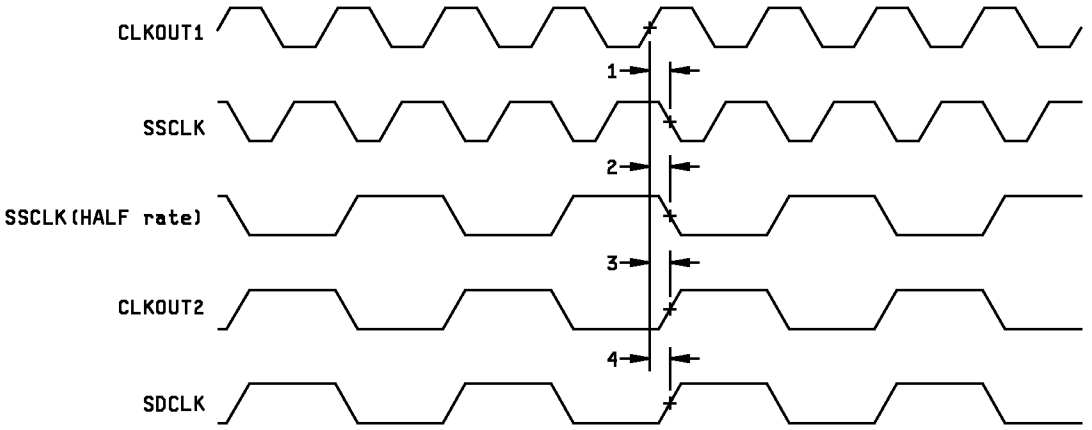
CLKIN TIMINGS



CLKOUT1 TIMINGS



CLKOUT2 TIMINGS



RELATION OF CLKOUT2,SDCLK,AND SSCLK TO CLKOUT1

FIGURE 4. Timing waveforms.- Continued

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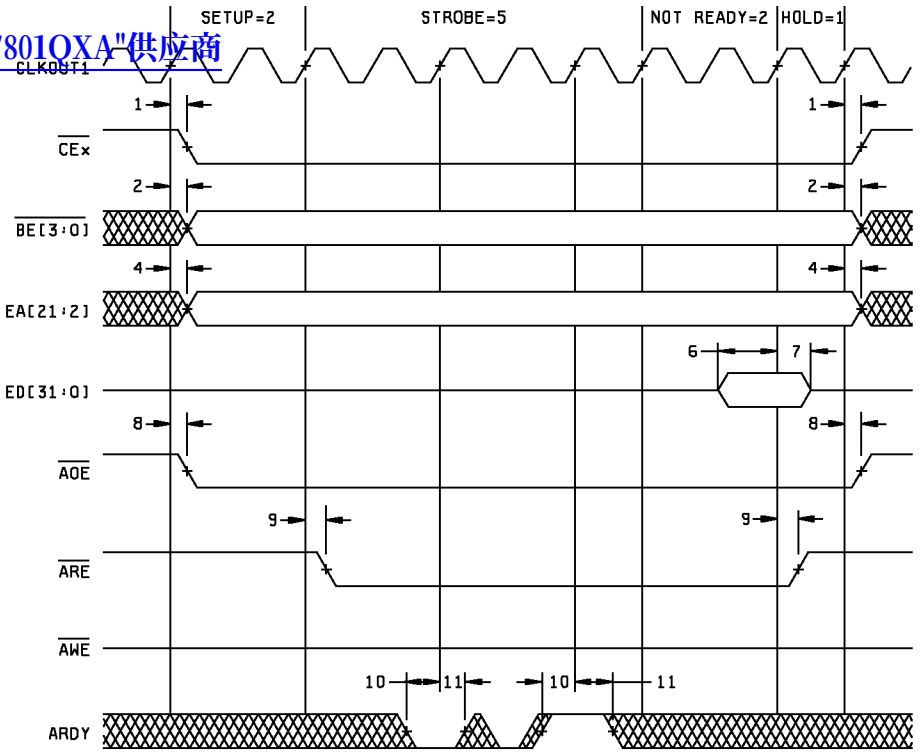
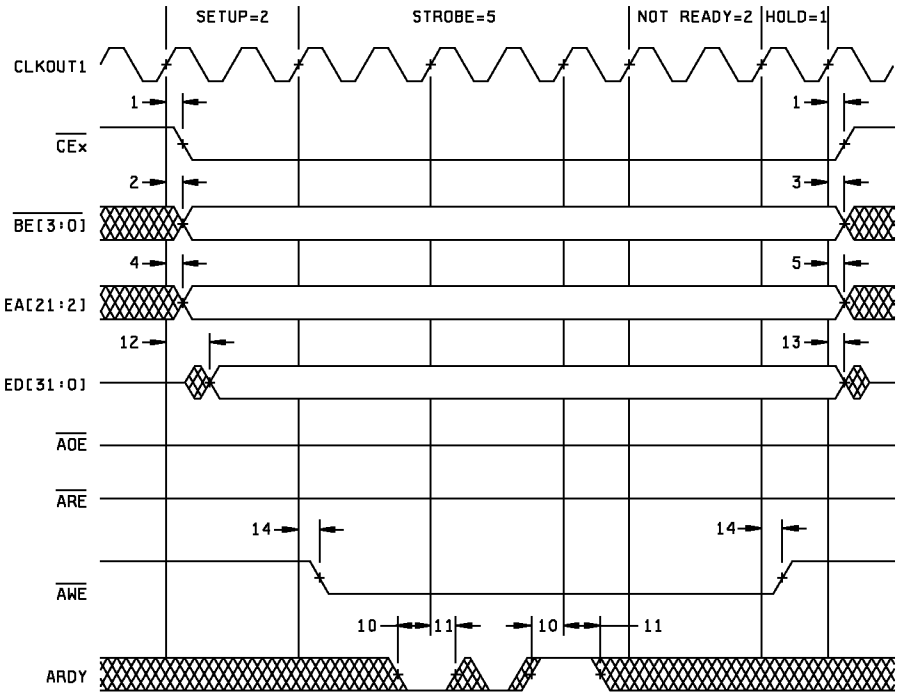


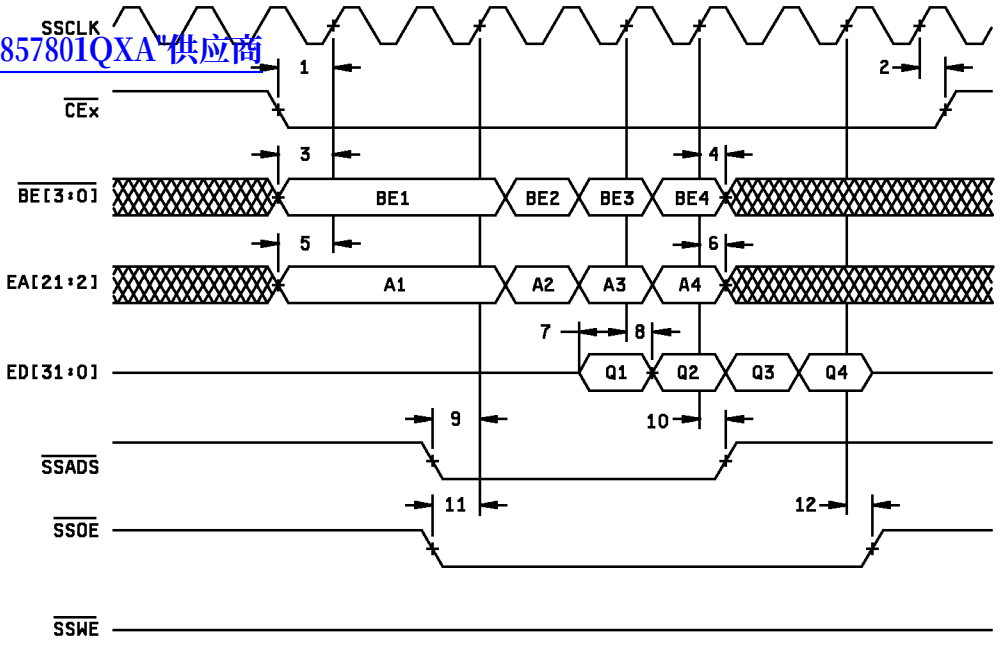
ASYNCHRONOUS MEMORY READ TIMING



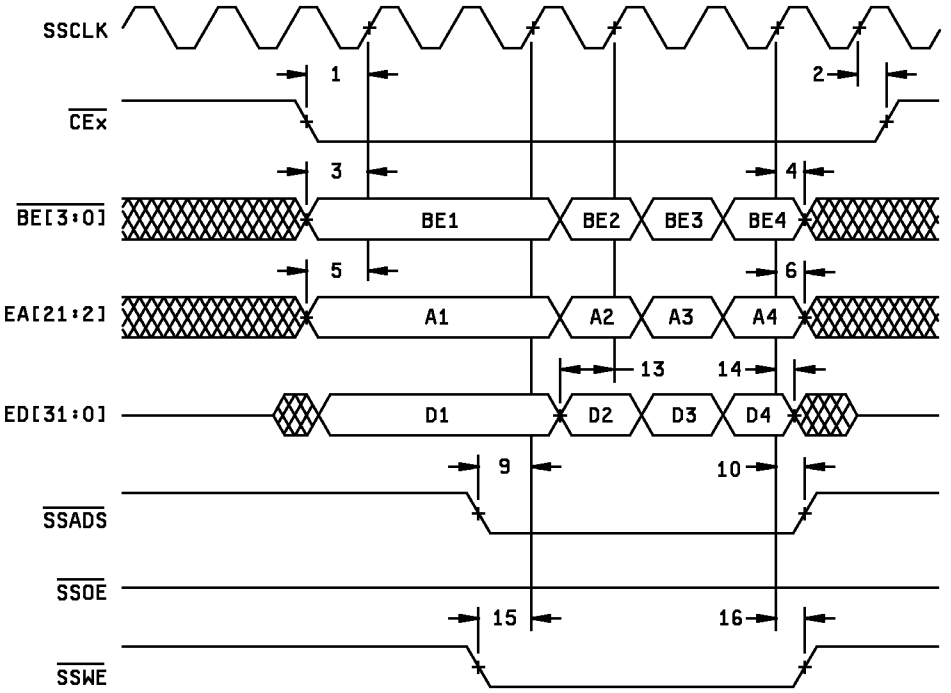
ASYNCHRONOUS MEMORY WRITE TIMING

FIGURE. 4. Timing waveforms. - Continued

查询"5962-9857801QXA"供应商



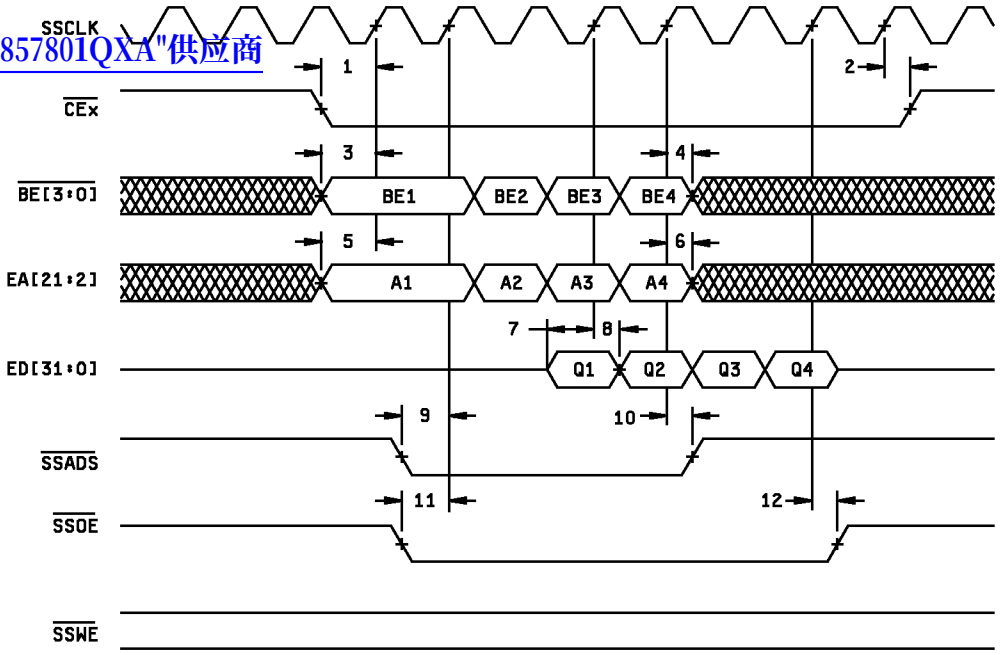
SBSRAM READ TIMING(FULL-RATE SSCLK)



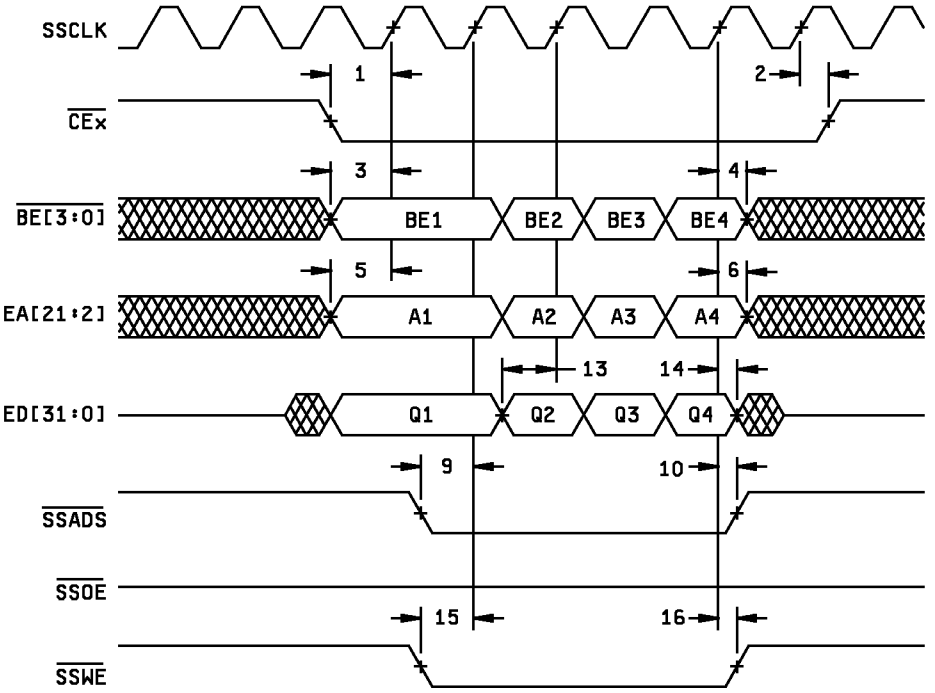
SBSRAM WRITE TIMING(FULL-RATE SSCLK)

FIGURE 4. Timing waveforms. - Continued

查询"5962-9857801QXA"供应商



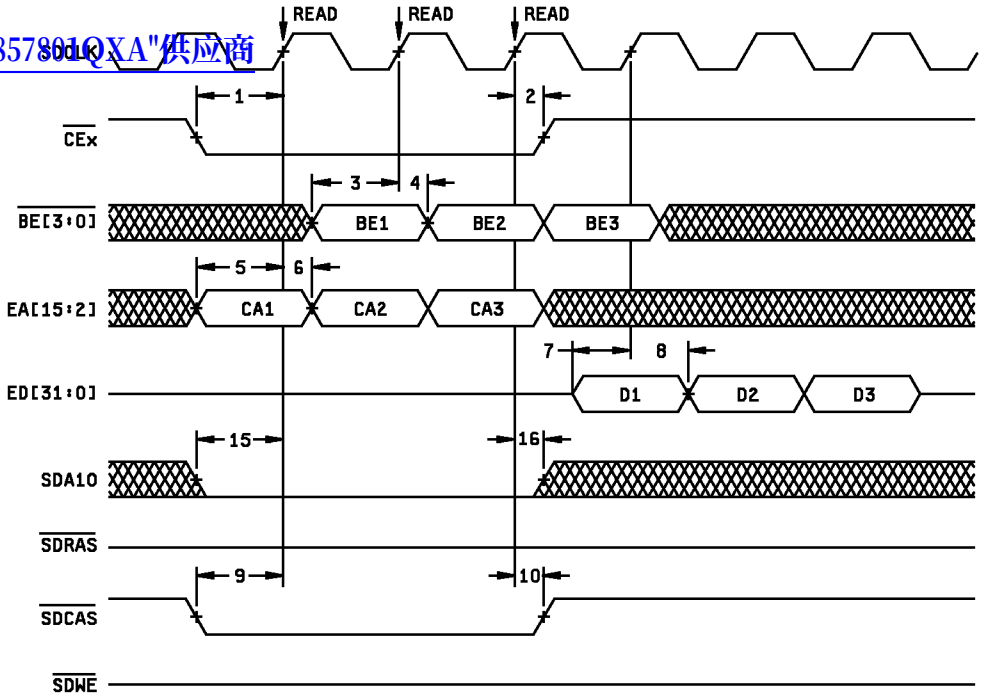
SBSRAM READ TIMING(HALF-RATE SSCLK)



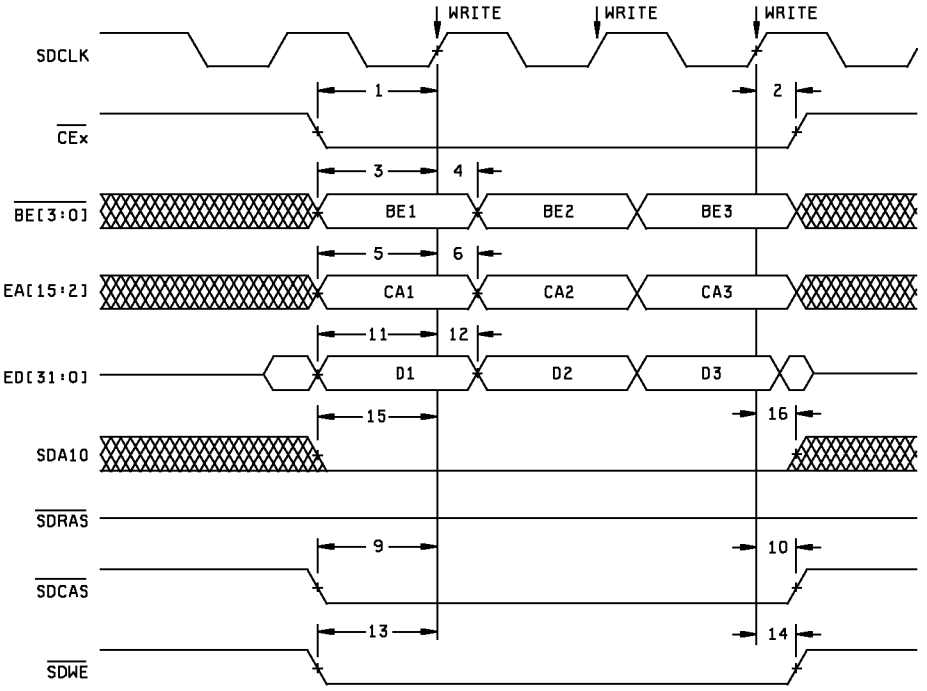
SBSRAM WRITE TIMING(HALF-RATE SSCLK)

FIGURE 4. Timing waveforms. - Continued

查询"5962-9857801QXA"供应商



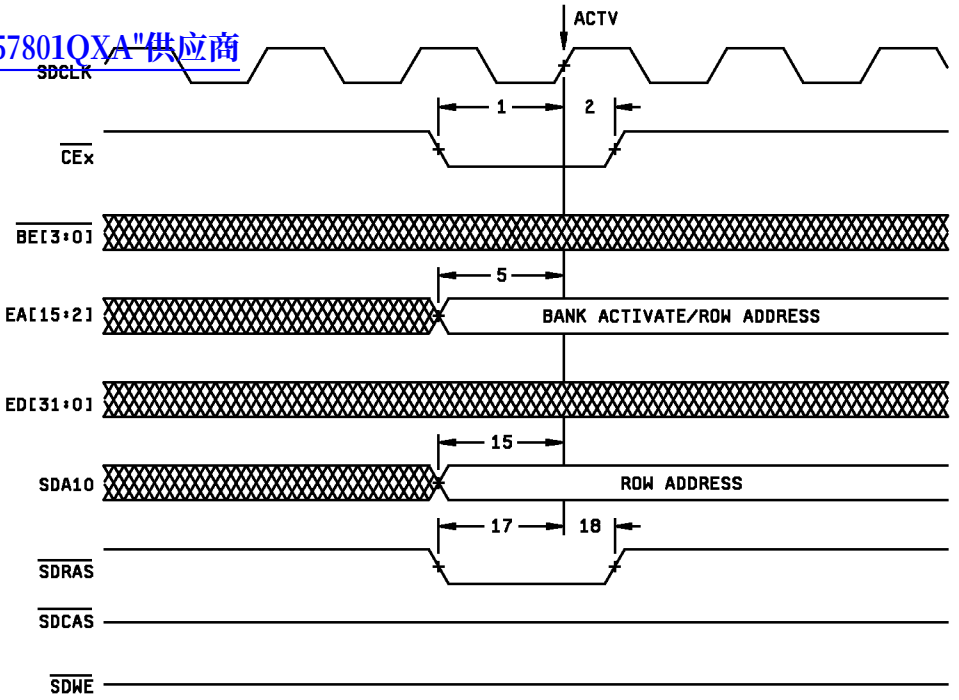
THREE SDRAM READ COMMANDS



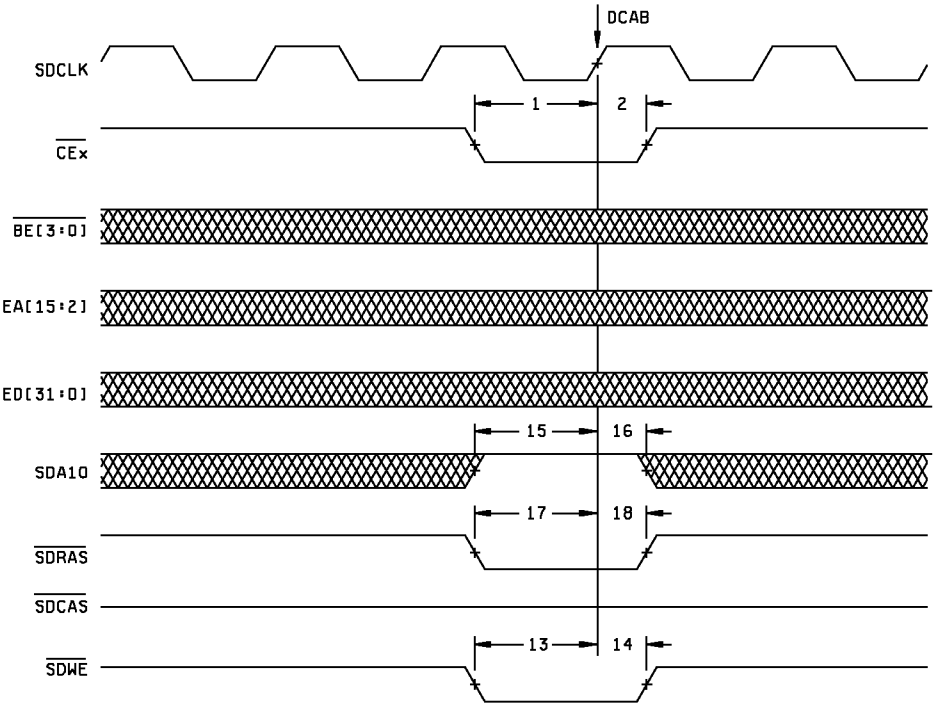
THREE SDRAM WRT COMMANDS

FIGURE 4. Timing waveforms. - Continued

查询"5962-9857801QXA"供应商



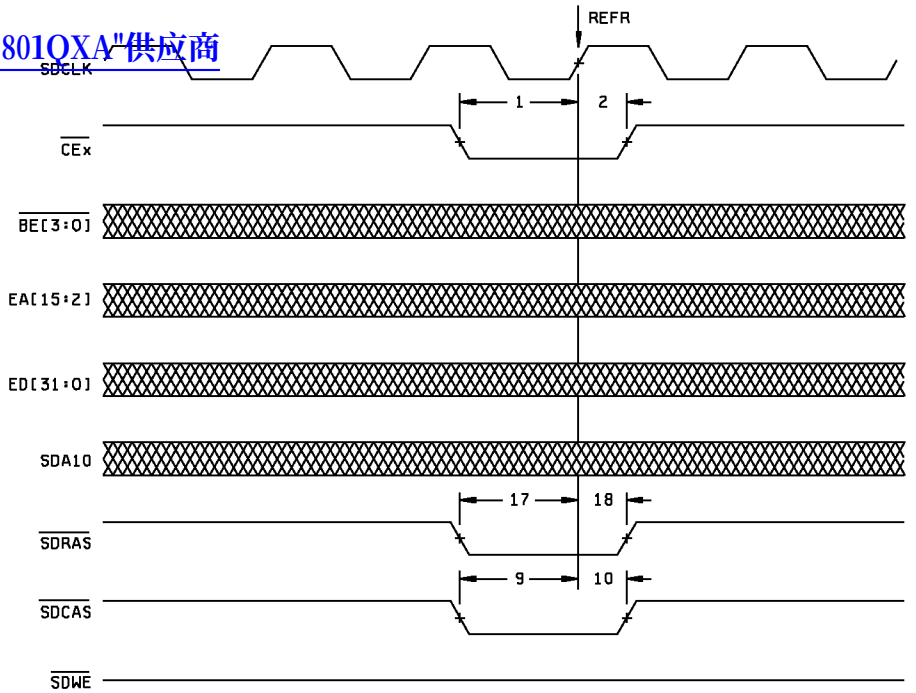
SDRAM ACTV COMMAND



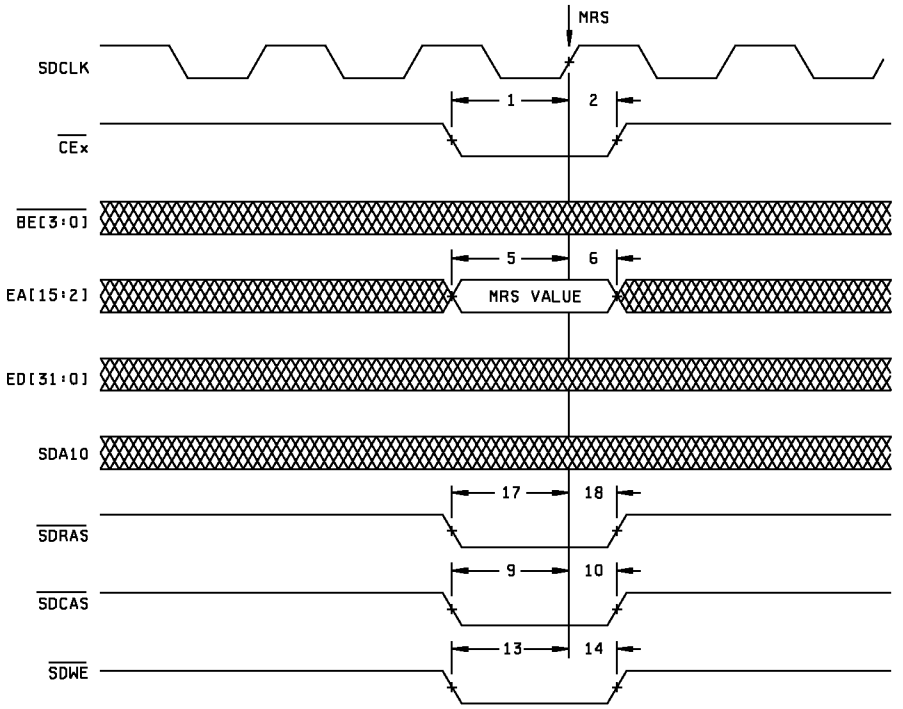
SDRAM DCAB COMMAND

FIGURE 4. Timing waveforms. - Continued

查询"5962-9857801QXA"供应商



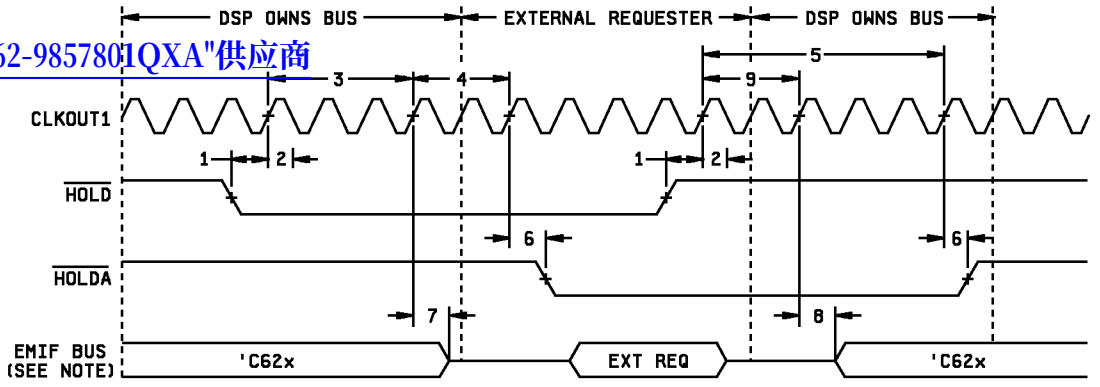
SDRAM REFR COMMAND



SDRAM MRS COMMAND

FIGURE 4. Timing waveforms. - Continued

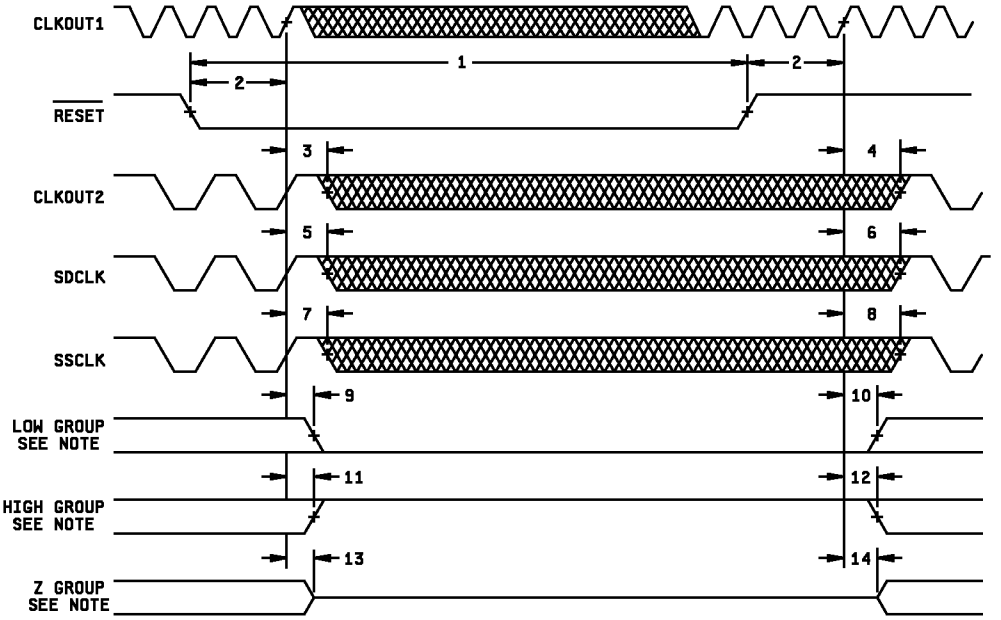
查询"5962-9857801QXA"供应商



HOLD/HOLDA TIMING

NOTE:

EMIF Bus consists of CE[3:0], BE[3:0], ED[31:0], EA[21:2], ARE, AOE, AWE, SSADS, SSOE, SSWE, SDA10, SDRAS, SDCAS, and SDWE.

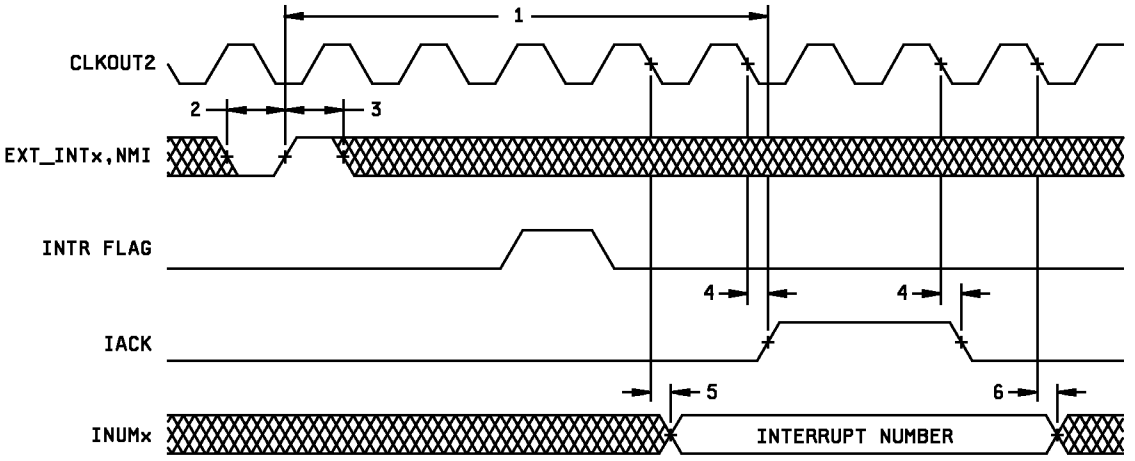


RESET TIMING

NOTES:
Low group consists of: IACK, INUM[3:0], DMAC[3:0], PD, TOUT0, and TOUT1.
High group consists of: HINT.
Z group consists of: EA[21:2], ED[31:0], CE[3:0], BE[3:0], ARE, AWE, AOE, SSADS, SSOE, SSWE, SDA10, SDRAS, SDCAS SDWE, HD[15:0], CLKX0, CLKX1, FSX0, FSX1, DX0,DX1, CLKR0, CLKR1, FSR0, and FSR1.

FIGURE 4. Timing waveforms. - Continued

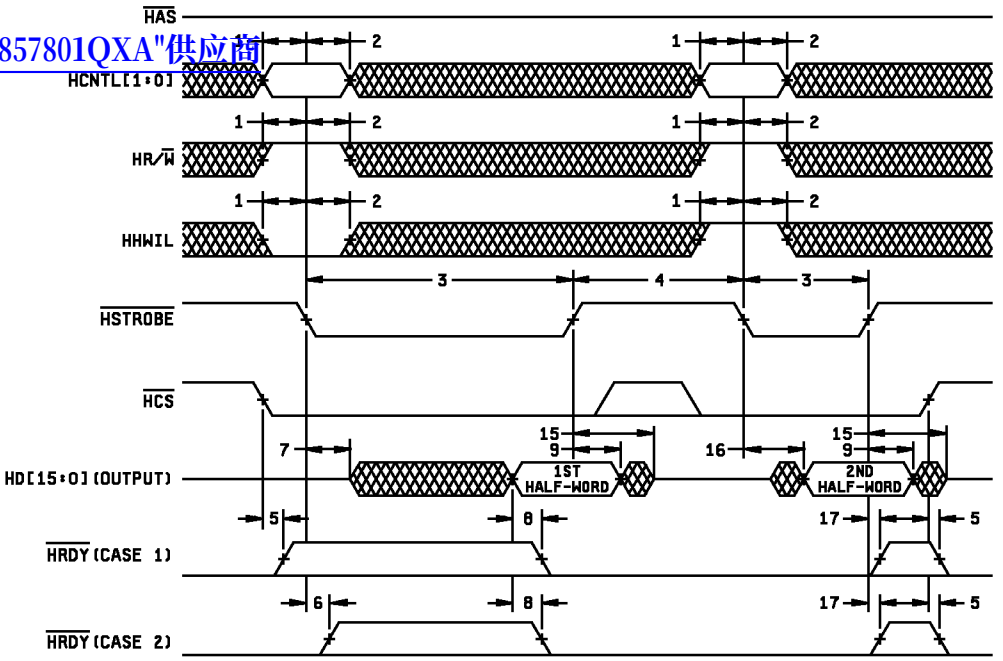
查询"5962-9857801QXA"供应商



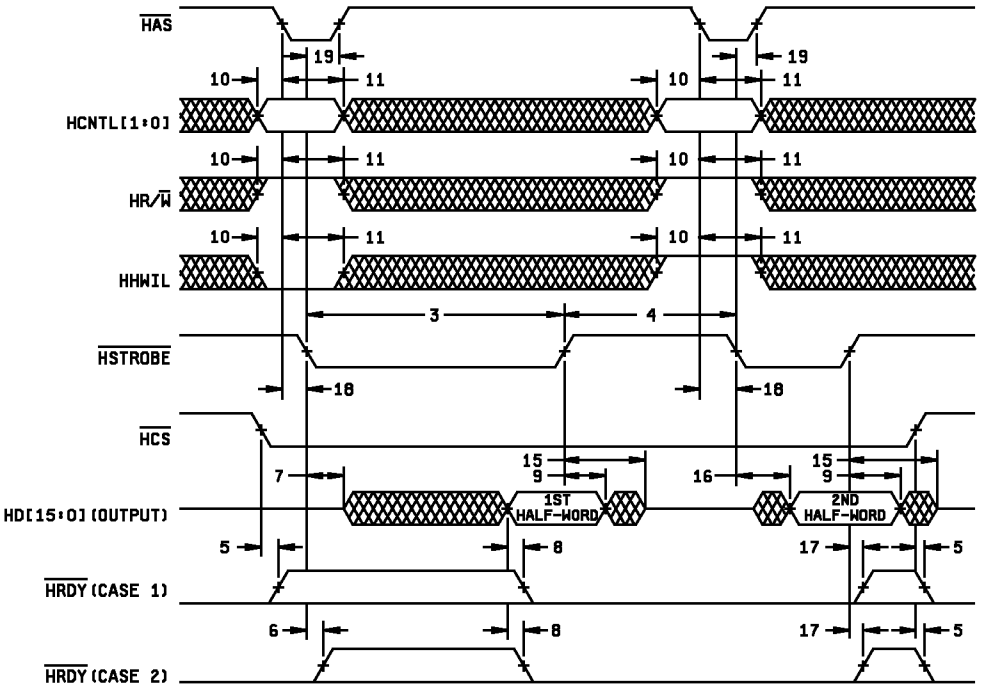
INTERRUPT TIMING

FIGURE 4. Timing waveforms. - Continued

查询"5962-9857801QXA"供应商



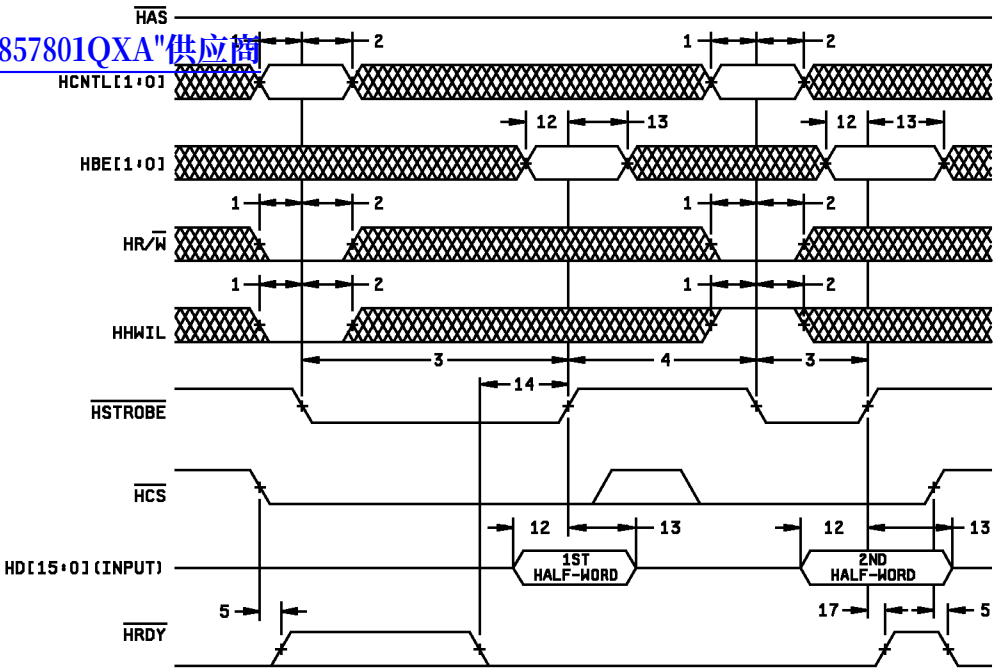
HPI READ TIMING (HAS NOT USED,TIED HIGH)



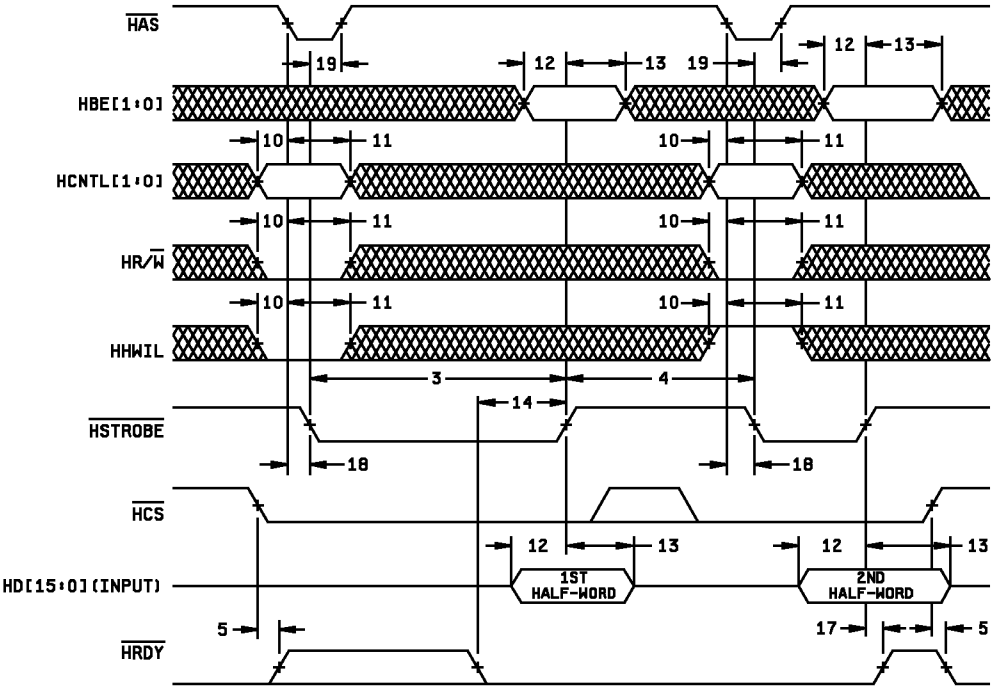
HPI READ TIMING (HAS USED)

FIGURE 4. Timing waveforms. - Continued

查询"5962-9857801QXA"供应商



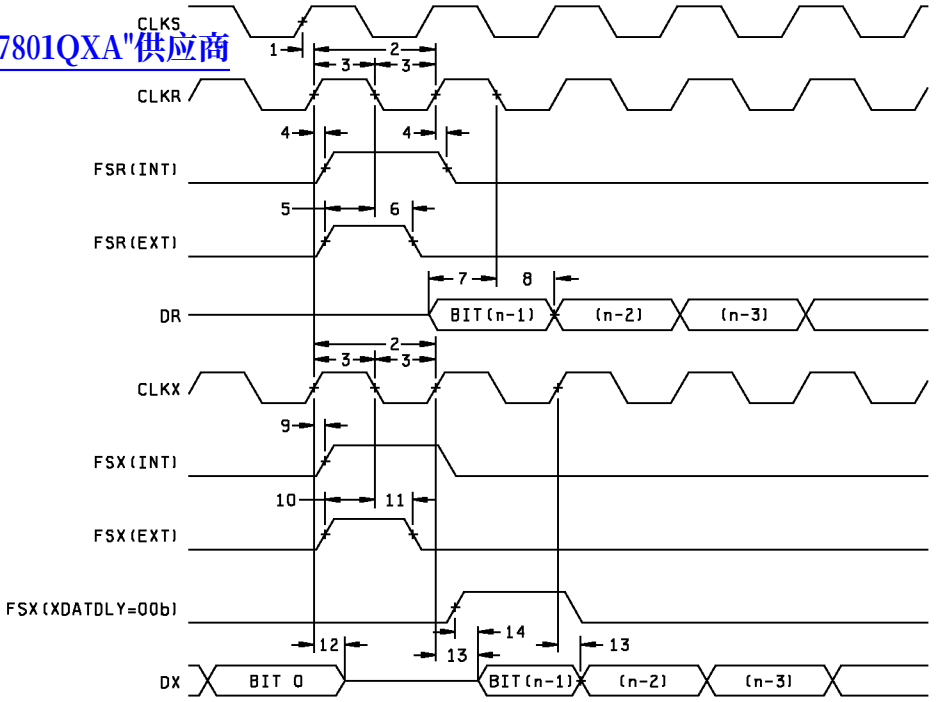
HPI WRITE TIMING (HAS NOT USED,TIED HIGH)



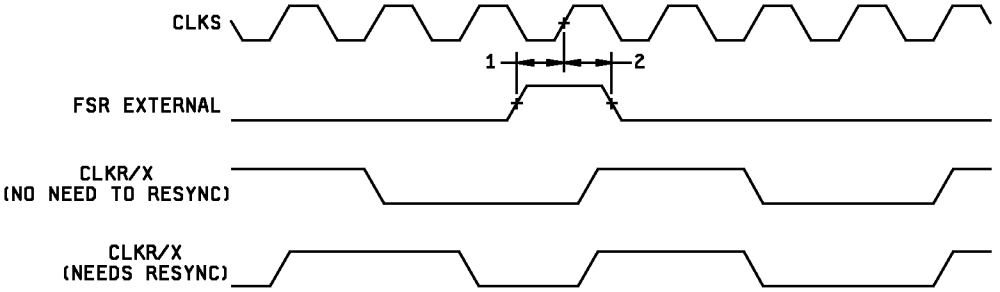
HPI WRITE TIMING (HAS USED)

FIGURE 4. Timing waveforms. - Continued

查询"5962-9857801QXA"供应商



McBSP TIMINGS



FSR TIMING WHEN GSYNC=1

FIGURE 4. Timing waveforms. – Continued

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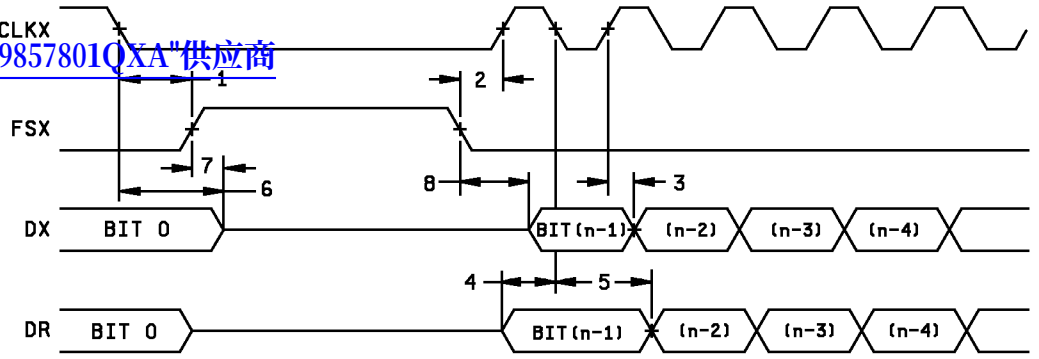
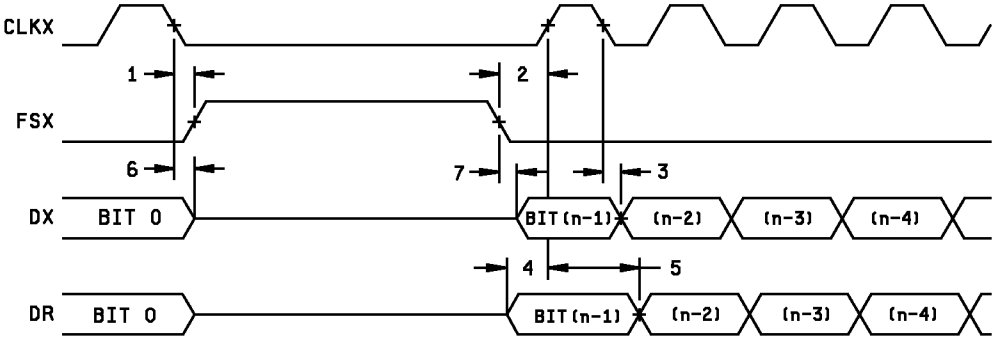
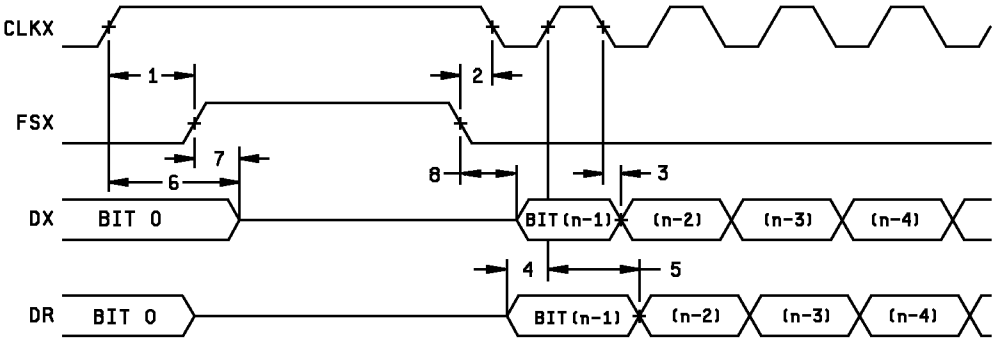


McBSP TIMING AS SPI MASTER OR SLAVE:CLKSTP=10b,CLKXP=0



McBSP TIMING AS SPI MASTER OR SLAVE:CLKSTP=11b,CLKXP=0



McBSP TIMING AS SPI MASTER OR SLAVE:CLKSTP=10b,CLKXP=1

FIGURE 4. Timing waveforms. – Continued

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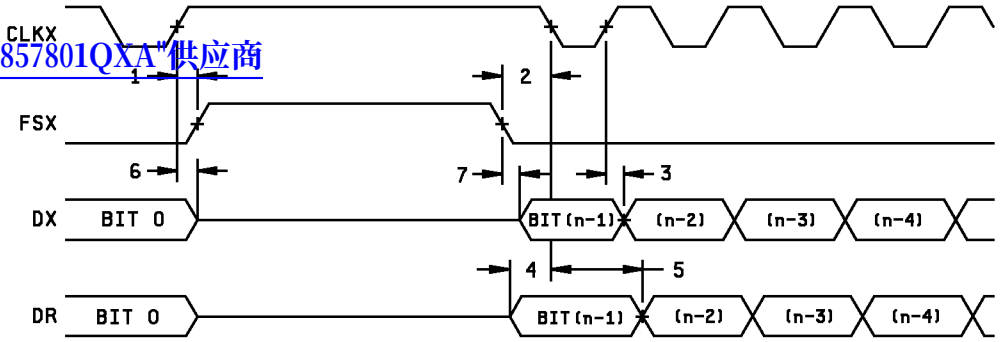
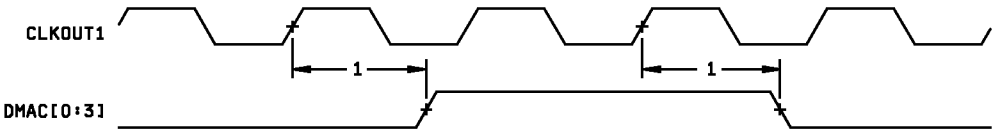
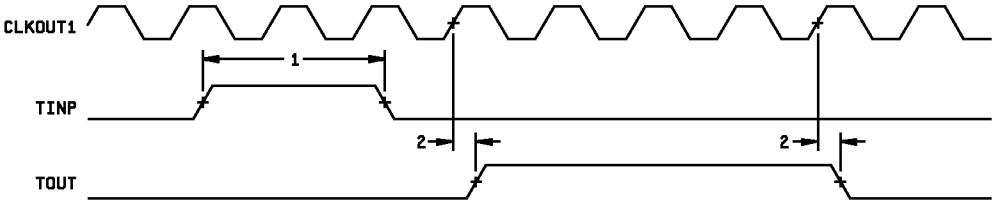


McBSP TIMING AS SPI MASTER OR SLAVE:CLKSTP=11b,CLKXP=1



DMAC TIMING



TIMER TIMING

FIGURE 4. Timing waveforms. – Continued

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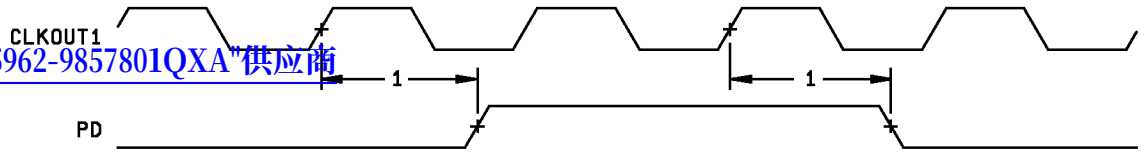
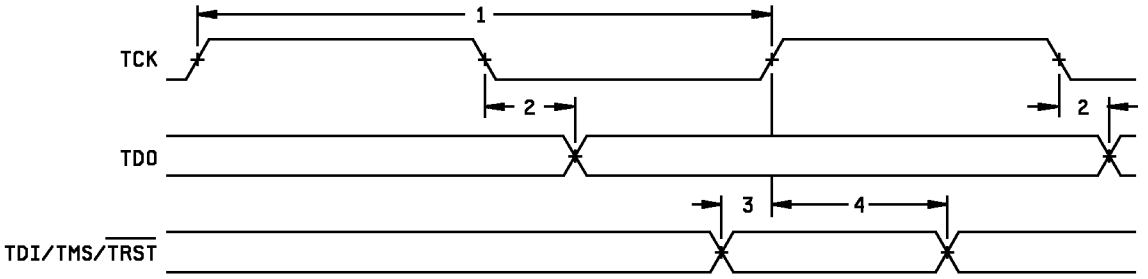


POWER-DOWN TIMING



JTAG TEST-PORT TIMING

FIGURE 4. Timing waveforms. - Continued

4. QUALITY ASSURANCE PROVISIONS

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4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

(2) T_A = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-PRF-38535 permits alternate in-line control testing. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

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a. Tests shall be as specified in table II herein.

b. Subgroup 4 (C_{IN}, C_{OUT}) shall be measured only for the initial test and after process or design changes which may affect input capacitance. One pin of each input/output driver (buffer) type shall be tested on each sample device. A minimum sample size of 5 devices with zero rejects shall be required.

c. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the functionality of the device. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device; these tests shall have been fault graded in accordance with MIL-STD-883, test method 5012 (see 1.5 herein).

TABLE II. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class M	Device class Q	Device class V
Interim electrical parameters (see 4.2)	1, 7	1, 7	1, 7
Final electrical parameters (see 4.2)	1/ 1,2,3,7,8,9,10,11	1/1,2,3,7,8,9, 10,11	2/ 1,2,3,7,8, 9,10,11
Group A test requirements (see 4.4)	1,2,3,7,8,9,10,11	1,2,3,7,8,9, 10,11	1,2,3,7,8,9, 10,11
Group C end-point electrical parameters (see 4.4)	1,7,9	1,7,9	1,7,9
Group D end-point electrical parameters (see 4.4)	1,7,9	1,7,9	1,7,9
Group E end-point electrical parameters (see 4.4)			

1/ PDA applies to subgroup 1.
2/ PDA applies to subgroups 1 and 7.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a Test condition D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

b. T_A = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

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4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

a. End-point electrical parameters shall be as specified in table II herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at T_A = +25°C ±5°C, after exposure, to the subgroups specified in table II herein.

c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform Defense Supply Center Columbus when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0674.

6.4 Comments. Comments on this drawing should be directed to DSCC-VA , Columbus, Ohio 43216-5000, or telephone (614) 692-0674.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

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6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DSCC-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

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STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 00-01-31

Approved sources of supply for SMD 5962-98578 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-9857801QXA	01295	SMJ320C6201B

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the vendor to determine its availability.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number	Vendor name and address
01295	Texas Instruments Incorporated 13500 N. Central Expressway P.O. Box 655303 Dallas, TX 75265 Point of contact: 6412 Highway 75 South Sherman, TX 75090-0084

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.