



74AC16374

16-BIT D-TYPE FLIP-FLOP WITH 3-STATE OUTPUTS (NON INVERTED)

- HIGH SPEED:
 $f_{MAX} = 120\text{MHz}$ (TYP.) at $V_{CC} = 5\text{V}$
- LOW POWER DISSIPATION:
 $I_{CC} = 8\mu\text{A}$ (MAX.) at $T_A=25^\circ\text{C}$
- HIGH NOISE IMMUNITY:
 $V_{NIH} = V_{NIL} = 28\% V_{CC}$ (MIN.)
- 50Ω TRANSMISSION LINE DRIVING CAPABILITY
- SYMMETRICAL OUTPUT IMPEDANCE:
 $|I_{OH}| = I_{OL} = 24\text{mA}$ (MIN)
- OPERATING VOLTAGE RANGE:
 V_{CC} (OPR) = 2V to 6V
- IMPROVED LATCH-UP IMMUNITY



ORDER CODES

PACKAGE	TUBE	T & R
TSSOP		74AC16374TTR

DESCRIPTION

The 74AC16374 is an advanced high-speed CMOS 16-BIT D-TYPE FLIP-FLOP (3-STATE) fabricated with sub-micron silicon gate and double-layer metal wiring C²MOS technology.

This 16 bit D-Type Flip-Flop is controlled by two clock inputs (CK) and two output enable inputs (\overline{OE}). The device can be used as two 8-bit flip-flops or one 16-bit flip-flop.

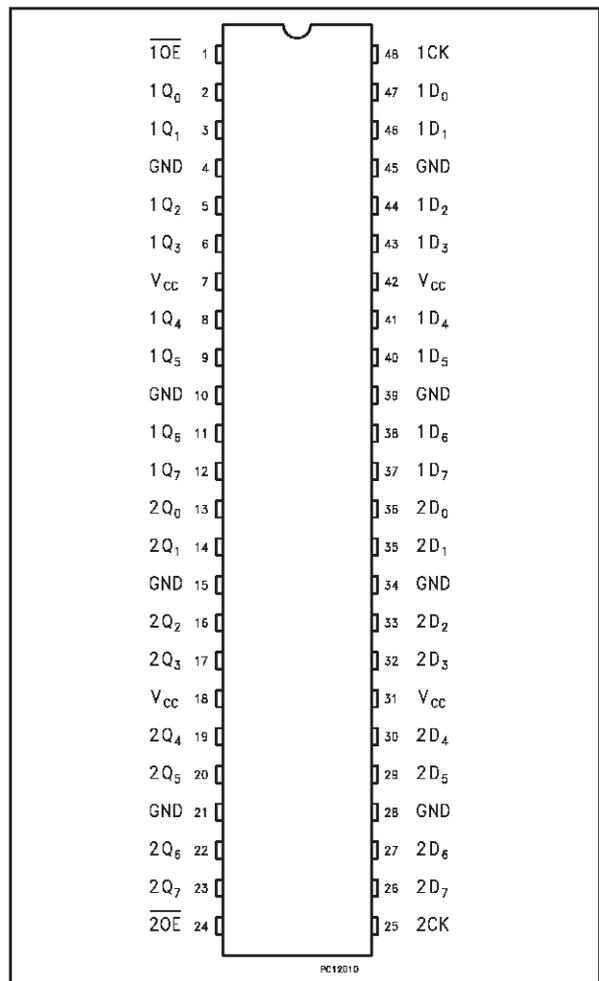
On the positive transition of the clock, the Q outputs will be set to the logic state that were setup at the D inputs.

While the (\overline{OE}) input is low, the outputs will be in a normal logic state (high or low logic level); while \overline{OE} is high, the outputs will be in a high impedance state.

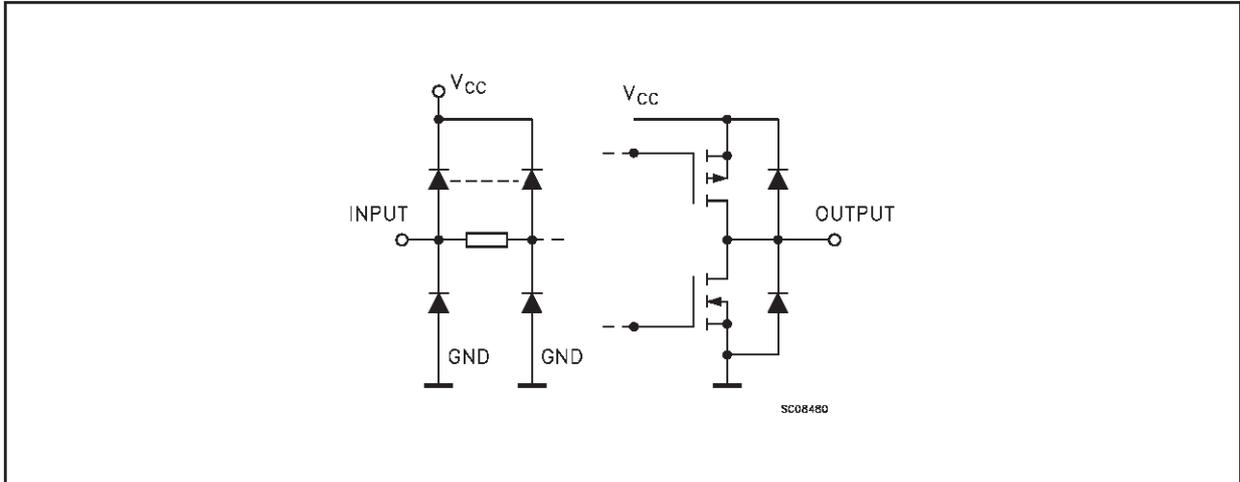
The output control does not affect the internal operation of flip-flops; that is, the old data can be retained or the new data can be entered even while the outputs are off.

All inputs and outputs are equipped with protection circuits against static discharge, giving them 2KV ESD immunity and transient excess voltage.

PIN CONNECTION



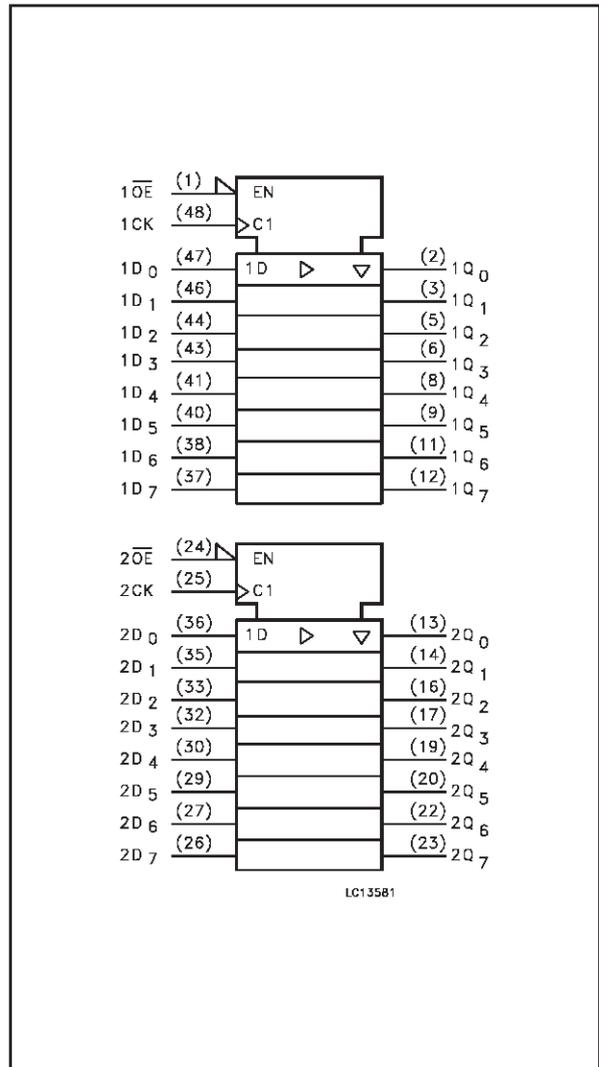
INPUT AND OUTPUT EQUIVALENT CIRCUIT



PIN DESCRIPTION

PIN No	SYMBOL	NAME AND FUNCTION
1	1OE	3 State Output Enable Input (Active LOW)
2, 3, 5, 6, 8, 9, 11, 12	1Q0 to 1Q7	3-State Outputs
13, 14, 16, 17, 19, 20, 22, 23	2Q0 to 2Q7	3-State Outputs
24	2OE	3 State Output Enable Input (Active LOW)
25	2CK	Clock Input (LOW-to-HIGH Edge Trigger)
36, 35, 33, 32, 30, 29, 27, 26	2D0 to 2D7	Data Inputs
47, 46, 44, 43, 41, 40, 38, 37	1D0 to 1D7	Data Inputs
48	1CK	Clock Input (LOW-to-HIGH Edge Trigger)
4, 10, 15, 21, 28, 34, 39, 45	GND	Ground (0V)
7, 18, 31, 42	V _{CC}	Positive Supply Voltage

IEC LOGIC SYMBOLS

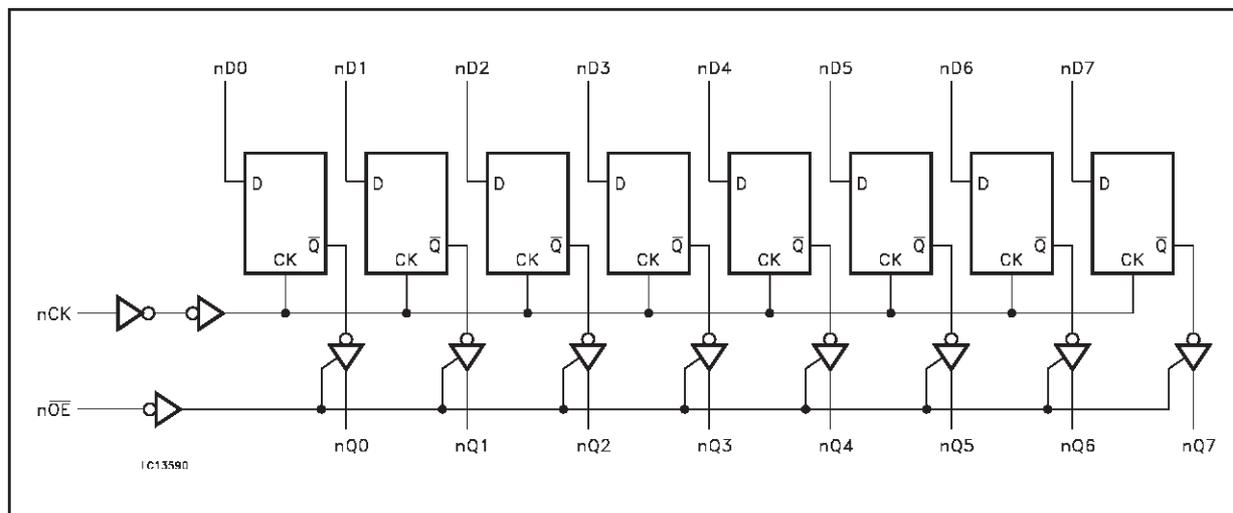


TRUTH TABLE

INPUTS			OUTPUTS
\overline{OE}	CK	D	Q
H	X	X	Z
L		X	NO CHANGE
L		L	L
L		H	H

X : Don't Care
Z : High Impedance

LOGIC DIAGRAM



This logic diagram has not to be used to estimate propagation delays

ABSOLUTE MAXIMUM RATINGS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	-0.5 to +7	V
V_I	DC Input Voltage	-0.5 to $V_{CC} + 0.5$	V
V_O	DC Output Voltage	-0.5 to $V_{CC} + 0.5$	V
I_{IK}	DC Input Diode Current	± 20	mA
I_{OK}	DC Output Diode Current	± 20	mA
I_O	DC Output Current	± 50	mA
I_{CC} or I_{GND}	DC V_{CC} or Ground Current	± 400	mA
T_{stg}	Storage Temperature	-65 to +150	$^{\circ}C$
T_L	Lead Temperature (10 sec)	300	$^{\circ}C$

Absolute Maximum Ratings are those values beyond which damage to the device may occur. Functional operation under these conditions is not implied.

RECOMMENDED OPERATING CONDITIONS

Symbol	Parameter	Value	Unit
V_{CC}	Supply Voltage	2 to 6	V
V_I	Input Voltage	0 to V_{CC}	V
V_O	Output Voltage	0 to V_{CC}	V
T_{op}	Operating Temperature	-55 to 125	$^{\circ}C$
dt/dv	Input Rise and Fall Time $V_{CC} = 3.0, 4.5$ or $5.5V$ (note 1)	8	ns/V

1) V_{IN} from 30% to 70% of V_{CC}

DC SPECIFICATIONS

Symbol	Parameter	Test Condition		Value						Unit	
		V _{CC} (V)		T _A = 25 °C			-40 to 85°C		-55 to 125°C		
				Min.	Typ.	Max.	Min.	Max.	Min.		Max.
V _{IH}	High Level Input Voltage	3.0	V _O = 0.1 V or V _{CC} -0.1V	2.1	1.5		2.1		2.1		V
		4.5		3.15	2.25		3.15		3.15		
		5.5		3.85	2.75		3.85		3.85		
V _{IL}	Low Level Input Voltage	3.0	V _O = 0.1 V or V _{CC} -0.1V		1.5	0.9		0.9		0.9	V
		4.5			2.25	1.35		1.35		1.35	
		5.5			2.75	1.65		1.65		1.65	
V _{OH}	High Level Output Voltage	3.0	I _O =-50 μA	2.9	2.99		2.9		2.9		V
		4.5	I _O =-50 μA	4.4	4.49		4.4		4.4		
		5.5	I _O =-50 μA	5.4	5.49		5.4		5.4		
		3.0	I _O =-12 mA	2.56			2.46		2.46		
		4.5	I _O =-24 mA	3.86			3.76		3.76		
		5.5	I _O =-24 mA	4.86			4.76		4.76		
V _{OL}	Low Level Output Voltage	3.0	I _O =50 μA		0.002	0.1		0.1		0.1	V
		4.5	I _O =50 μA		0.001	0.1		0.1		0.1	
		5.5	I _O =50 μA		0.001	0.1		0.1		0.1	
		3.0	I _O =12 mA			0.36		0.44		0.44	
		4.5	I _O =24 mA			0.36		0.44		0.44	
		5.5	I _O =24 mA			0.36		0.44		0.44	
I _I	Input Leakage Current	5.5	V _I = V _{CC} or GND			± 0.1		± 1		± 1	μA
I _{OZ}	High Impedance Output Leakage Current	5.5	V _I = V _{IH} or V _{IL} V _O = V _{CC} or GND			± 0.5		± 5		± 5	μA
I _{CC}	Quiescent Supply Current	5.5	V _I = V _{CC} or GND			8		80		80	μA
I _{OLD}	Dynamic Output Current (note 1, 2)	5.5	V _{OLD} = 1.65 V max					75		75	mA
I _{OHD}			V _{OHD} = 3.85 V min					-75		-75	mA

1) Maximum test duration 2ms, one output loaded at a time

2) Incident wave switching is guaranteed on transmission lines with impedances as low as 50Ω

AC ELECTRICAL CHARACTERISTICS ($C_L = 50 \text{ pF}$, $R_L = 500 \Omega$, Input $t_r = t_f = 3\text{ns}$)

Symbol	Parameter	Test Condition		Value						Unit	
		V _{CC} (V)		T _A = 25 °C			-40 to 85 °C		-55 to 125 °C		
				Min.	Typ.	Max.	Min.	Max.	Min.		Max.
t _{PLH} t _{PHL}	Propagation Delay Time CK to Q	3.3(*)			5.9	9.8		17.0		17.0	ns
		5.0(**)			4.2	6.5		10.8		10.8	
t _{PZL} t _{PZH}	Output Enable Time	3.3(*)			6.7	11.1		21.2		21.2	ns
		5.0(**)			4.9	7.3		12.1		12.1	
t _{PLZ} t _{PHZ}	Output Disable Time	3.3(*)			6.3	10.0		12.0		12.0	ns
		5.0(**)			4.9	7.6		9.1		9.1	
t _W	CLOCK Pulse Width HIGH or LOW	3.3(*)		2.5	2.0		5.2		5.2		ns
		5.0(**)		2.5	2.0		4.2		4.2		
t _s	Setup Time D to CK, HIGH or LOW	3.3(*)		1.5	1.0		2.5		2.5		ns
		5.0(**)		2.0	1.2		2.5		2.5		
t _h	Hold Time D to CK, HIGH or LOW	3.3(*)		1.0	-0.5		1.5		1.5		ns
		5.0(**)		1.0	-0.5		1.5		1.5		
f _{MAX}	Maximum Clock Frequency	3.3(*)		60	100		60		60		MHz
		5.0(**)		100	120		100		100		

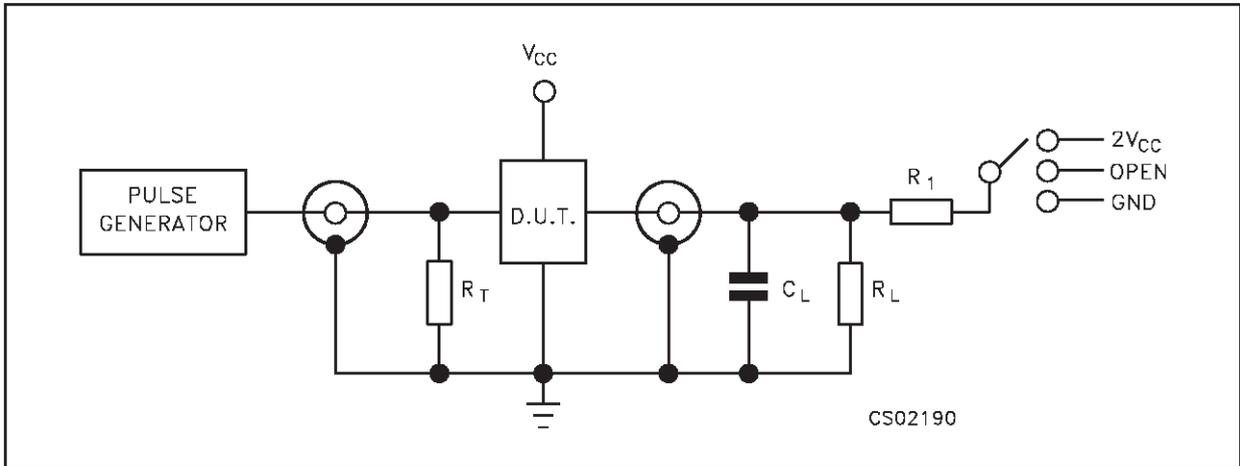
(*) Voltage range is 3.3V ± 0.3V
 (**) Voltage range is 5.0V ± 0.5V

CAPACITIVE CHARACTERISTICS

Symbol	Parameter	Test Condition		Value						Unit	
		V _{CC} (V)		T _A = 25 °C			-40 to 85 °C		-55 to 125 °C		
				Min.	Typ.	Max.	Min.	Max.	Min.		Max.
C _{IN}	Input Capacitance	5.0			3.5						pF
C _{OUT}	Output Capacitance	5.0			11						pF
C _{PD}	Power Dissipation Capacitance (note 1)	5.0	f _{IN} =10MHz		20						pF

1) C_{PD} is defined as the value of the IC's internal equivalent capacitance which is calculated from the operating current consumption without load. (Refer to Test Circuit). Average operating current can be obtained by the following equation. I_{CC(opr)} = C_{PD} × V_{CC} × f_{IN} + I_{CC}/16 (per circuit)

TEST CIRCUIT



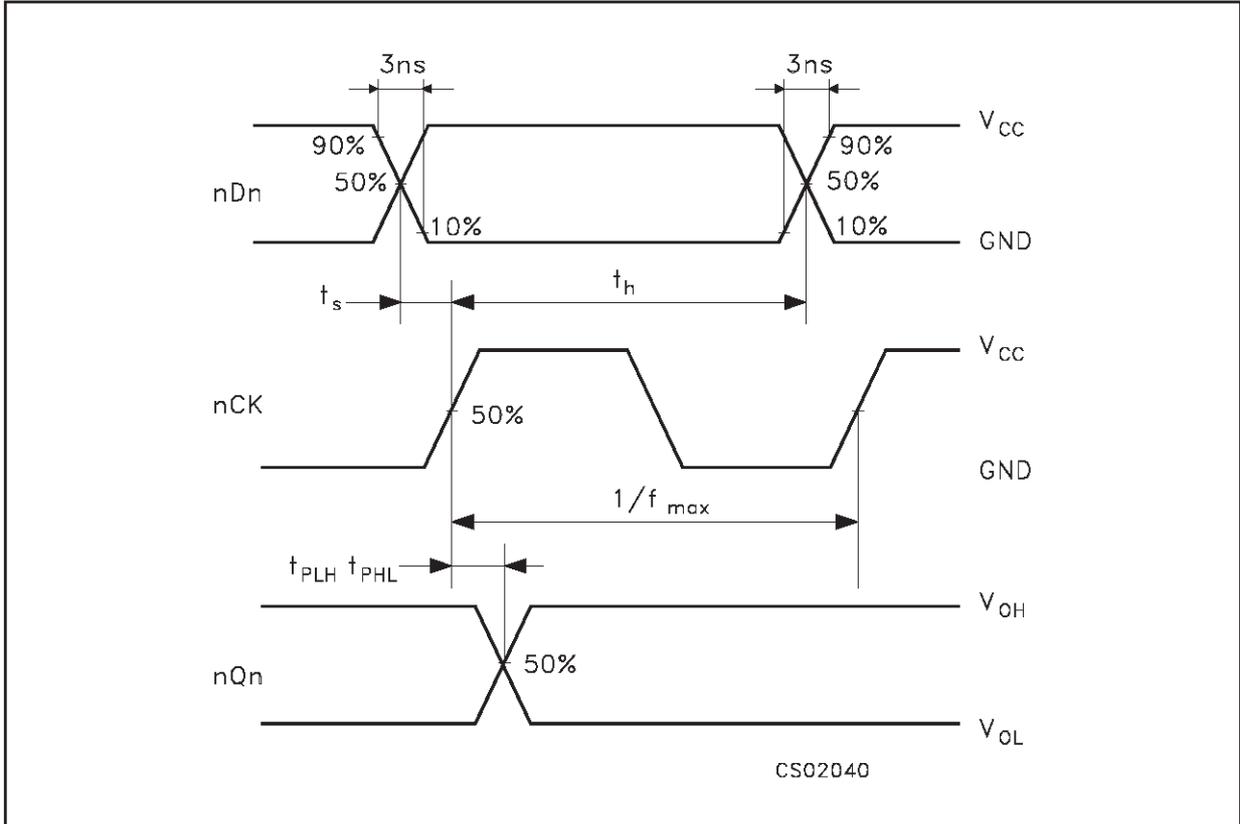
Test	Switch
t_{PLH} , t_{PHL}	Open
t_{PZL} , t_{PLZ}	$2V_{CC}$
t_{PZH} , t_{PHZ}	GND

$C_L = 50\text{pF}$ or equivalent (includes jig and probe capacitance)

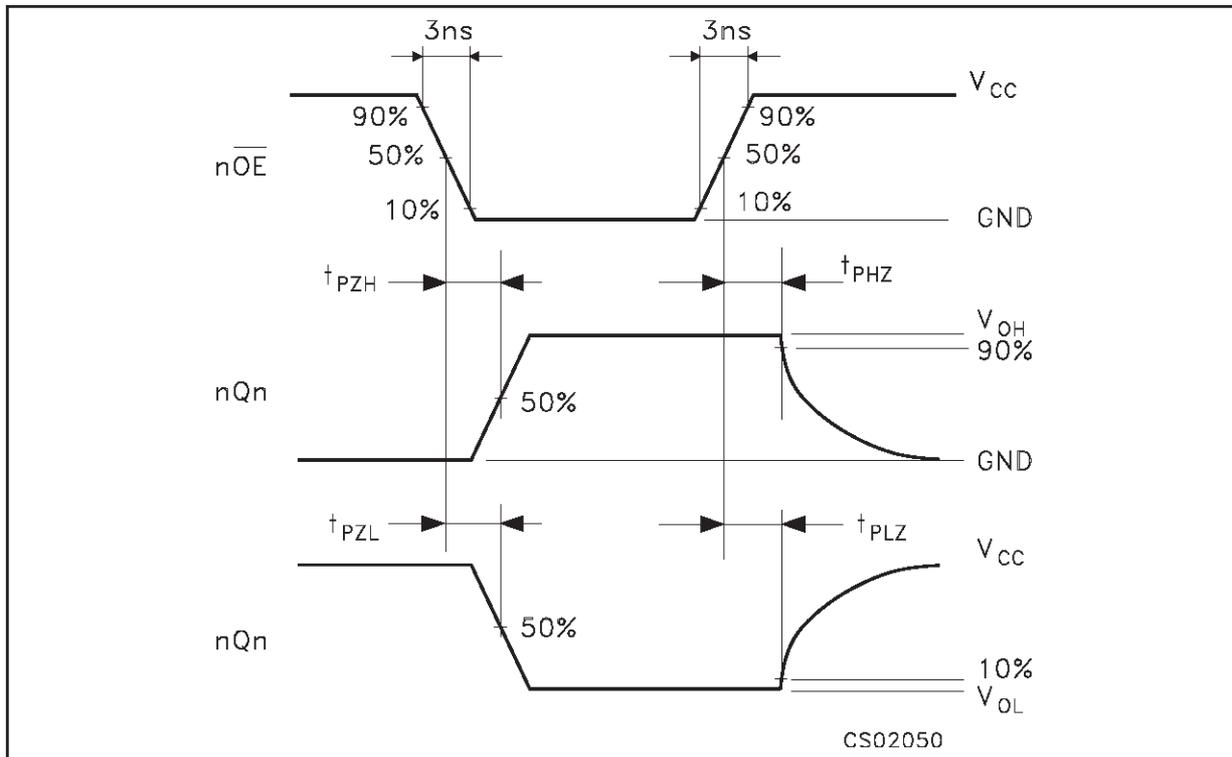
$R_L = R_1 = 500\Omega$ or equivalent

$R_T = Z_{OUT}$ of pulse generator (typically 50Ω)

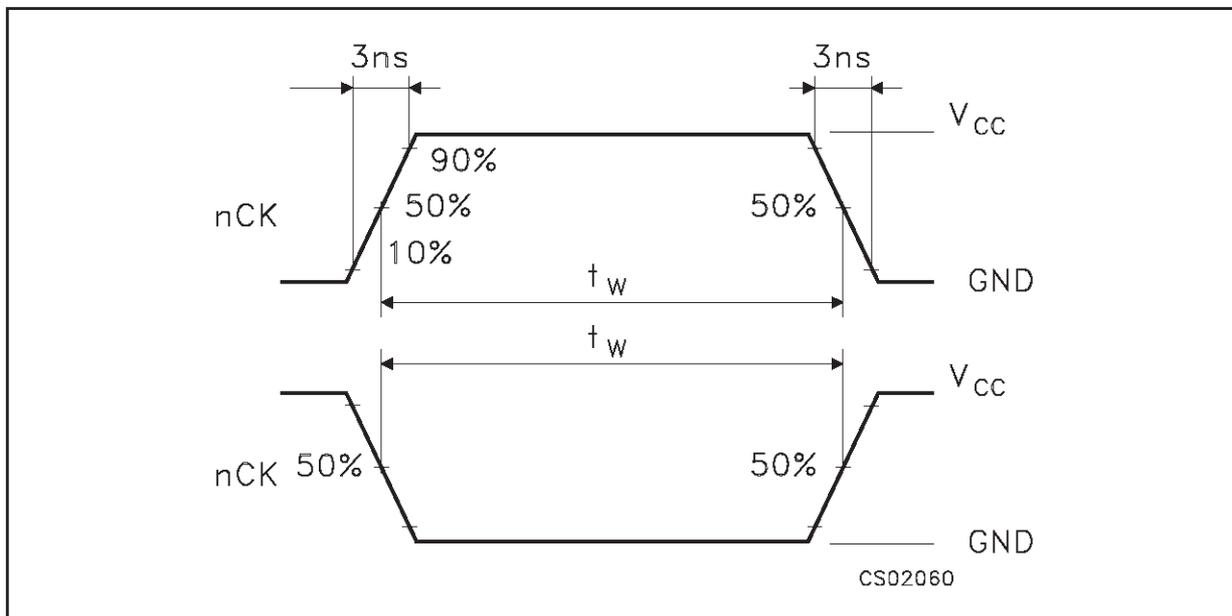
WAVEFORM 1: PROPAGATION DELAYS, SETUP AND HOLD TIMES ($f=1\text{MHz}$; 50% duty cycle)



WAVEFORM 2: OUTPUT ENABLE AND DISABLE TIMES (f=1MHz; 50% duty cycle)

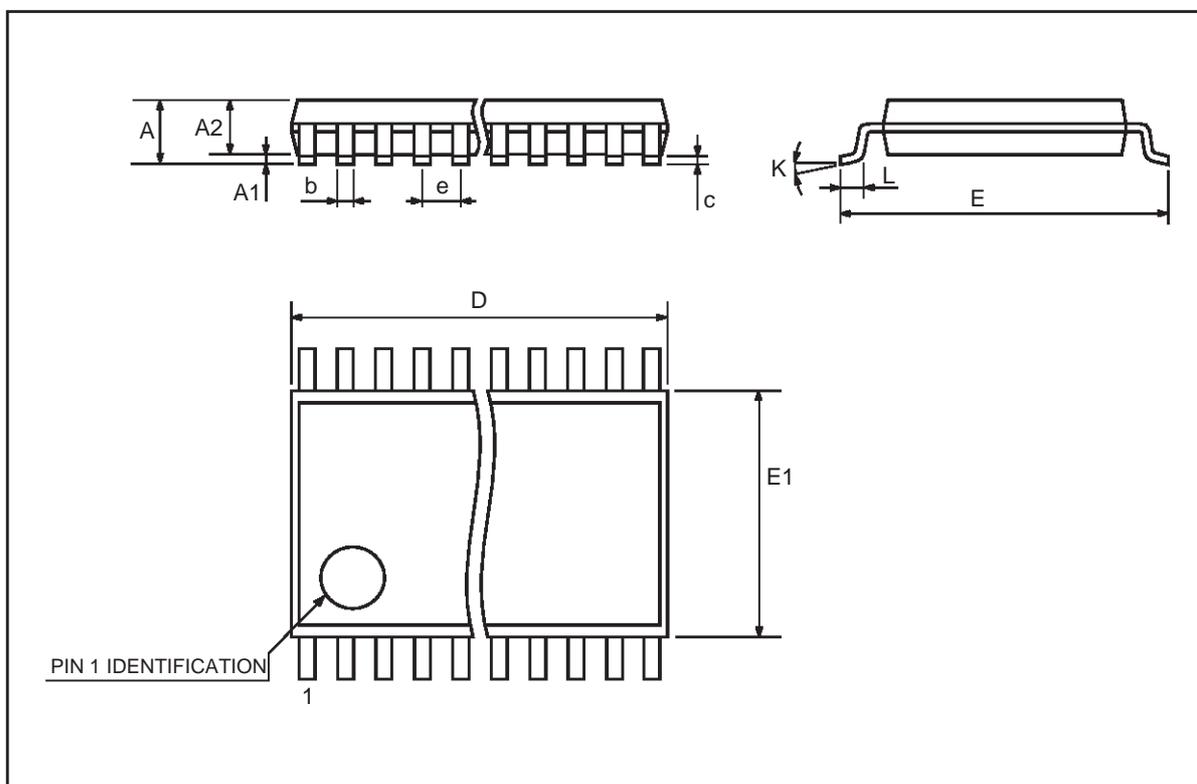


WAVEFORM 3: CLOCK PULSE WIDTHS (f=1MHz; 50% duty cycle)



TSSOP48 MECHANICAL DATA

DIM.	mm			inch		
	MIN.	TYP.	MAX.	MIN.	TYP.	MAX.
A			1.1			0.433
A1	0.05	0.10	0.15	0.002	0.004	0.006
A2	0.85	0.9	0.95	0.335	0.354	0.374
b	0.17		0.27	0.0067		0.011
c	0.09		0.20	0.0035		0.0079
D	12.4	12.5	12.6	0.408	0.492	0.496
E	7.95	8.1	8.25	0.313	0.319	0.325
E1	6.0	6.1	6.2	0.236	0.240	0.244
e		0.5 BSC			0.0197 BSC	
K	0°	4°	8°	0°	4°	8°
L	0.50	0.60	0.70	0.020	0.024	0.028



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