



October 1992  
Revised March 1999

# 74VHC240

## Octal Buffer/Line Driver with 3-STATE Outputs

### General Description

The VHC240 is an advanced high speed CMOS octal bus buffer fabricated with silicon gate CMOS technology. It achieves high speed operation similar to equivalent Bipolar Schottky TTL while maintaining the CMOS low power dissipation. The VHC240 is an inverting 3-STATE buffer having two active-LOW output enables. This device is designed to drive buslines or buffer memory address registers.

An input protection circuit ensures that 0V to 7V can be applied to the input pins without regard to the supply voltage. This device can be used to interface 5V to 3V systems and two supply systems such as battery backup. This circuit prevents device destruction due to mismatched supply and input voltages.

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### Features

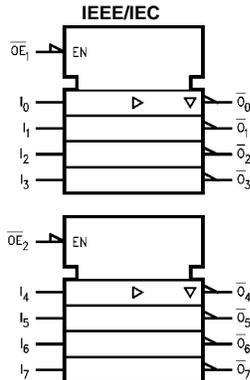
- High Speed:  $t_{PD} = 3.6ns$  (typ) at  $T_A = 25^\circ C$
- Low power dissipation:  $I_{CC} = 4 \mu A$  (max) @  $T_A = 25^\circ C$
- High noise immunity:  $V_{NIH} = V_{NIL} = 28\% V_{CC}$  (min)
- Power down protection is provided on all inputs
- Low noise:  $V_{OLP} = 0.9V$  (max)
- Pin and function compatible with 74HC240

### Ordering Code:

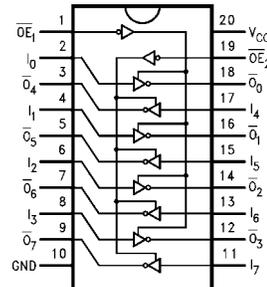
Order Number	Package Number	Package Description
74VHC240M	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
74VHC240SJ	M20D	20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74VHC240MTC	MTC20	20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
74VHC240N	N20A	20-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300" Wide

Surface mount packages are also available on Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

### Logic Symbol



### Connection Diagram



### Pin Descriptions

Pin Names	Description
$\overline{OE}_1, \overline{OE}_2$	3-STATE Output Enable Inputs
$I_0-I_7$	Inputs
$\overline{O}_0-\overline{O}_7$	Outputs 3-STATE Outputs

74VHC240 Octal Buffer/Line Driver with 3-STATE Outputs

74VHC240

### Truth Tables

Inputs		Outputs (Pins 12, 14, 16, 18)
$\overline{OE}_1$	$I_n$	
L	L	H
L	H	L
H	X	Z

Inputs		Outputs (Pins 3, 5, 7, 9)
$\overline{OE}_1$	$I_n$	
L	L	H
L	H	L
H	X	Z

H = HIGH Voltage Level  
L = LOW Voltage Level  
X = Immaterial  
Z = High Impedance

Absolute Maximum Ratings (Note 1)		Recommended Operating Conditions (Note 2)	
Supply Voltage ( $V_{CC}$ )	-0.5V to +7.0V	Supply Voltage ( $V_{CC}$ )	2.0V to 5.5V
DC Input Voltage ( $V_{IN}$ )	-0.5V to +7.0V	Input Voltage ( $V_{IN}$ )	0V to +5.5V
DC Output Voltage ( $V_{OUT}$ )	-0.5V to $V_{CC} + 0.5V$	Output Voltage ( $V_{OUT}$ )	0V to $V_{CC}$
Input Diode Current ( $I_{IK}$ )	-20 mA	Operating Temperature ( $T_{OPR}$ )	-40°C to +85°C
Output Diode Current ( $I_{OK}$ )	±20 mA	Input Rise and Fall Time ( $t_r, t_f$ )	$V_{CC} = 3.3V \pm 0.3V$ 0 ns/V ~ 100 ns/V
DC Output Current ( $I_{OUT}$ )	±25 mA		$V_{CC} = 5.0V \pm 0.5V$ 0 ns/V ~ 20 ns/V
DC $V_{CC}$ /GND Current ( $I_{CC}$ )	±75 mA	<b>Note 1:</b> Absolute Maximum Ratings are values beyond which the device may be damaged or have its useful life impaired. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation outside databook specifications.	
Storage Temperature ( $T_{STG}$ )	-65°C to +150°C	<b>Note 2:</b> Unused inputs must be held HIGH or LOW. They may not float.	
Lead Temperature ( $T_L$ ) (Soldering, 10 seconds)	260°C		

DC Electrical Characteristics									
Symbol	Parameter	$V_{CC}$ (V)	$T_A = 25^\circ C$			$T_A = -40^\circ C$ to $+85^\circ C$		Units	Conditions
			Min	Typ	Max	Min	Max		
$V_{IH}$	HIGH Level Input Voltage	2.0 3.0 – 5.5	1.50			1.50		V	
$V_{IL}$	LOW Level Input Voltage	2.0 3.0 – 5.5			0.50 0.3 $V_{CC}$		0.50 0.3 $V_{CC}$	V	
$V_{OH}$	HIGH Level Output Voltage	2.0	1.9	2.0		1.9		V	$V_{IN} = V_{IH}$ or $V_{IL}$ $I_{OH} = -50 \mu A$
		3.0	2.9	3.0		2.9			
		4.5	4.4	4.5		4.4		V	$I_{OH} = -4 \text{ mA}$ $I_{OH} = -8 \text{ mA}$
		3.0	2.58			2.48			
4.5	3.94			3.80					
$V_{OL}$	LOW Level Output Voltage	2.0		0.0	0.1		0.1	V	$V_{IN} = V_{IH}$ or $V_{IL}$ $I_{OL} = 50 \mu A$
		3.0		0.0	0.1		0.1		
		4.5		0.0	0.1		0.1	V	$I_{OL} = 4 \text{ mA}$ $I_{OL} = 8 \text{ mA}$
		3.0			0.36		0.44		
4.5			0.36		0.44				
$I_{OZ}$	3-STATE Output Off-State Current	5.5			±0.25		±2.5	µA	$V_{IN} = V_{IH}$ or $V_{IL}$ $V_{OUT} = V_{CC}$ or GND
$I_{IN}$	Input Leakage Current	0 – 5.5			±0.1		±1.0	µA	$V_{IN} = 5.5V$ or GND
$I_{CC}$	Quiescent Supply Current	5.5			4.0		40.0	µA	$V_{IN} = V_{CC}$ or GND

Noise Characteristics						
Symbol	Parameter	$V_{CC}$ (V)	$T_A = 25^\circ C$		Units	Conditions
			Typ	Limits		
$V_{OLP}$ (Note 3)	Quiet Output Maximum Dynamic $V_{OL}$	5.0	0.6	0.9	V	$C_L = 50 \text{ pF}$
$V_{OLV}$ (Note 3)	Quiet Output Minimum Dynamic $V_{OL}$	5.0	-0.6	-0.9	V	$C_L = 50 \text{ pF}$
$V_{IHD}$ (Note 3)	Minimum HIGH Level Dynamic Input Voltage	5.0			V	$C_L = 50 \text{ pF}$
$V_{ILD}$ (Note 3)	Maximum LOW Level Dynamic Input Voltage	5.0			V	$C_L = 50 \text{ pF}$

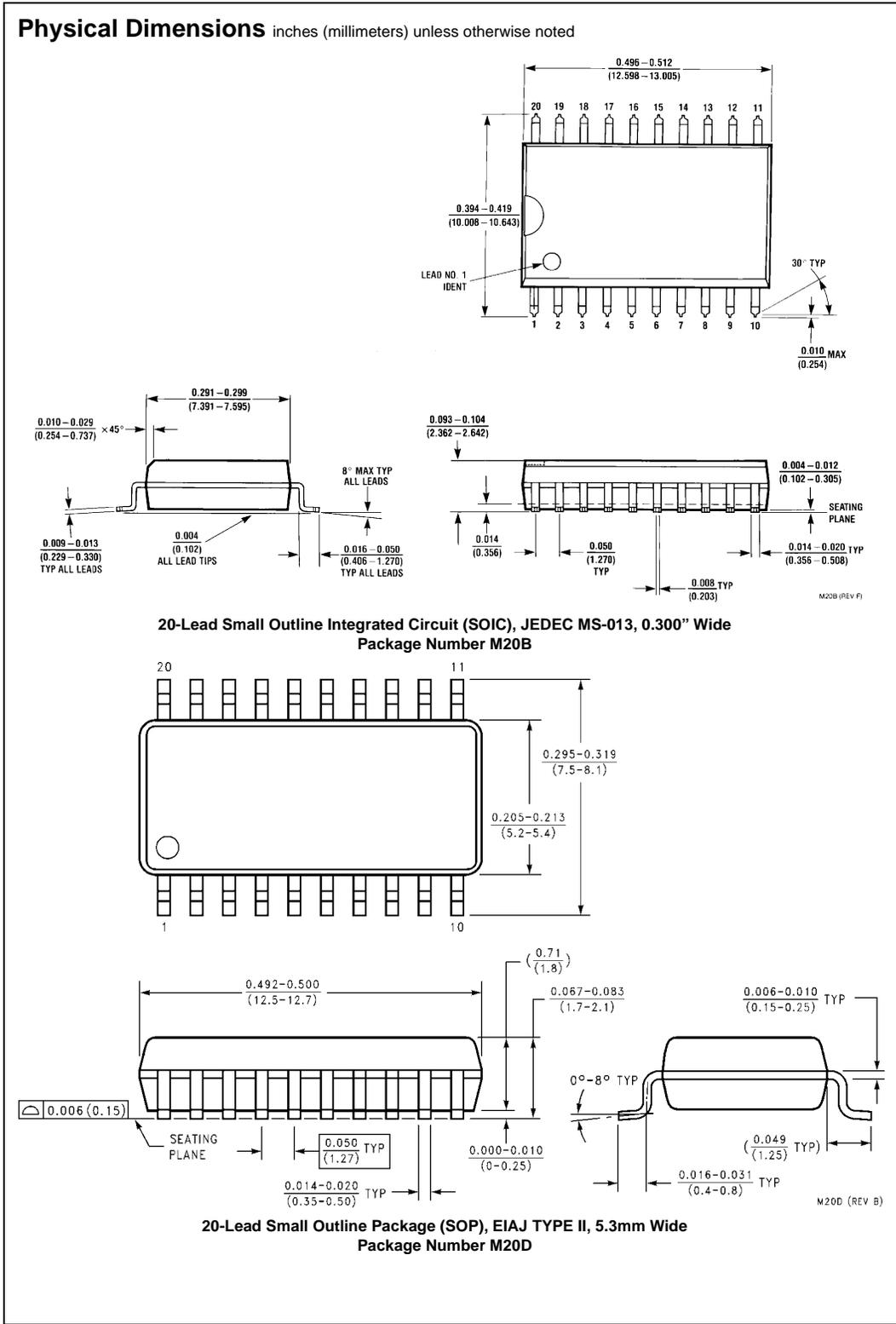
**Note 3:** Parameter guaranteed by design.

74VHC240

AC Electrical Characteristics									
Symbol	Parameter	V <sub>CC</sub> (V)	T <sub>A</sub> = 25°C			T <sub>A</sub> = -40°C to +85°C		Units	Conditions
			Min	Typ	Max	Min	Max		
t <sub>PLH</sub>	Propagation Delay Time	3.3 ± 0.3		5.3	7.5	1.0	9.0	ns	C <sub>L</sub> = 15 pF
t <sub>PHL</sub>				7.8	11.0	1.0	12.5		C <sub>L</sub> = 50 pF
		5.0 ± 0.5		3.6	5.5	1.0	6.5	ns	C <sub>L</sub> = 15 pF
				5.1	7.5	1.0	8.5		C <sub>L</sub> = 50 pF
t <sub>PZL</sub>	3-STATE Output	3.3 ± 0.3		6.6	10.6	1.0	12.5	ns	R <sub>L</sub> = 1 kΩ
t <sub>PZH</sub>	Enable Time	5.0 ± 0.5		9.1	14.1	1.0	16.0		C <sub>L</sub> = 15 pF
				4.7	7.3	1.0	8.5		C <sub>L</sub> = 50 pF
				6.2	9.3	1.0	10.5		C <sub>L</sub> = 50 pF
t <sub>PLZ</sub>	3-STATE Output Disable Time	3.3 ± 0.3		10.3	14.0	1.0	16.0	ns	R <sub>L</sub> = 1 kΩ
t <sub>PHZ</sub>		5.0 ± 0.5	6.7		9.2	1.0	10.5		C <sub>L</sub> = 50 pF
t <sub>OSSLH</sub>	Output to	3.3 ± 0.3			1.5		1.5	ns	(Note 4)
t <sub>OSSLH</sub>	Output Skew	5.0 ± 0.5			1.0		1.0		C <sub>L</sub> = 50 pF
C <sub>IN</sub>	Input Capacitance			4	10		10	pF	V <sub>CC</sub> = Open
C <sub>OUT</sub>	Output Capacitance			6				pF	V <sub>CC</sub> = 5.0V
C <sub>PD</sub>	Power Dissipation Capacitance			17				pF	(Note 5)

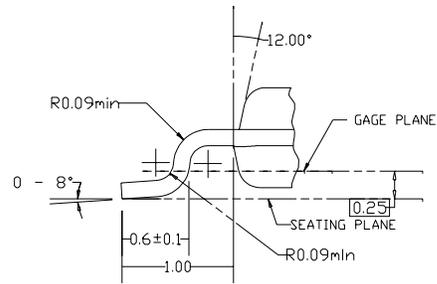
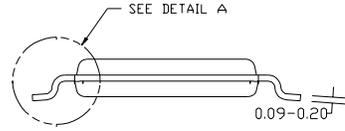
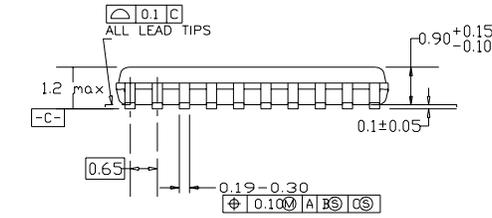
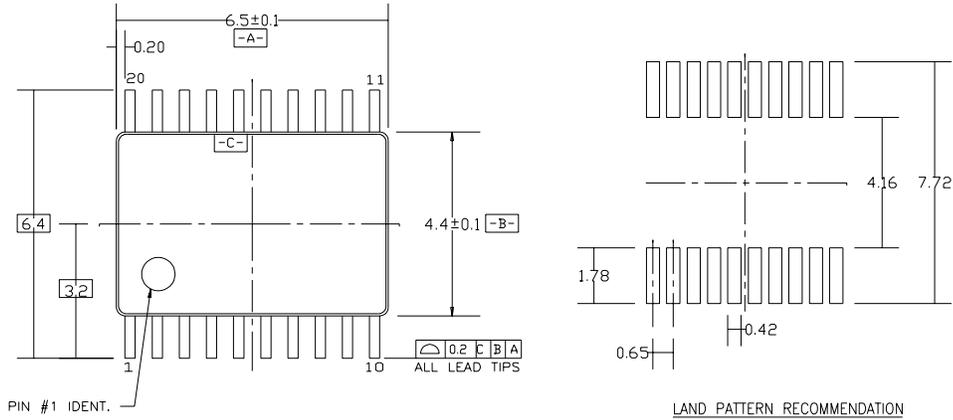
**Note 4:** Parameter guaranteed by design. t<sub>OSSLH</sub> = |t<sub>PLHmax</sub> - t<sub>PLHmin</sub>|; t<sub>OSSLH</sub> = |t<sub>PHLmax</sub> - t<sub>PHLmin</sub>|

**Note 5:** C<sub>PD</sub> is defined as the value of the internal equivalent capacitance which is calculated from the operating current consumption without load. Average operating current can be obtained by the equation: I<sub>CC (opr.)</sub> = C<sub>PD</sub> \* V<sub>CC</sub> \* f<sub>IN</sub> + I<sub>CC</sub>/8 (per bit).



74VHC240

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



DIMENSIONS ARE IN MILLIMETERS

NOTES:

- A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AC, REF NOTE 6, DATE 7/93.
- B. DIMENSIONS ARE IN MILLIMETERS.
- C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLDS FLASH, AND TIE BAR EXTRUSIONS.
- D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

**20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide Package Number MTC20**

