REVISIONS			
LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED
A	Pages 4, 5, and 6, table I, change V_{CM}, CMRR, I_B, I_{IO}, V_{VIO}, C_{IN}, E_N, BGE, BGE/Δt, V_{IH}, I_{IH}, I_{IL}, V_{OH}, V_{OL}, FT, and I_{CC}. Delete T_R and P_D. Page 9, figure 1, case X, change A and A1 dimensions. Page 10, figure 1 - Continued, case Y, change overall package height and delete the dimensions for the distance between top of substrate and top of lid. Change vendor CAGE number. Editorial changes throughout.	91-01-25	Monica L. Poelking
B	Pages 5 and 6, table I, change BZE/Δt, BGE/Δt, and t_a. Pages 12 and 13, correct terminal connections. Inactivated case Y (flat package). Editorial changes throughout.	91-09-20	Monica L. Poelking
C	Add device types 03, 04, and CAGE number 50721. Rewrite entire document.	93-05-11	K. A. Cottongim
D	Changes in accordance with NOR 5962-R139-97.	96-11-25	K. A. Cottongim
E	Changes in table I for device types 03 and 04.	99-03-04	K. A. Cottongim
F	Figure 1; For the case outline X, corrected the dimension R. Added dimension T to case outline X to define the measurement from the edge of the package to the center of the first horizontal pin for all four corners. Figure 1 conversion table, added dimension T. -sld	00-01-05	Raymond Monnin

REV																			
SHEET																			
REV	F	F	F	F	F	F													
SHEET	15	16	17	18	19	20													

REV STATUS OF SHEETS																
REV	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F	F
SHEET	1	2	3	4	5	6	7	8	9	10	11	12	13	14		

PMIC N/A

STANDARD MICROCIRCUIT DRAWING

THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE

AMSC N/A

PREPARED BY
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DRAWING APPROVAL DATE
89-07-24

REVISION LEVEL
F

DEFENSE SUPPLY CENTER COLUMBUS
P. O. BOX 3990
COLUMBUS, OHIO 43216-5000

MICROCIRCUIT, HYBRID, LINEAR, 12-BIT DATA ACQUISITION SYSTEM

SIZE	CAGE CODE	
A	**67268**	**5962-88514**

SHEET 1 OF 20

DSCC FORM 2233
APR 97

5962-E076-00

1. SCOPE

1.1 Scope. This drawing describes device requirements for class H hybrid microcircuits to be processed in accordance with MIL-PRF-38534 and a choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN).

1.2 PIN. The PIN shall be as shown in the following example:

5962-88514	01	X	A
Drawing number	Device type (see 1.2.1)	Case outline (see 1.2.2)	Lead finish (see 1.2.3)

1.2.1 Device type(s). The device type(s) shall identify the circuit function as follows:

Device type	Generic number	Circuit function
01	HS9403B-8	12-bit data acquisition system, 8-channel differential input
02	HS9403B-16	12-bit data acquisition system, 16-channel single-ended input
03	HDAS-8	12-bit data acquisition system, 8-channel differential input
04	HDAS-16	12-bit data acquisition system, 16-channel single-ended input

1.2.2 Case outline(s). The case outline(s) shall be as designated in MIL-STD-1835 and as follows:

Outline letter	Descriptive designator	Terminals	Package style
X	See figure 1	62	Quad package
Y	See figure 1	64	Flat package

1.2.3 Lead finish. The lead finish shall be as specified in MIL-PRF-38534.

1.3 Absolute maximum ratings. 1/

Positive supply voltage range (V_{CC})	-0.5 V dc to +18 V dc
Negative supply voltage range (V_{EE})	+0.5 V dc to -18 V dc
Logic supply voltage range (V_{DD})	-0.5 V dc to +7 V dc
Analog input channels	±35 V dc 2/
Digital inputs	-0.5 V dc to +7 V dc
Power dissipation (P_D)	2 W
Thermal resistance (θ_{JC})	30°C/W
Thermal resistance (θ_{JA})	45°C/W
Lead temperature (soldering, 10 seconds)	+300°C
Storage temperature range	-65°C to +150°C
Junction temperature (T_J)	+175°C

1.4 Recommended operating conditions.

Positive supply voltage range (V_{CC})	+14.5 V dc to +15.5 V dc
Negative supply voltage range (V_{EE})	-14.5 V dc to -15.5 V dc
Logic supply voltage range (V_{DD})	+4.5 V dc to +5.5 V dc
Ambient operating temperature range (T_A)	-55°C to +125°C

1/ Stresses above the maximum ratings may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
2/ ±20 V in power off condition.

2. APPLICABLE DOCUMENTS

2.1 Government specifications, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solitation.

SPECIFICATION

DEPARTMENT OF DEFENSE

MIL-PRF-38534 - Hybrid Microcircuits, General Specification for.

STANDARDS

DEPARTMENT OF DEFENSE

MIL-STD-883 - Test Method Standard Microcircuits.
MIL-STD-973 - Configuration Management.
MIL-STD-1835 - Interface Standard for Microcircuit Case Outlines.

HANDBOOK

DEPARTMENT OF DEFENSE

MIL-HDBK-103 - List of Standard Microcircuit Drawings (SMD's)
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, and handbooks are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

3. REQUIREMENTS

3.1 Item requirements. The individual item performance requirements for device class H shall be in accordance with MIL-PRF-38534. Compliance with MIL-PRF-38534 may include the performance of all tests herein or as designated in the device manufacturer's Quality Management (QM) plan or as designated for the applicable device class. Therefore, the tests and inspections herein may not be performed for the applicable device class (see MIL-PRF-38534). Futhermore, the manufacturers may take exceptions or use alternate methods to the tests and inspections herein and not perform them. However, the performance requirements as defined in MIL-PRF-38534 shall be met for the applicable device class.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38534 and herein.

3.2.1 Case outline(s). The case outline(s) shall be in accordance with figure 1 and 1.2.2 herein.

3.2.2 Functional diagram. The functional diagram shall be as specified on figure 2.

3.2.3 Terminal connections. The terminal connections shall be as specified on figure 3.

3.2.4 Timing diagram. The timing diagram shall be as specified on figure 4.

3.3 Electrical performance characteristics. Unless otherwise specified herein, the electrical performance characteristics are as specified in table I and shall apply over the full specified operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking of device(s). Marking of device(s) shall be in accordance with MIL-PRF-38534. The device shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's vendor similar PIN may also be marked as listed in QML-38534.

3.6 Data. In addition to the general performance requirements of MIL-PRF-38534, the manufacturer of the device described herein shall maintain the electrical test data (variables format) from the initial quality conformance inspection group A lot sample, for each device type listed herein. Also, the data should include a summary of all parameters manually tested, and for those which, if any, are guaranteed. This data shall be maintained under document revision level control by the manufacturer and be made available to the preparing activity (DSCC-VA) upon request.

3.7 Certificate of compliance. A certificate of compliance shall be required from a manufacturer in order to supply to this drawing. The certificate of compliance (original copy) submitted to DSCC-VA shall affirm that the manufacturer's product meets the performance requirements of MIL-PRF-38534 and herein.

3.8 Certificate of conformance. A certificate of conformance as required in MIL-PRF-38534 shall be provided with each lot of microcircuits delivered to this drawing.

4. QUALITY ASSURANCE PROVISIONS

4.1 Sampling and inspection. Sampling and inspection procedures shall be in accordance with MIL-PRF-38534 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein.

4.2 Screening. Screening shall be in accordance with MIL-PRF-38534. The following additional criteria shall apply:

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to either DSCC-VA or the acquiring activity upon request. Also, the test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

(2) T_A as specified in accordance with table I of method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table II herein, except interim electrical parameter tests prior to burn-in are optional at the discretion of the manufacturer.

TABLE I. Electrical performance characteristics.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
ANALOG INPUTS							
Input voltage range	V_{IN}	Unipolar 2/ unipolar V_{IN} = 0 to +5 V	1, 2, 3	All	0 0	10 10	mV V
		Bipolar Bipolar V_{IN} = -10 V to +10 V	1, 2, 3	All	0 0	±10 ±10	mV V
Common mode voltage range	V_{CM}	3/	1, 2, 3	All	±11		V
Common mode rejection ratio	CMRR	G = 1 (10 kHz) 3/	4, 5, 6	01, 02	-74		dB
				03, 04	-65		
		G = 1000 (60 Hz) 3/	4, 5, 6	01, 02	-110		
				03, 04	-65		
Input bias current	I_{IB}	3/	1	All		200	pA
			2, 3	All		20	nA
Input offset current	I_{IO}	3/	1	All		100	pA
			2, 3	All		15	nA
Input offset voltage	V_{IO}	Input = 0 V 3/	1, 2, 3	All		5	mV
Input capacitance	C_{IN}	Off channel 3/	4	All		10	pF
		On channel 3/		01		50	
				02		100	
Voltage noise	En	G = 1 3/	4, 5, 6	All		150	µV(RMS)
		G = 1000 3/				1.62	
ACCURACY							
Nonlinearity	NL	End-point method 4/	1	01,02	-0.5	+0.5	LSB
			2, 3		-1	+1	
			4	03,04	-0.99	+0.99	
			5, 6		-1.5	+1.5	
Differential nonlinearity	DNL	4/	1	01,02	-0.5	+0.5	LSB
			2, 3		-1	+1	
			4	03,04	-0.99	+0.99	
			5, 6		-1.5	+1.5	

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ $-55°C \le T_A \le +125°C$ unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
ACCURACY - Continued.							
Unipolar offset error	UOE	0 to 10 V range (000000000001)	1	01,02	-0.1	+0.1	% FSR
			4	03,04	-0.1	+0.1	
Unipolar offset error drift	ΔUOE/Δt	0 to 10 V range (000000000001)	2, 3	01,02	-7	+7	ppm of FSR/°C
			5, 6	03,04	-20	+20	
Bipolar zero error	BZE	-10 V to +10 V range (100000000000)	1	01,02	-0.1	+0.1	% FSR
			4	03,04	-0.1	+0.1	
Bipolar zero error drift	BZE/Δt	-10 V to +10 V range (100000000000)	2, 3	01,02	-2.5	+2.5	ppm of FSR/°C
			5, 6	03,04	-2.5	+2.5	
Bipolar gain error	BGE	-10 V to +10 V range (000000000001) (111111111111)	1	01,02	-0.2	+0.2	%
			4	03,04	-0.2	+0.2	
Bipolar gain error drift	BGE/Δt	-10 V to +10 V range (000000000001) (111111111111)	2, 3	01, 02	-20	+20	ppm/°C
			5, 6	03, 04	-40	+40	
Power supply rejection ratio	+PSRR	(All 0's and all 1's) $V_S = V_{CC} \pm 0.5$ V, $V_S = V_{DD} \pm 0.5$ V	1, 2, 3	All		.005 .005	%/%
	-PSRR	$V_S = V_{EE} \pm 0.5$ V				.005	
	REFSRR	+10 V internal ref				.01	
Resolution	RES		1, 2, 3	All	12		bits
DIGITAL INPUTS							
Input voltage (high)	V_{IH}	Load = 40 µA	1, 2, 3	All	2.4	5.5	V
Input voltage (low)	V_{IL}	Load = -0.8 mA	1, 2, 3	All	0	0.8	V
Input current (high)	I_{IH}	V_{IN} = 2.0 V, logic "1"	1, 2, 3	All		40	µA
Input current (low)	I_{IL}	V_{IN} = 0 V, logic "0"	1, 2, 3	All	-0.8		mA
DIGITAL OUTPUTS							
Output voltage (high)	V_{OH}	I_{OH} = -40 µA (1 TTL load)	1, 2, 3	All	2.4		V
Output voltage (low)	V_{OL}	I_{OL} = +1.6 mA (1 TTL load)	1, 2, 3	All		0.4	V

See footnotes at end of table.

TABLE I. Electrical performance characteristics - Continued.

Test	Symbol	Conditions 1/ -55°C ≤ T_A ≤ +125°C unless otherwise specified	Group A subgroups	Device type	Limits		Unit
					Min	Max	
DYNAMIC CHARACTERISTICS							
S/H acquisition time	t_a	10 V step settling to 0.01% FSR See figure 4 3/	4, 5, 6	All		10	µs
A/D conversion time	t_c	See figure 4	4	All		10	µs
			5, 6			15	
Feedthrough	FT	Analog input = 20 Vpp at 1 kHz 3/	4, 5, 6	All	-.01		%
Strobe command pulse width	t_{pw}/strobe	See figure 4 3/	9, 10, 11	All	40		ns
Setup time, digital inputs to strobe	t_s/strobe	See figure 4 3/	9, 10, 11	All	50		ns
Hold time, digital inputs from strobe	t_h/strobe	See figure 4 3/	9, 10, 11	All	50		ns
$\overline{\text{Enable}}$ three-state to valid	t_{t-s}/to $_{-v}$	See figure 4 3/	9, 10, 11	All	40		ns
$\overline{\text{Enable}}$ valid to three-state	t_{t-s}/to $_{t-s}$	See figure 4 3/	9, 10, 11	All	30		ns
POWER SUPPLIES							
Quiescent supply current (positive)	I_{CC}	V_{CC} = +15.5 V, no load	1, 2, 3	All		+60	mA
Quiescent supply current (negative)	I_{EE}	V_{EE} = -15.5 V, no load	1, 2, 3	All		-68	mA
Quiescent supply current (logic)	I_{DD}	V_{DD} = +5.5 V, no load	1, 2, 3	All		+32	mA
Power dissipation	P_D		1, 2, 3	All		2	W

1/ Unless otherwise specified, the following conditions apply:
V_{CC} = +15 V dc, V_{EE} = -15 V dc, V_{DD} = +5 V dc
Input logic "0" = +0.8 V dc
Input logic "1" = +2.0 V dc
Output logic "0" = +0.4 V dc
Output logic "1" = +2.5 V dc
VFSR = 20 V

2/ Selectable with proper gain range.

3/ Parameter shall be tested as part of device initial characterization and after design and process changes. Parameter shall be guaranteed to limits specified in table I for all lots not specifically tested.

4/ Tested at major carries and sums only.

Case outline X.

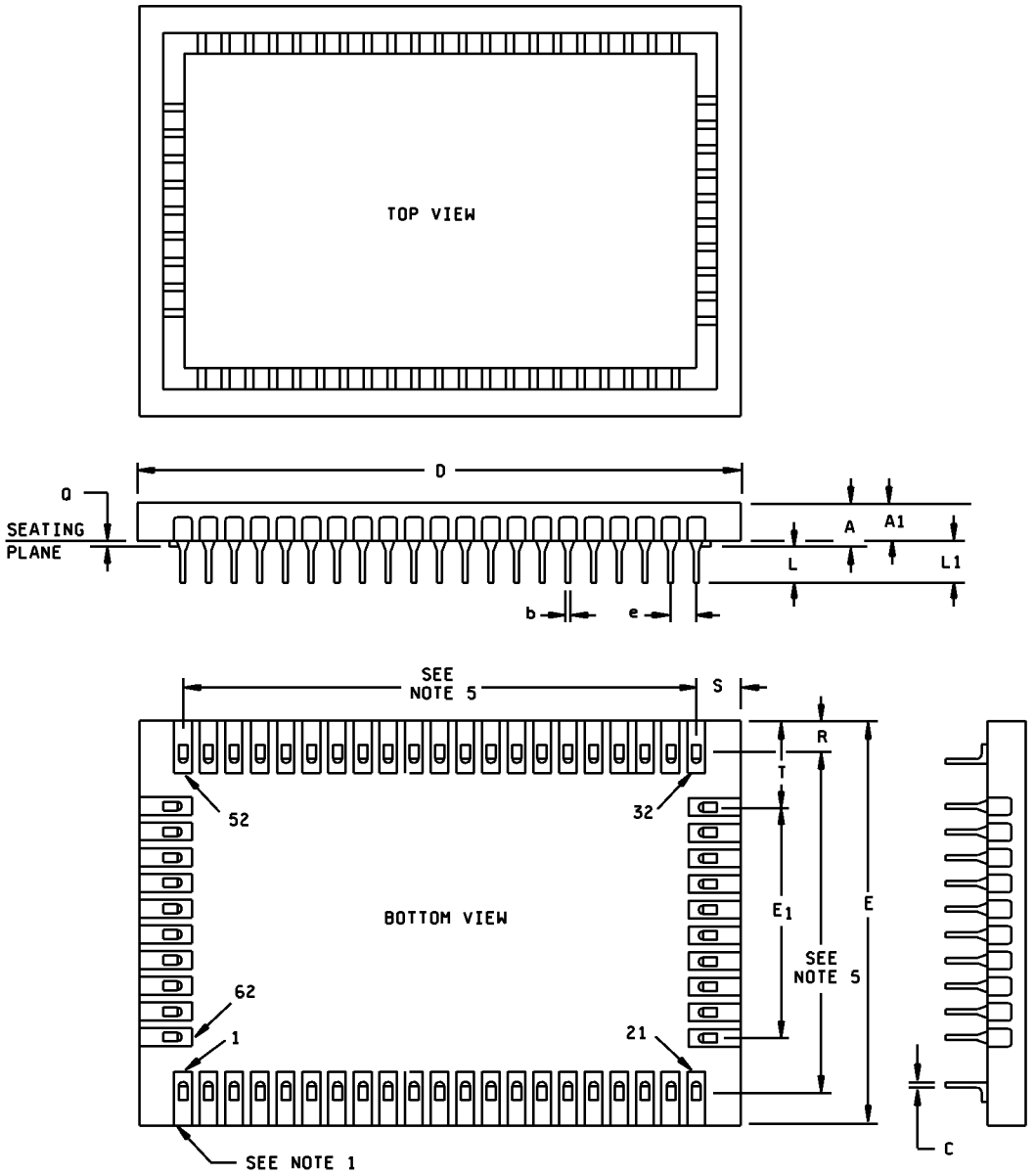


FIGURE 1. Case outlines.

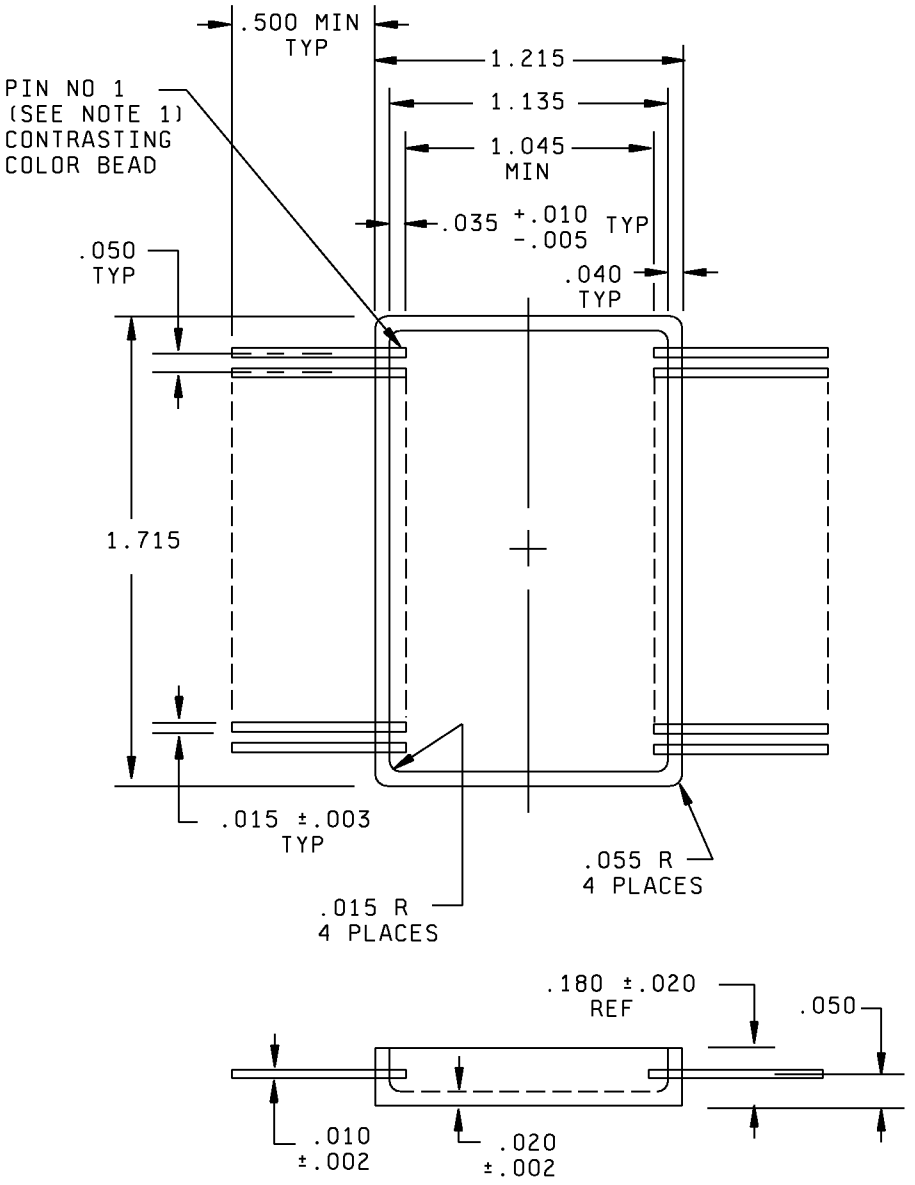
Case outline X - Continued.

Symbol	Dimensions				Notes
	Inches		Millimeters		
	Min	Max	Min	Max	
A	.170	.220	4.32	5.59	
A1	.145	.175	3.68	4.45	
b	.016	.021	0.41	0.53	10
C	.009	.015	0.23	0.38	10
D	2.227	2.323	57.84	59.00	5
E	1.300	1.500	33.02	38.10	5
E_1	1.09	1.11	27.7	28.2	9
e	.100 BSC		2.54 BSC		7, 11
L	.160	.210	4.06	5.33	
L1	.185	.245	4.70	6.22	
Q	.025	.045	0.64	1.14	6
R	.130	.170	3.30	4.32	8
S	.085	.115	2.16	2.92	8
T	.230	.270	5.84	6.86	8

NOTES:
1. Pin 1 is identified by the ESD triangle(s) marked on top of package.
2. Dimensions are in inches.
3. Metric equivalents are given for general information only.
4. The manufacturer's identification shall not be used as pin one identification mark.
5. This dimension allows for off-center lid overrun.
6. Dimension Q shall be measured from the seating plane to the base plane.
7. The basic pin spacing is .100 (2.54 mm) between center lines. Each pin center line shall be located within ±.010 (0.25 mm) of its exact position to pins 1 and 52.
8. Applies to all four corners (leads 1, 21, 32, and 52).
9. E_1 shall be measured at the center line of the leads.
10. All leads: Increase maximum limit by .003 (0.08 mm) measured at the center of the flat, when finish A or B is applied.
11. Twenty-one spaces.
12. Leads in true position within .010R (0.25 mm) at MMC at seating plane.

FIGURE 1. Case outlines - Continued.

Case outline Y.



Inches	mm
.002	0.05
.003	0.08
.005	0.13
.010	0.25
.015	0.38
.020	0.50
.035	0.89
.040	1.02
.050	1.27
.055	1.40
.180	4.57
.500	12.70
1.045	26.54
1.135	28.83
1.215	30.86
1.715	43.56

NOTES:
1. Pin number one to be contrasting color bead from other beads.
2. Dimensions are in inches.
3. Metric equivalents are given for general information only.
4. Hermeticity 1 x 10^{-8} cc/s minimum.

FIGURE 1. Case outlines - Continued.

Device types 01 and 02

Case outline X

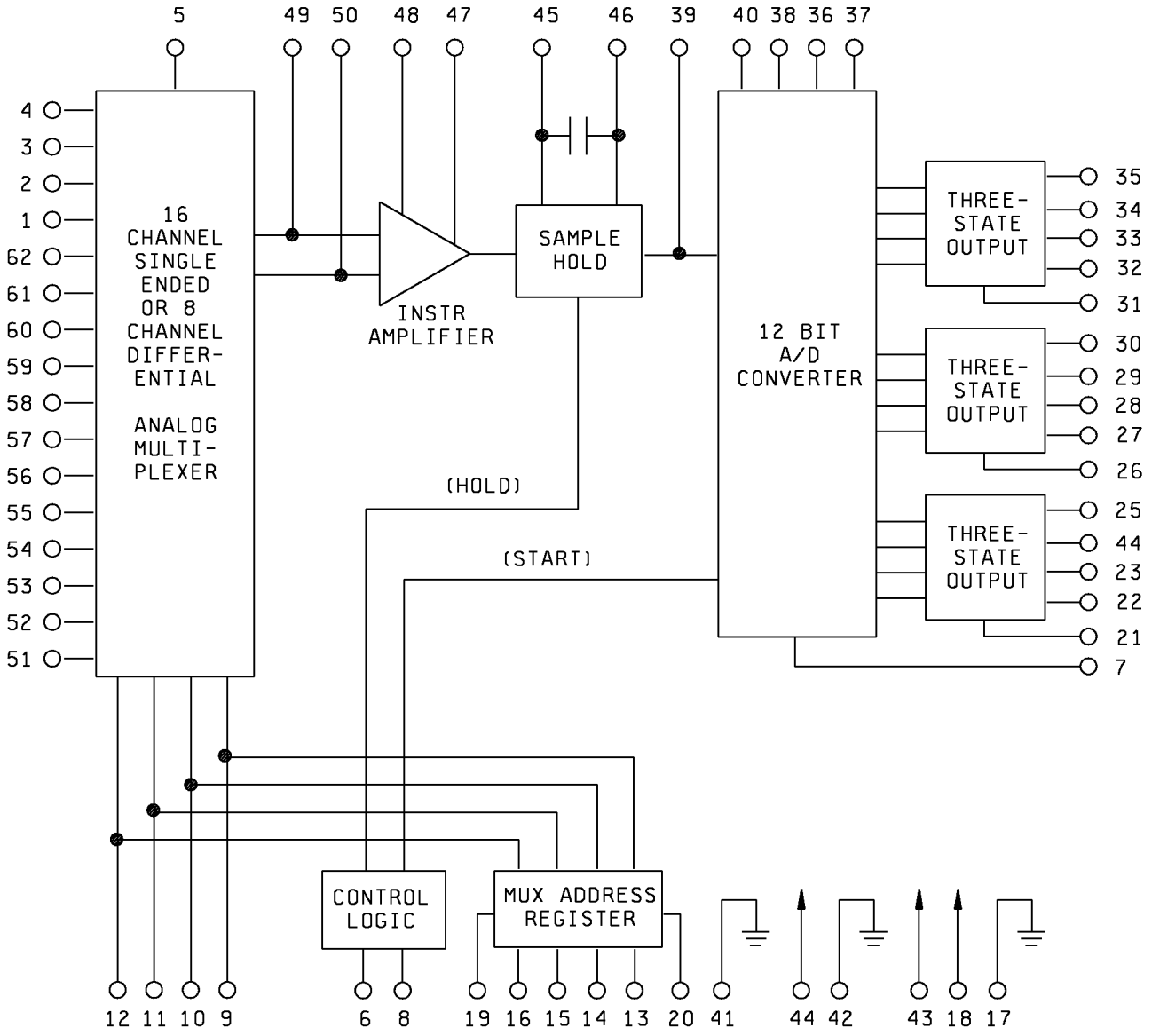


FIGURE 2. Functional diagram.

STANDARDIZED MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE A		5962-88514
		REVISION LEVEL F	SHEET 11

Device types 03 and 04

Case outline X

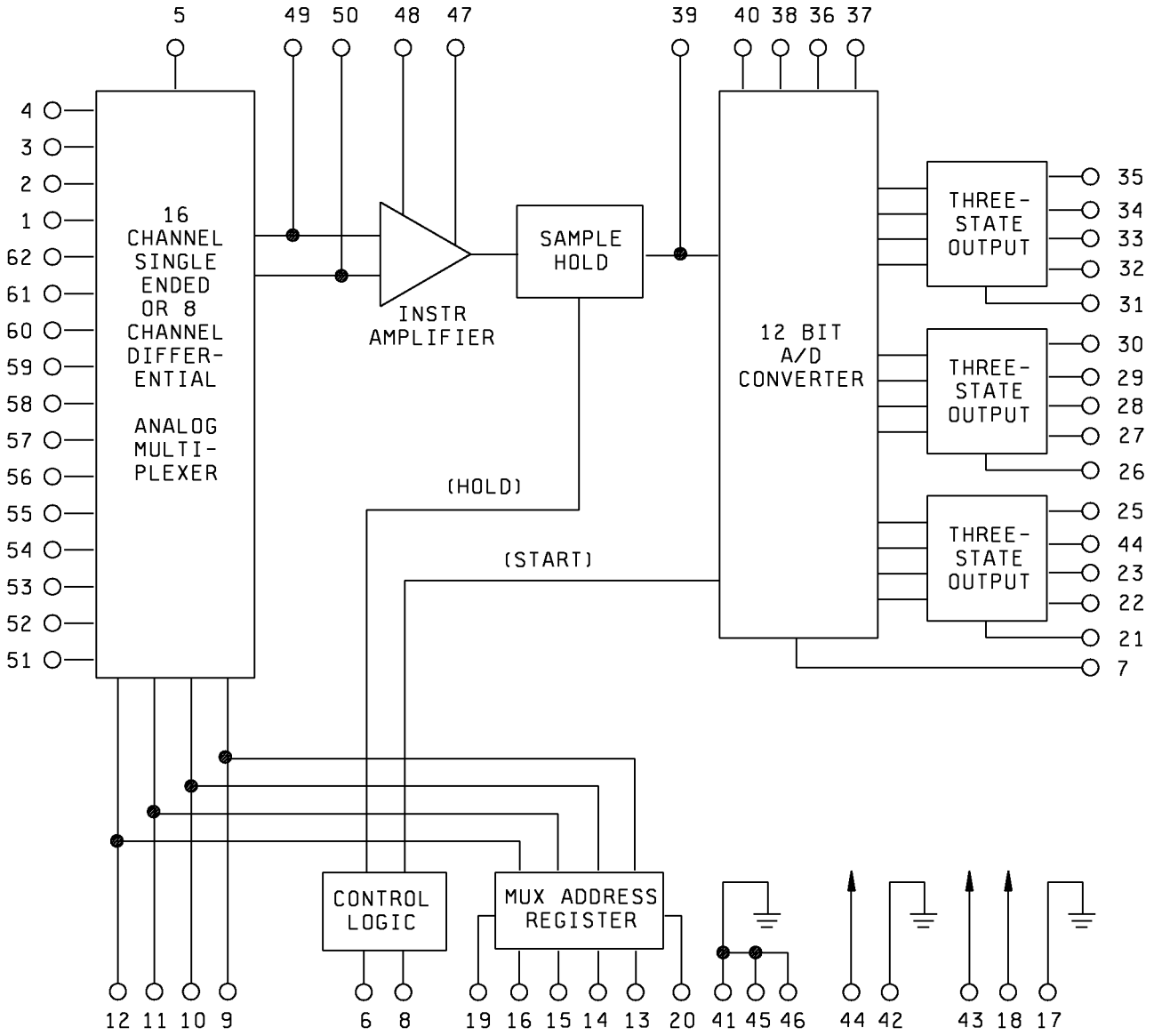


FIGURE 2. Functional diagram - Continued.

STANDARDIZED MICROCIRCUIT DRAWING DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000	SIZE A		5962-88514
		REVISION LEVEL F	SHEET 12

Device types	01 and 03	02 and 04
Case outline	X	X
Terminal number	Terminal symbol	
1	CH 3(+) IN	CH 3 IN
2	CH 2(+) IN	CH 2 IN
3	CH 1(+) IN	CH 1 IN
4	CH 0(+) IN	CH 0 IN
5	MUX ENABLE	MUX ENABLE
6	R DELAY	R DELAY
7	$\overline{EOC}$	$\overline{EOC}$
8	STROBE	STROBE
9	A8	A8
10	A4	A4
11	A2	A2
12	A1	A1
13	RA8	RA8
14	RA4	RA4
15	RA2	RA2
16	RA1	RA1
17	DIGITAL GND	DIGITAL GND
18	V_{DD}	V_{DD}
19	$\overline{LOAD}$	$\overline{LOAD}$
20	$\overline{CLEAR}$	$\overline{CLEAR}$
21	ENABLE (9-12)	ENABLE (9-12)
22	BIT 12 OUT (LSB)	BIT 12 OUT (LSB)
23	BIT 11 OUT	BIT 11 OUT
24	BIT 10 OUT	BIT 10 OUT
25	$\overline{BIT\ 9\ OUT}$	$\overline{BIT\ 9\ OUT}$
26	ENABLE (5-8)	ENABLE (5-8)
27	BIT 8 OUT	BIT 8 OUT
28	BIT 7 OUT	BIT 7 OUT
29	BIT 6 OUT	BIT 6 OUT
30	$\overline{BIT\ 5\ OUT}$	$\overline{BIT\ 5\ OUT}$
31	ENABLE (1-4)	ENABLE (1-4)

FIGURE 3. Terminal connections.

Device types	01 and 03	02 and 04
Case outline	X	X
Terminal number	Terminal symbol	
32	BIT 4 OUT	BIT 4 OUT
33	BIT 3 OUT	BIT 3 OUT
34	BIT 2 OUT	BIT 2 OUT
35	BIT 1 OUT (MSB)	BIT 1 OUT (MSB)
36	GAIN ADJ	GAIN ADJ
37	OFFSET ADJ	OFFSET ADJ
38	BIPOLAR INPUT	BIPOLAR INPUT
39	SAMPLE/HOLD OUT	SAMPLE/HOLD OUT
40	+10 V REF OUT	+10 V REF OUT
41	ANALOG SIGNAL GND	ANALOG SIGNAL GND
42	ANALOG POWER GND	ANALOG POWER GND
43	V_{CC}	V_{CC}
44	V_{EE}	V_{EE}
45	1/	1/
46	2/	2/
47	R GAIN LOW	R GAIN LOW
48	R GAIN HIGH	R GAIN HIGH
49	AMP IN HIGH	AMP IN HIGH
50	AMP IN LOW	AMP IN LOW
51	CH 7 (-)IN	CH 15 IN
52	CH 6 (-)IN	CH 14 IN
53	CH 5 (-)IN	CH 13 IN
54	CH 4 (-)IN	CH 12 IN
55	CH 3 (-)IN	CH 11 IN
56	CH 2 (-)IN	CH 10 IN
57	CH 1 (-)IN	CH 9 IN
58	CH 0 (-)IN	CH 8 IN
59	CH 7 (+)IN	CH 7 IN
60	CH 6 (+)IN	CH 6 IN
61	CH 5 (+)IN	CH 5 IN
62	CH 4 (+)IN	CH 4 IN

NOTES:
1/ Pin 45 for device types 01 and 02 is C HOLD HIGH. Pin 45 for device types 03 and 04 is ANALOG SIGNAL GND.
2/ Pin 46 for device types 01 and 02 is C HOLD LOW. Pin 46 for device types 03 and 04 is ANALOG SIGNAL GND.

FIGURE 3. Terminal connections - Continued.

Device type	02	Device type	02
Case outline	Y	Case outline	Y
Terminal number	Terminal symbol	Terminal number	Terminal symbol
1	BIT 4	17	RA1
2	$\overline{EN}$ 1-4	18	RA2
3	BIT 5	19	RA4
4	BIT 6	20	RA8
5	BIT 7	21	A1
6	BIT 8	22	A2
7	$\overline{EN}$ 5-8	23	A4
8	BIT 9	24	A8
9	BIT 10	25	$\overline{STROBE}$
10	BIT 11	26	$\overline{EOC}$
11	BIT 12 (LSB)	27	R DELAY
12	$\overline{EN}$ 9-12	28	MUX ENABLE
13	$\overline{CLEAR}$	29	CH 0
14	$\overline{LOAD}$	30	CH1
15	+5 V	31	CH2
16	DIGITAL GND	32	CH3

FIGURE 3. Terminal connections - Continued.

Device type	02	Device type	02
Case outline	Y	Case outline	Y
Terminal number	Terminal symbol	Terminal number	Terminal symbol
33	CH 4	49	C HOLD LOW
34	CH 5	50	C HOLD HIGH
35	CH 6	51	-15 V
36	CH 7	52	+15 V
37	CH 8	53	ANALOG POWER GND
38	CH 9	54	ANALOG POWER GND
39	CH 10	55	ANALOG SIGNAL GND
40	CH 11	56	ANALOG SIGNAL GND
41	CH 12	57	+10 V REF OUT
42	CH 13	58	S/H OUTPUT
43	CH 14	59	OFFSET ADJUST
44	CH 15	60	BIPOLAR INPUT
45	AMP IN LOW	61	GAIN ADJUST
46	AM IN HIGH	62	BIT 1 (MSB)
47	R GAIN HIGH	63	BIT 2
48	R GAIN LOW	64	BIT 3

FIGURE 3. Terminal connections - Continued.

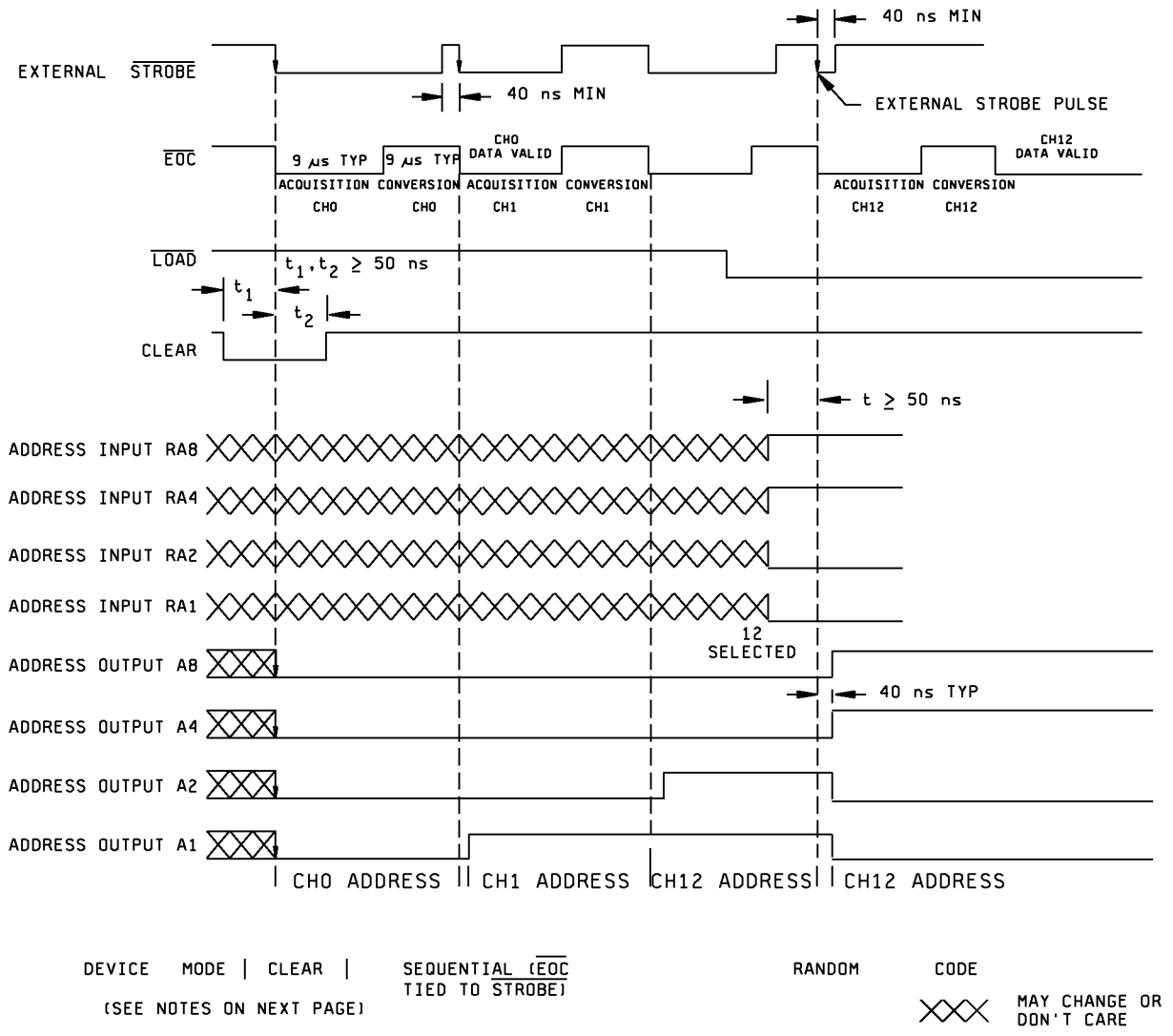


FIGURE 4. Timing diagram.

NOTES:

1. $\overline{\text{STROBE}}$ "H" or "L" initiates acquisition and conversion of analog signal.
2. $\overline{\text{EOC}}$ "H" indicates conversion in process.
   "L" indicates conversion complete.
3. $\overline{\text{LOAD}}$ "L" will allow random address mode. Acquisition and conversion will be accomplished on channel selected at address inputs. "H" will cause sequential address mode. Acquisition and conversion will be accomplished on analog input channels in sequence. $\overline{\text{LOAD}}$ "L" will be initiated on falling transition of $\overline{\text{STROBE}}$ pulse.
4. CLEAR "H" prevents $\overline{\text{STROBE}}$ pulse from causing address change.
   "L" allows next $\overline{\text{STROBE}}$ pulse to reset MUX ADDRESS to CHO overriding $\overline{\text{LOAD}}$ command.
5. When the $\overline{\text{EOC}}$ goes "H" indicating that an A/D conversion has begun, the MSB goes "L" and all other bits go "H". Output bits are set to their final state on succeeding falling $\overline{\text{STROBE}}$ pulse.
6. Conversion time is defined as the time $\overline{\text{EOC}}$ is "H".
7. Once an acquisition and conversion cycle is begun, it cannot be stopped by applying another $\overline{\text{STROBE}}$ pulse.
8. Output data will be valid 40 ns after $\overline{\text{STROBE}}$ and $\overline{\text{EOC}}$ have returned "L". Parallel output data at the BIT outputs will remain valid and the EOC "L" until 10 ns after another acquisition and conversion cycle is started.
9. When the Data Acquisition System is initially "powered-up", it may come on at any point in the cycle. Disregard the first output indications.

FIGURE 4. Timing diagram - Continued.

TABLE II. Electrical test requirements.

MIL-PRF-38534 test requirements	Subgroups (in accordance with MIL-PRF-38534, group A test table)
Interim electrical parameters	
Final electrical test parameters	1*, 2, 3, 4, 9
Group A test requirements	1, 2, 3, 4, 5, 6, 9, 10, 11
Group C end-point electrical parameters	1, 2, 3

* PDA applies to subgroup 1.

4.3 Conformance and periodic inspections. Conformance inspection (CI) and periodic inspection (PI) shall be in accordance with MIL-PRF-38534 and as specified herein.

4.3.1 Group A inspection (CI). Group A inspection shall be in accordance with MIL-PRF-38534 and as follows:

a. Tests shall be as specified in table II herein.

b. Subgroups 7 and 8 shall be omitted.

4.3.2 Group B inspection (PI). Group B inspection shall be in accordance with MIL-PRF-38534.

4.3.3 Group C inspection (PI). Group C inspection shall be in accordance with MIL-PRF-38534 and as follows:

a. End-point electrical parameters shall be as specified in table II herein.

b. Steady-state life test, method 1005 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to either DSCC-VA or the acquiring activity upon request. Also, the test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

(2) T_A as specified in accordance with table I of method 1005 of MIL-STD-883.

(3) Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.3.4 Group D inspection (PI). Group D inspection shall be in accordance with MIL-PRF-38534.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38534.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.2 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.3 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.

6.4 Record of users. Military and industrial users shall inform Defense Supply Center Columbus when a system application requires configuration control and the applicable SMD. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0544.

6.5 Comments. Comments on this drawing should be directed to DSCC-VA, P. O. Box 3990, Columbus, Ohio 43216-5000, or telephone (614) 692-0512.

6.6 Sources of supply. Sources of supply are listed in QML-38534. The vendors listed in MIL-HDBK-103 and QML-38534 have submitted a certificate of compliance (see 3.7 herein) to DSCC-VA and have agreed to this drawing.

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 00-01-05

Approved sources of supply for SMD 5962-88514 are listed below for immediate acquisition only and shall be added to MIL-HDBK-103 and QML-38534 during the next revisions. MIL-HDBK-103 and QML-38534 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revisions of MIL-HDBK-103 and QML-38534.

Standard microcircuit drawing PIN 1/	Vendor CAGE number	Vendor similar PIN 2/
5962-8851401XC 5962-8851401XA	33256 33256	HS9403B-8 HS9403B-8
5962-8851402XC 5962-8851402XA	33256 33256	HS9403B-16 HS9403B-16
5962-8851402YX	3/	HS9403B-16FP
5962-8851403XC 5962-8851403XA	50721 50721	HDAS-8/883 HDAS-8/883
5962-8851404XC 5962-8851404XA	50721 50721	HDAS-16/883 HDAS-16/883

1/ The lead finish shown for each PIN, representing a hermetic package, is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed contact the Vendor to determine availability.
2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.
3/ Not available from a QML source.

Vendor CAGE number	Vendor name and address
33256	Sipex Corporation 22 Linnell Circle Billerica, MA 01821
50721	Datel, Incorporated 11 Cabot Boulevard Mansfield, MA 02048