FAIRCHILD SEMICONDUCTOR®

May 2009

FDMS6681Z

P-Channel PowerTrench® MOSFET

-30 V, -49 A, 3.2 mΩ

Features

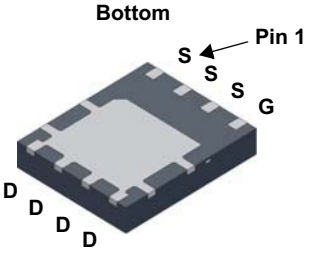
- Max $r_{DS(on)}$ = 3.2 mΩ at V_{GS} = -10 V, I_D = -21.1 A
- Max $r_{DS(on)}$ = 5.0 mΩ at V_{GS} = -4.5 V, I_D = -15.7 A
- Advanced Package and Silicon combination for low $r_{DS(on)}$
- HBM ESD protection level of 8kV typical(note 3)
- MSL1 robust package design
- RoHS Compliant

General Description

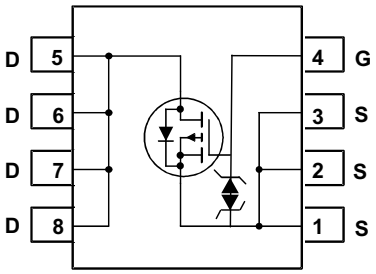
The FDMS6681Z has been designed to minimize losses in load switch applications. Advancements in both silicon and package technologies have been combined to offer the lowest $r_{DS(on)}$ and ESD protection.

Applications

- Load Switch in Notebook and Server
- Notebook Battery Pack Power Management



Power 56



MOSFET Maximum Ratings T_A = 25 °C unless otherwise noted

Symbol	Parameter			Ratings	Units
V_{DS}	Drain to Source Voltage			-30	V
V_{GS}	Gate to Source Voltage			±25	V
I_D	Drain Current -Continuous (Package limited)	T_C = 25 °C		-49	A
	-Continuous (Silicon limited)	T_C = 25 °C		-116	
	-Continuous	T_A = 25 °C	(Note 1a)	-21.1	
	-Pulsed			-90	
P_D	Power Dissipation	T_C = 25 °C		73	W
	Power Dissipation	T_A = 25 °C	(Note 1a)	2.5	
T_J, T_{STG}	Operating and Storage Junction Temperature Range			-55 to +150	°C

Thermal Characteristics

$R_{\theta JC}$	Thermal Resistance, Junction to Case		1.7	°C/W
$R_{\theta JA}$	Thermal Resistance, Junction to Ambient	(Note 1a)	50	

Package Marking and Ordering Information

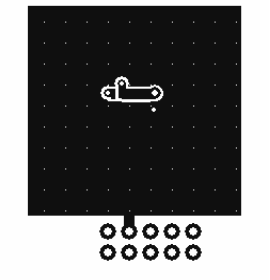
Device Marking	Device	Package	Reel Size	Tape Width	Quantity
FDMS6681Z	FDMS6681Z	Power 56	13 ”	12 mm	3000 units

Electrical Characteristics T_J = 25 °C unless otherwise noted

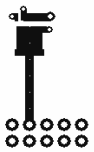
Symbol	Parameter	Test Conditions	Min	Typ	Max	Units
Off Characteristics						
BV_{DSS}	Drain to Source Breakdown Voltage	I_D = -250 μA, V_{GS} = 0 V	-30			V
$\frac{\Delta BV_{DSS}}{\Delta T_J}$	Breakdown Voltage Temperature Coefficient	I_D = -250 μA, referenced to 25 °C		20		mV/°C
I_{DSS}	Zero Gate Voltage Drain Current	V_{DS} = -24 V, V_{GS} = 0 V			-1	μA
I_{GSS}	Gate to Source Leakage Current	V_{GS} = ±25 V, V_{DS} = 0 V			±10	μA
On Characteristics						
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{GS} = V_{DS}, I_D = -250 μA	-1	-1.7	-3	V
$\frac{\Delta V_{GS(th)}}{\Delta T_J}$	Gate to Source Threshold Voltage Temperature Coefficient	I_D = -250 μA, referenced to 25 °C		-7		mV/°C
$r_{DS(on)}$	Static Drain to Source On Resistance	V_{GS} = -10 V, I_D = -22.1 A		2.7	3.2	mΩ
		V_{GS} = -4.5 V, I_D = -15.7 A		4.0	5.0	
		V_{GS} = -10 V, I_D = -22.1 A, T_J = 125 °C		3.9	5.0	
g_{FS}	Forward Transconductance	V_{DD} = -10 V, I_D = -22.1 A		143		S
Dynamic Characteristics						
C_{iss}	Input Capacitance	V_{DS} = -15 V, V_{GS} = 0 V, f = 1 MHz		7803	10380	pF
C_{oss}	Output Capacitance			1540	2050	pF
C_{rss}	Reverse Transfer Capacitance			1345	2020	pF
Switching Characteristics						
$t_{d(on)}$	Turn-On Delay Time	V_{DD} = -15 V, I_D = -22.1 A, V_{GS} = -10 V, R_{GEN} = 6 Ω		15	24	ns
t_r	Rise Time			38	61	ns
$t_{d(off)}$	Turn-Off Delay Time			260	416	ns
t_f	Fall Time			197	316	ns
Q_g	Total Gate Charge	V_{GS} = 0 V to -10 V; V_{DD} = -15 V, I_D = -22.1 A		172	241	nC
Q_g	Total Gate Charge	V_{GS} = 0 V to -5 V; V_{DD} = -15 V, I_D = -22.1 A		97	136	nC
Q_{gs}	Gate to Source Charge	V_{DD} = -15 V, I_D = -22.1 A		22		nC
Q_{gd}	Gate to Drain “Miller” Charge	V_{DD} = -15 V, I_D = -22.1 A		46		nC
Drain-Source Diode Characteristics						
V_{SD}	Source to Drain Diode Forward Voltage	V_{GS} = 0 V, I_S = -2.1 A (Note 2)		0.68	1.2	V
		V_{GS} = 0 V, I_S = -22.1 A (Note 2)		0.79	1.25	V
t_{rr}	Reverse Recovery Time	I_F = -22.1 A, di/dt = 100 A/μs		44	71	ns
Q_{rr}	Reverse Recovery Charge			39	63	nC

NOTES:

1. $R_{\theta JA}$ is determined with the device mounted on a 1 in^2 pad 2 oz copper pad on a 1.5 x 1.5 in. board of FR-4 material. $R_{\theta JC}$ is guaranteed by design while $R_{\theta CA}$ is determined by the user's board design.



a. 50 °C/W when mounted on a 1 in^2 pad of 2 oz copper.



b. 125 °C/W when mounted on a minimum pad of 2 oz copper.

2. Pulse Test: Pulse Width < 300 μs, Duty cycle < 2.0%.
3. The diode connected between the gate and source servers only as protection against ESD. No gate overvoltage rating is implied.

Typical Characteristics T_J = 25 °C unless otherwise noted

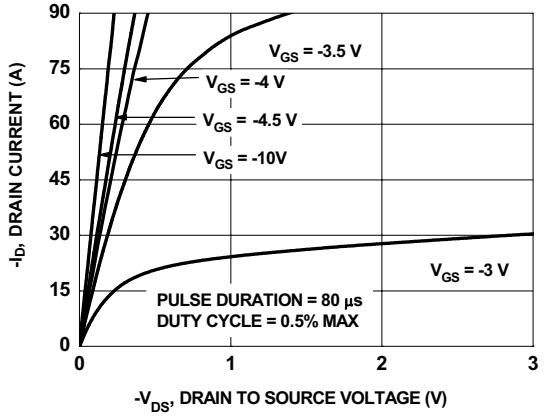


Figure 1. On Region Characteristics

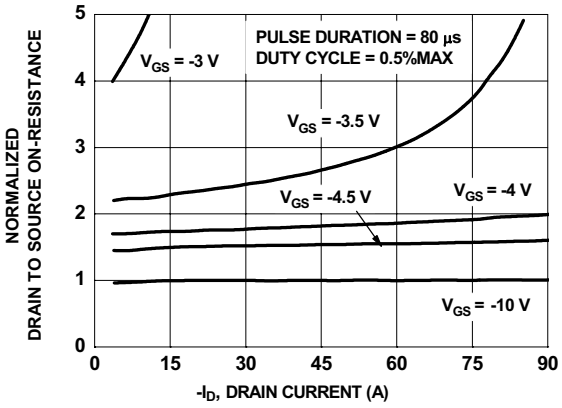


Figure 2. Normalized On-Resistance vs Drain Current and Gate Voltage

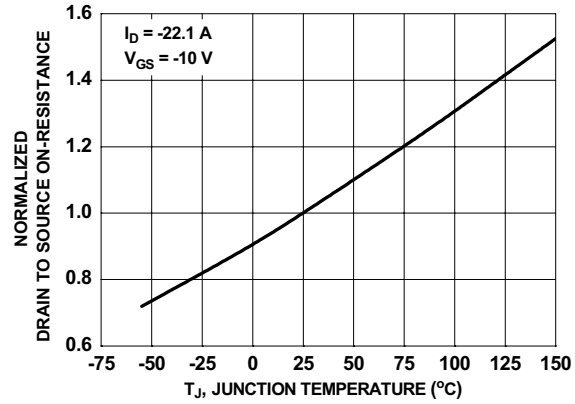


Figure 3. Normalized On Resistance vs Junction Temperature

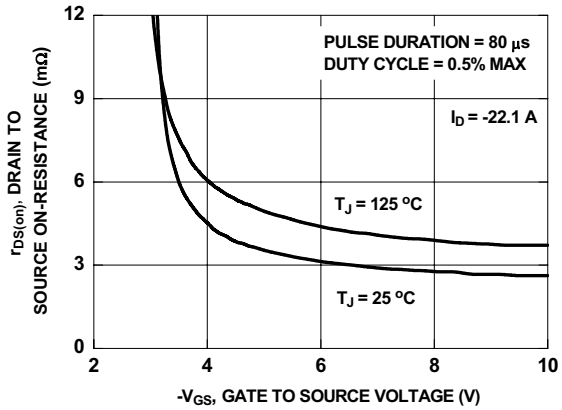


Figure 4. On-Resistance vs Gate to Source Voltage

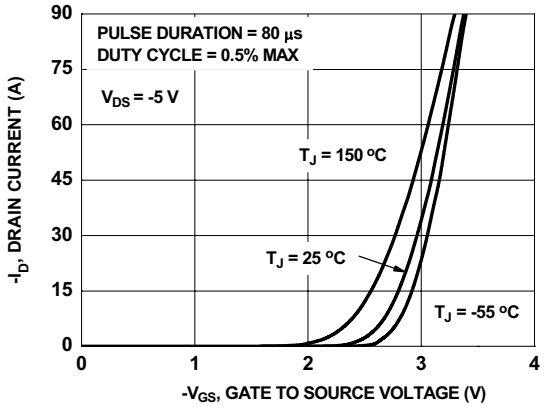


Figure 5. Transfer Characteristics

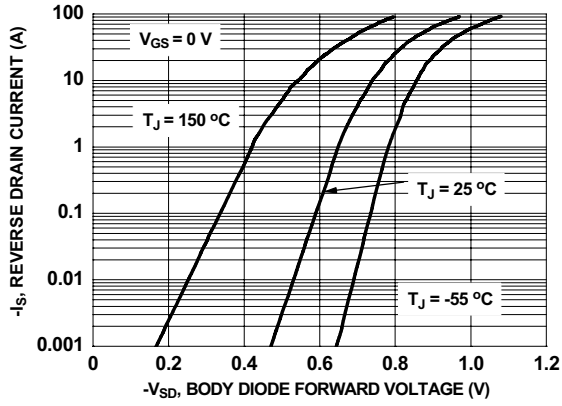


Figure 6. Source to Drain Diode Forward Voltage vs Source Current

Typical Characteristics T_J = 25 °C unless otherwise noted

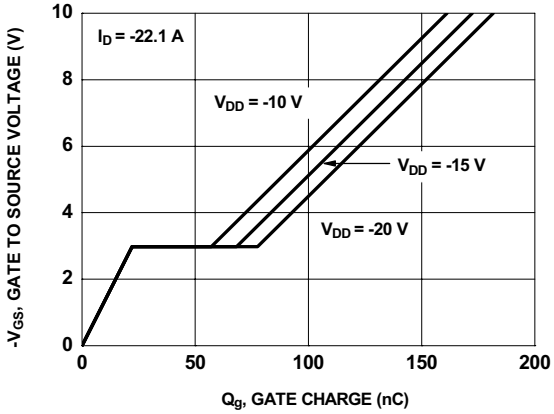


Figure 7. Gate Charge Characteristics

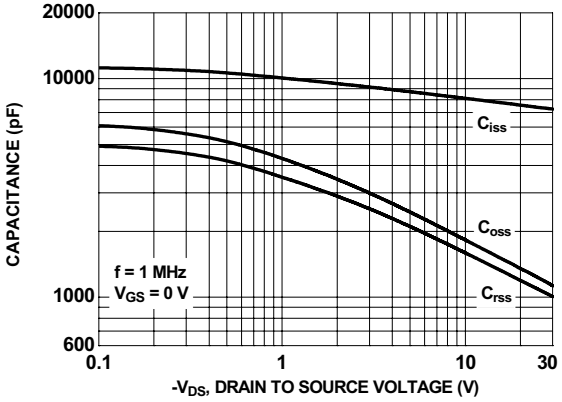


Figure 8. Capacitance vs Drain to Source Voltage

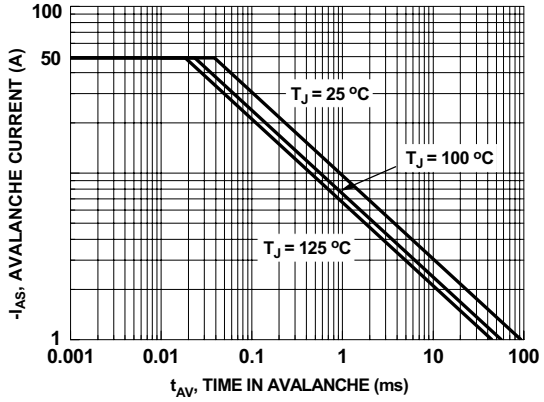


Figure 9. Unclamped Inductive Switching Capability

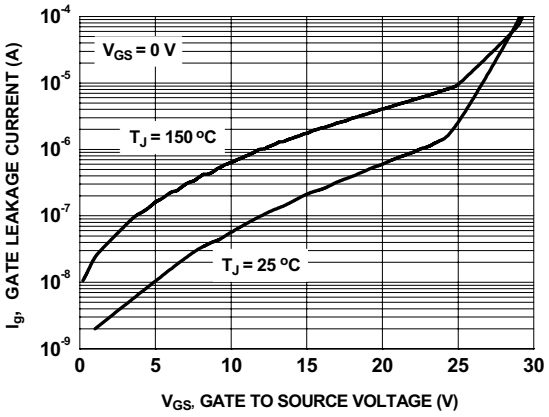


Figure 10. I_{gss} vs V_{gss}

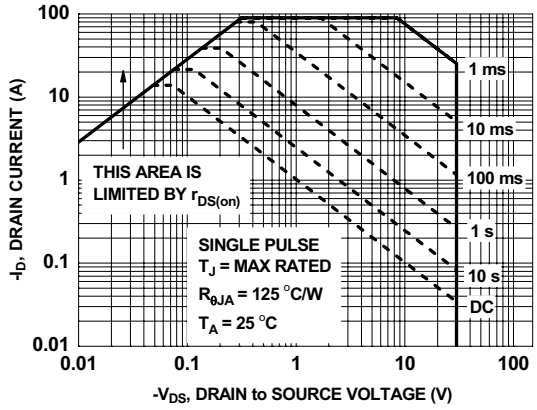


Figure 11. Forward Bias Safe Operating Area

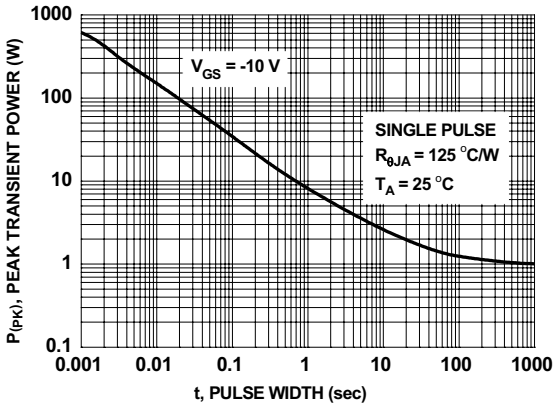


Figure 12. Single Pulse Maximum Power Dissipation

Typical Characteristics T_J = 25 °C unless otherwise noted

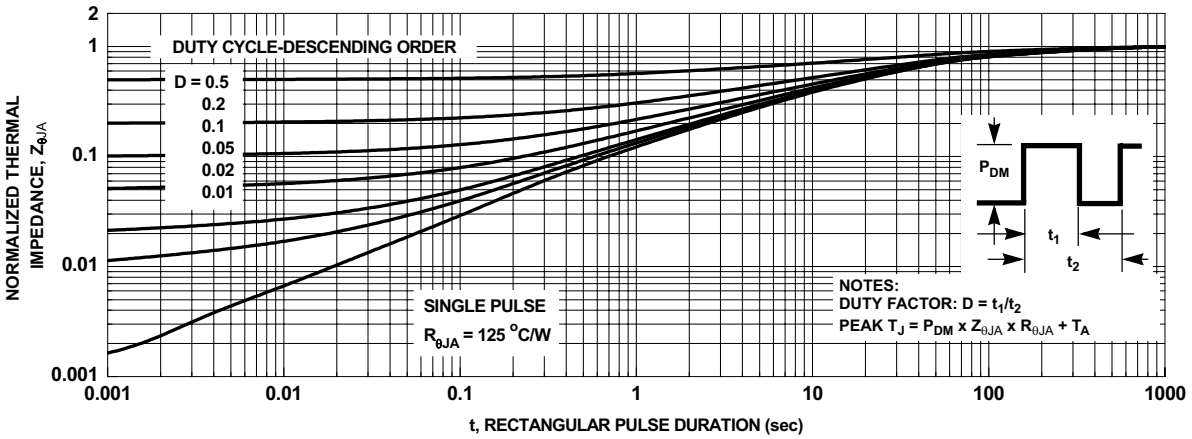
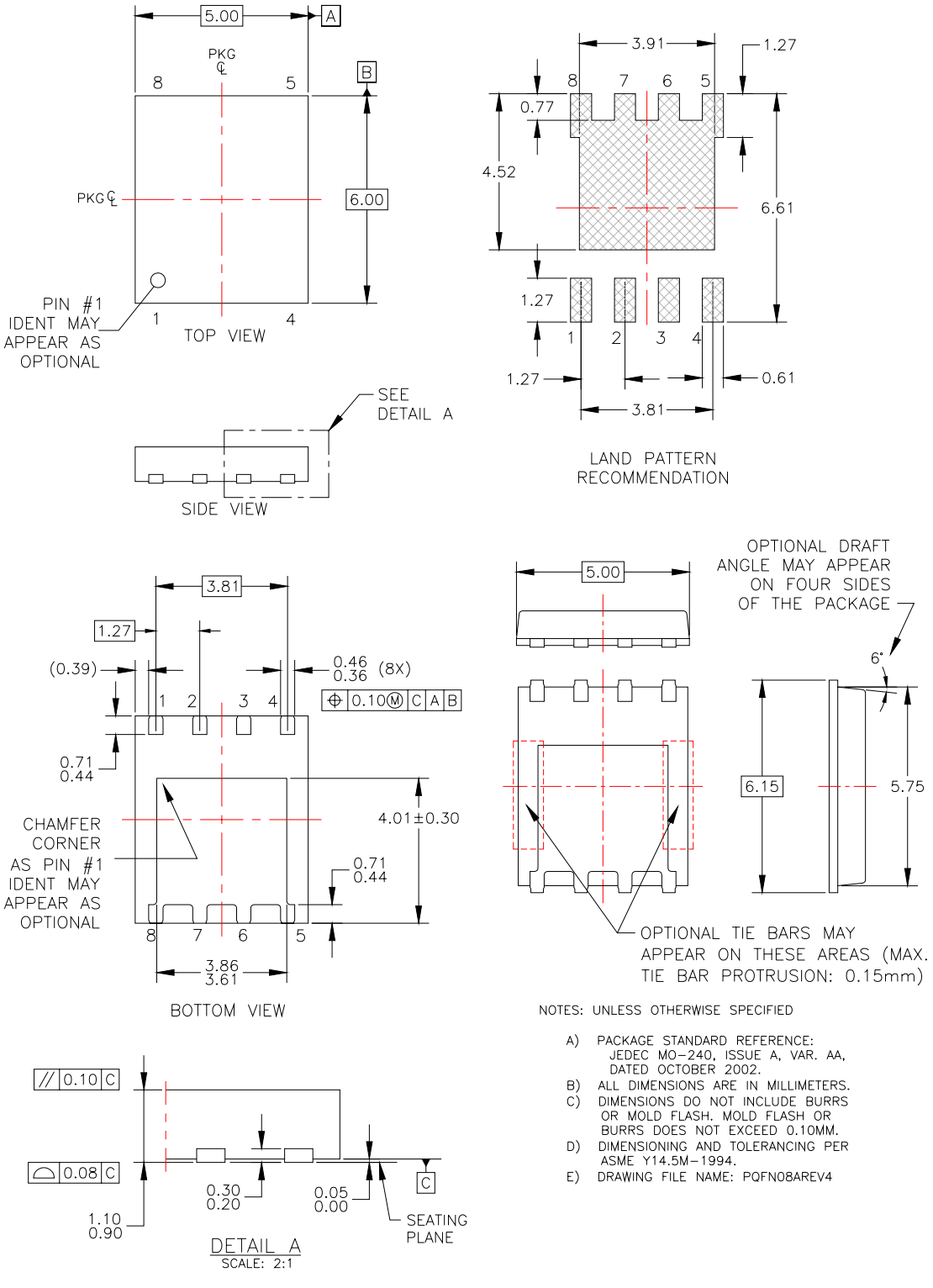


Figure 13. Junction-to-Ambient Transient Thermal Response Curve

Dimensional Outline and Pad Layout



NOTES: UNLESS OTHERWISE SPECIFIED

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B) ALL DIMENSIONS ARE IN MILLIMETERS.
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D) DIMENSIONING AND TOLERANCING PER ASME Y14.5M-1994.
E) DRAWING FILE NAME: PQFN08AREV4

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