





Phase Control Thyristor

Preliminary Information

DS5932-1.1 January 2009 (LN 26574)

FEATURES

- Double Side Cooling
- High Surge Capability

APPLICATIONS

- High Power Drives
- High Voltage Power Supplies
- Static Switches

VOLTAGE RATINGS

Part and Ordering Number	Repetitive Peak Voltages V _{DRM} and V _{RRM} V	Conditions
DCR2560A85* DCR2560A80 DCR2560A75 DCR2560A70	8500 8000 7500 7000	$\begin{split} &T_{vj} = \text{-}40^\circ\!\text{C to }125^\circ\!\text{C},\\ &I_{DRM} = I_{RRM} = 300\text{mA},\\ &V_{DRM}, V_{RRM}t_p = 10\text{ms},\\ &V_{DSM}\&V_{RSM} = \\ &V_{DRM}\&V_{RRM} + 100V\\ &\text{respectively} \end{split}$

Lower voltage grades available. *8200V @ -40°C, 8500V @ 0°C

ORDERING INFORMATION

When ordering, select the required part number shown in the Voltage Ratings selection table.

For example:

DCR2560A85

Note: Please use the complete part number when ordering and quote this number in any future correspondence relating to your order.

KEY PARAMETERS

V _{DRM}	8500V
I _{T(AV)}	2560A
I _{TSM}	32500A
dV/dt*	1500V/μs
dl/dt	200Α/μs
	•

* Higher dV/dt selections available

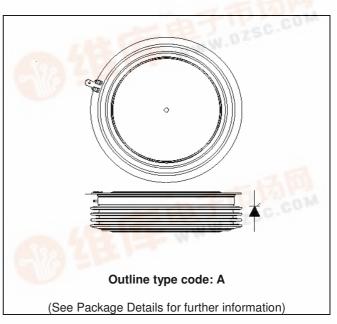


Fig. 1 Package outline





CURRENT RATINGS

T_{case} = 60 °C unless stated otherwise

Symbol	Parameter	Test Conditions	Max.	Units
Double Sid	de Cooled			
I _{T(AV)}	Mean on-state current	Half wave resistive load	2555	Α
I _{T(RMS)}	RMS value	-	4013	Α
I _T	Continuous (direct) on-state current	-	3710	Α

SURGE RATINGS

Symbol	Parameter	Parameter Test Conditions			
I _{TSM}	Surge (non-repetitive) on-state current	10ms half sine, T _{case} = 125 ℃	32.5	kA	
l ² t	I ² t for fusing	$V_R = 0$	5.28	MA ² s	

THERMAL AND MECHANICAL RATINGS

Symbol	Parameter	Test Conditions	Min.	Max.	Units	
R _{th(j-c)}	Thermal resistance – junction to case	Double side cooled	Double side cooled DC		0.00603	.c\M
		Single side cooled	Anode DC	-	0.01024	.c\M
			Cathode DC	-	0.01467	.c/M
R _{th(c-h)}	Thermal resistance – case to heatsink	Clamping force 83.0kN	Double side	-	0.001	.c\M
		(with mounting compound)	Single side	-	0.002	.c/M
T _{vj}	Virtual junction temperature	On-state (conducting)		-	135	ç
		Reverse (blocking)		-	125	ç
T _{stg}	Storage temperature range			-55	125	°C
F _m	Clamping force			74.0	91.0	kN

DYNAMIC CHARACTERISTICS

Symbol	Parameter	Test Conditio	Min.	Max.	Units	
I _{RRM} /I _{DRM}	Peak reverse and off-state current	At V _{RRM} /V _{DRM} , T _{case} = 125 ℃	-	300	mA	
dV/dt	Max. linear rate of rise of off-state voltage	To 67% V _{DRM} , T _j = 125℃, ga	ite open	-	1500	V/µs
dI/dt	Rate of rise of on-state current	From 67% V _{DRM} to 2x I _{T(AV)}	Repetitive 50Hz	-	100	A/μs
		Gate source 30V, 10Ω,	Non-repetitive	-	200	A/μs
		$t_r < 0.5 \mu s, T_j = 125 ^{\circ}\text{C}$				
$V_{T(TO)}$	Threshold voltage – Low level	500 to 1600A at T _{case} = 125°	С	-	0.9	V
	Threshold voltage – High level	1600 to 4000A at T _{case} = 125	-	1.18	V	
r _T	On-state slope resistance – Low level	500A to 1600A at T _{case} = 125	-	0.65	mΩ	
	On-state slope resistance – High level	1600A to 4000A at T _{case} = 12	-	0.46	mΩ	
t _{gd}	Delay time	$V_D = 67\% V_{DRM}$, gate source 30V, 10Ω			3	μs
		$t_r = 0.5 \mu s, T_j = 25 ^{\circ}C$				
tq	Turn-off time	$I_T = 3000A, T_j = 125 ^{\circ}C,$ $V_R = 200V, dI/dt = 1A/\mu s,$		1000	μs	
		dV _{DR} /dt = 20V/μs linear				
Qs	Stored charge	$I_T = 3000 A, \ T_j = 125^{\circ}\!C, \ dI/dt - 1A/\mu s, \\ V_{Rpeak} \sim \! 5100 V, \ V_R \sim 3400 V$			7950	μC
IL	Latching current	$T_j = 25 ^{\circ}\text{C}, V_D = 5V$	-	3	Α	
lμ	Holding current	$T_j = 25 {}^{\circ}\text{C}, \; R_{G-K} = \infty, \; I_{TM} = 500 A, \; I_T = 5 A$			300	mA

GATE TRIGGER CHARACTERISTICS AND RATINGS

Symbol	Parameter	Test Conditions	Max.	Units
V_{GT}	Gate trigger voltage	V _{DRM} = 5V, T _{case} = 25 ℃	1.5	٧
V_{GD}	Gate non-trigger voltage	At V _{DRM} , T _{case} = 125 °C	0.3	٧
I _{GT}	Gate trigger current	V _{DRM} = 5V, T _{case} = 25 ℃	400	mA
I _{GD}	Gate non-trigger current	V _{DRM} = 5V, T _{case} = 25 ℃	20	mA

CURVES

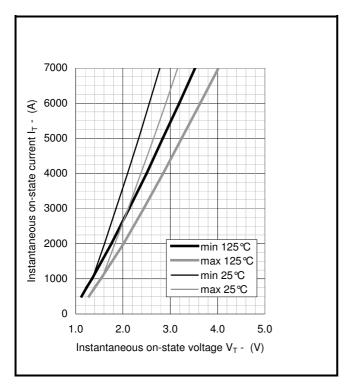


Fig.2 Maximum & minimum on-state characteristics

 V_{TM} EQUATION

 $V_{TM} = A + Bln (I_T) + C.I_T + D.\sqrt{I_T}$

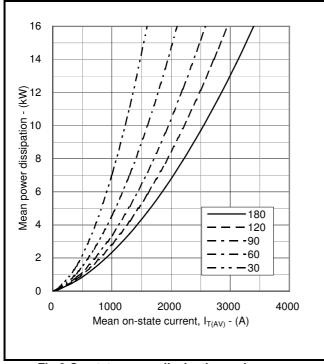
Where A = -0.224010

B = 0.1725829

C = 0.000292D = 0.01039

these values are valid for $T_j = 125$ °C for $I_T 500$ A to 4200A







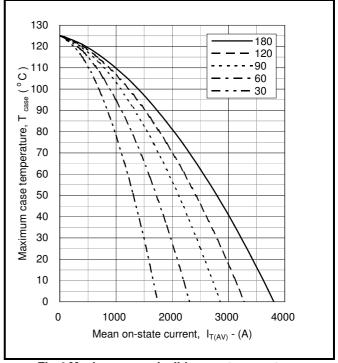


Fig.4 Maximum permissible case temperature, double side cooled – sine wave

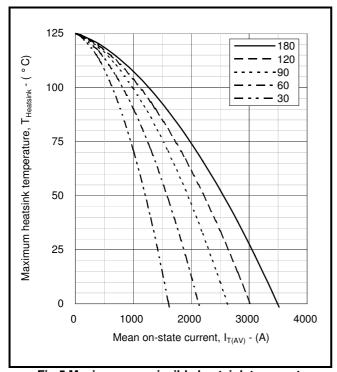


Fig.5 Maximum permissible heatsink temperature, double side cooled – sine wave

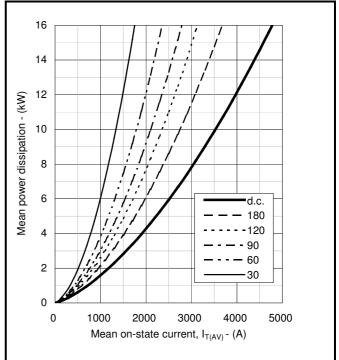


Fig.6 On-state power dissipation - rectangular wave



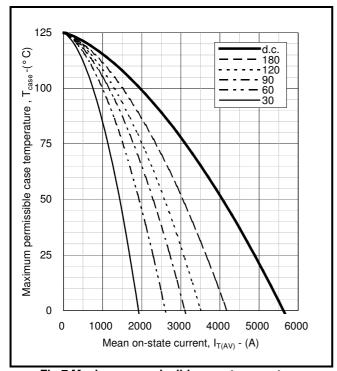


Fig.7 Maximum permissible case temperature, double side cooled - rectangular wave

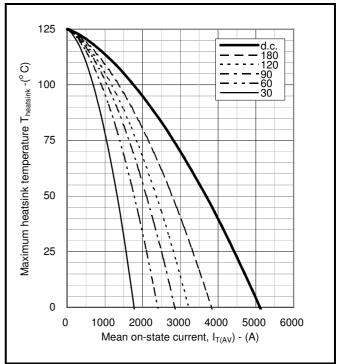
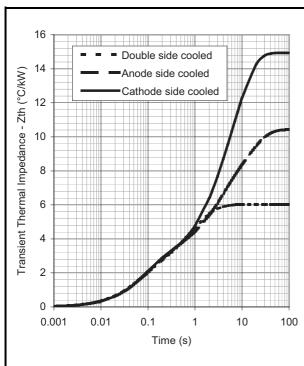


Fig.8 Maximum permissible heatsink temperature, double side cooled - rectangular wave



		1	2	3	4
Double side cooled	R _i (℃/kW)	3.01541	1.048955	0.983519	0.983519
Double side cooled	T _i (s)	0.703874	1.904794	0.059	0.059
Anode side cooled	R _i (℃/kW)	3.156003	4.092806	1.556555	1.623962
Ariode side cooled	T _i (s)	2.69023	13.79162	0.059	0.205916
Cathode side cooled	R _i (℃/kW)	7.077369	3.483481	1.745839	2.634274
Callibue side cooled	T _i (s)	6.648601	8.436484	1.762119	0.08069

$$Z_{th} = \sum_{i=1}^{i=4} [R_i \times (1 - \exp(T/T_i))]$$

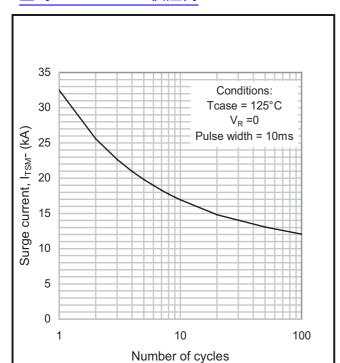
$\Delta R_{\text{th(j-c)}}$ Conduction

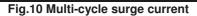
Tables show the increments of thermal resistance $R_{\text{th}(j\text{-}c)}$ when the device operates at conduction angles other than d.c.

D	Double side cooling Anode Side Cooling				
	ΔZ_{th}			1	_h (z)
θ°	sine. rect.		θ°	sine.	rect.
180	0.44	0.31	180	0.42	0.30
120	0.49	0.43	120	0.47	0.41
90	0.55	0.49	90	0.52	0.46
60	0.60	0.55	60	0.57	0.52
30	0.64	0.61	30	0.61	0.58
15	0.66 0.64		15	0.62	0.61

ıble side c	ooling		Anode Side Cooling				Cathode Sided Cooling		
ΔZ_{th}	(z)			ΔZ_t	_h (z)			ΔZ_{th} (z)	
sine.	rect.		θ°	sine.	rect.		θ°	sine.	rect.
0.44	0.31	1	180	0.42	0.30		180	0.42	0.30
0.49	0.43	1	120	0.47	0.41		120	0.47	0.41
0.55	0.49	- 1	90	0.52	0.46		90	0.52	0.46
0.60	0.55		60	0.57	0.52		60	0.57	0.52
0.64	0.61		30	0.61	0.58		30	0.60	0.58
0.66	0.64		15	0.62	0.61		15	0.62	0.60

Fig.9 Maximum (limit) transient thermal impedance – junction to case (°C/kW)





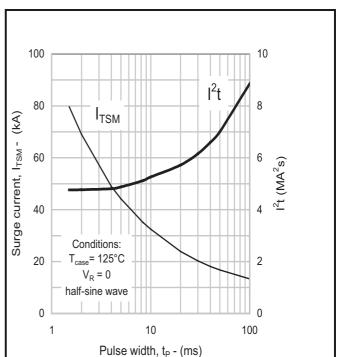


Fig.11 Single-cycle surge current

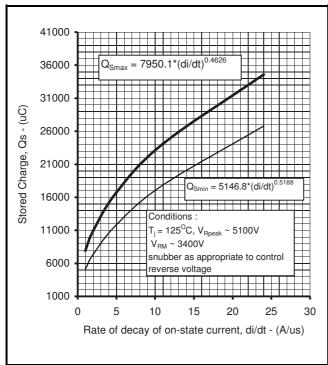


Fig.12 Stored charge

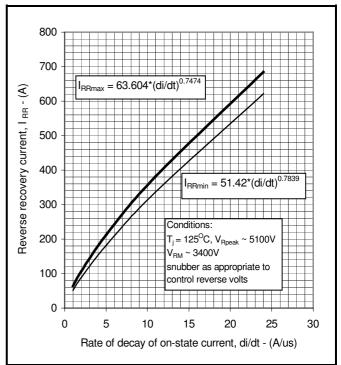


Fig.13 Reverse recovery current

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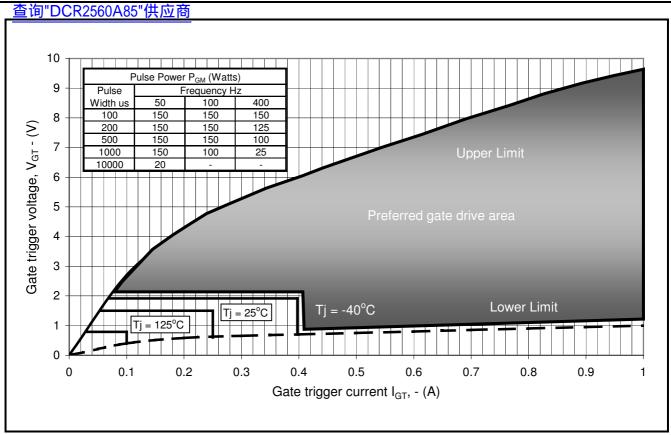


Fig14 Gate Characteristics

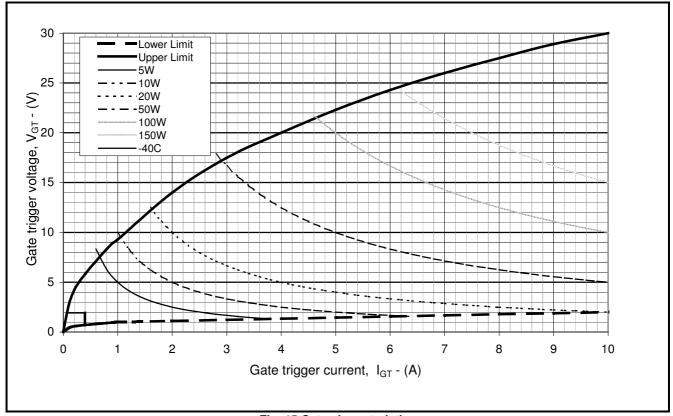


Fig. 15 Gate characteristics



查询"DCR2560A85"供应商 PACKAGE DETAILS

For further package information, please contact Customer Services. All dimensions in mm, unless stated otherwise. DO NOT SCALE.

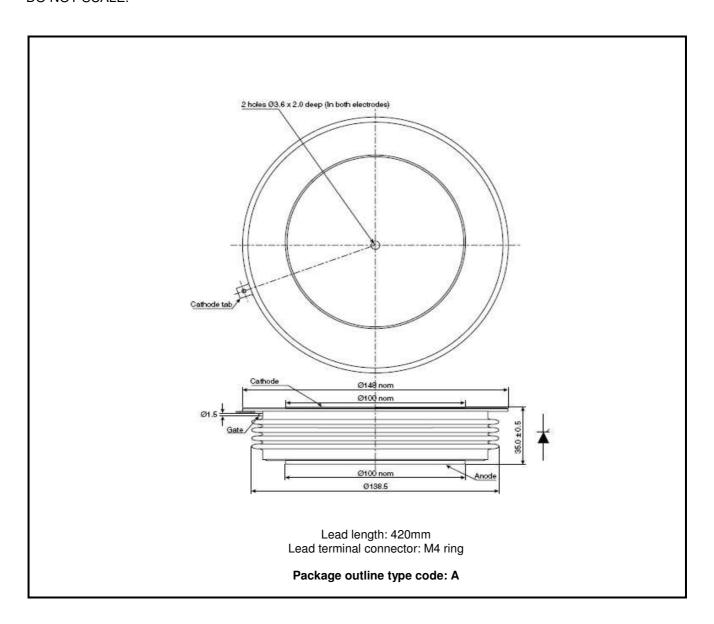


Fig.16 Package outline



'DCR2560A85"供应商

POWER ASSEMBLY CAPABILITY

The Power Assembly group was set up to provide a support service for those customers requiring more than the basic semiconductor, and has developed a flexible range of heatsink and clamping systems in line with advances in device voltages and current capability of our semiconductors.

We offer an extensive range of air and liquid cooled assemblies covering the full range of circuit designs in general use today. The Assembly group offers high quality engineering support dedicated to designing new units to satisfy the growing needs of our customers.

Using the latest CAD methods our team of design and applications engineers aim to provide the Power Assembly Complete Solution (PACs).

HEATSINKS

The Power Assembly group has its own proprietary range of extruded aluminium heatsinks which have been designed to optimise the performance of Dynex semiconductors. Data with respect to air natural, forced air and liquid cooling (with flow rates) is available on request.

For further information on device clamps, heatsinks and assemblies, please contact your nearest sales representative or Customer Services.

Stresses above those listed in this data sheet may cause permanent damage to the device. In extreme conditions, as with all semiconductors, this may include potentially hazardous rupture of the package. Appropriate safety precautions should always be followed.



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