

# 3.3V 16-bit bus transceiver/register (3-State)

# 74LVT16652A

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## FEATURES

- 16-bit bus interface
- 3-State buffers
- Output capability: +64mA/-32mA
- TTL input and output switching levels
- Input and output interface capability to systems at 5V supply
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- Power-up reset
- Power-up 3-State
- No bus current loading when output is tied to 5V bus
- Latch-up protection exceeds 500mA per JEDEC Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model

## DESCRIPTION

The 74LVT16652A is a high-performance BiCMOS product designed for  $V_{CC}$  operation at 3.3V. The device can be used as two 8-bit transceivers or one 16-bit transceiver.

Complimentary output-enable (OEAB and  $\overline{OEBA}$ ) inputs are provided to control the transceiver functions. Select-control (SAB and SBA) inputs are provided to select whether real-time or stored data is transferred. A Low-input level selects real-time data, and a High input level selects stored data. The circuitry used for select control eliminates the typical decoding glitch that occurs in a multiplexer during the transition between stored and real-time data.

Data on the A or B bus, or both, can be stored in the internal flip-flops by Low-to-High transitions at the appropriate clock (CPAB or CPBA) inputs regardless of the levels on the select-control or output-enable inputs. When SAB and SBA are in real-time transfer mode, it is possible to store data without using the internal D-type flip-flops by simultaneously enabling OEAB and  $\overline{OEBA}$ . In this configuration, each output reinforces its input. Thus, when all other data sources to the two sets of bus lines are at high impedance, each set of bus lines remains at its last level configuration.

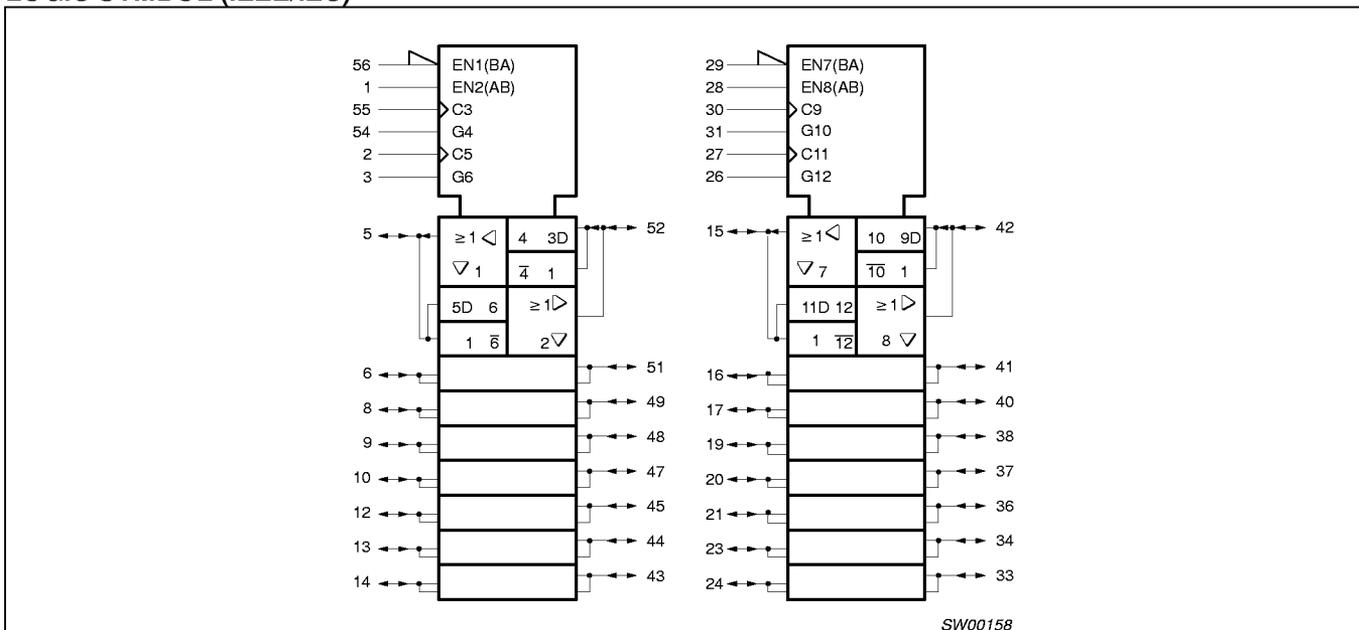
## QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS $T_{amb} = 25^{\circ}C$	TYPICAL	UNIT
$t_{PLH}$ $t_{PHL}$	Propagation delay nAx to nBx or nBx to nAx	$C_L = 50pF$ ; $V_{CC} = 3.3V$	1.9	ns
$C_{IN}$	Input capacitance Control pins	$V_I = 0V$ or $3.0V$	3	pF
$C_{I/O}$	I/O pin capacitance	Outputs disabled; $V_I = 0V$ or $3.0V$	9	pF
$I_{CCZ}$	Total supply current	Outputs disabled; $V_{CC} = 3.6V$	70	$\mu A$

## ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
56-Pin Plastic SSOP Type III	-40°C to +85°C	74LVT16652A DL	VT16652A DL	SOT371-1
56-Pin Plastic TSSOP Type II	-40°C to +85°C	74LVT16652A DGG	VT16652A DGG	SOT364-1

## LOGIC SYMBOL (IEEE/IEC)

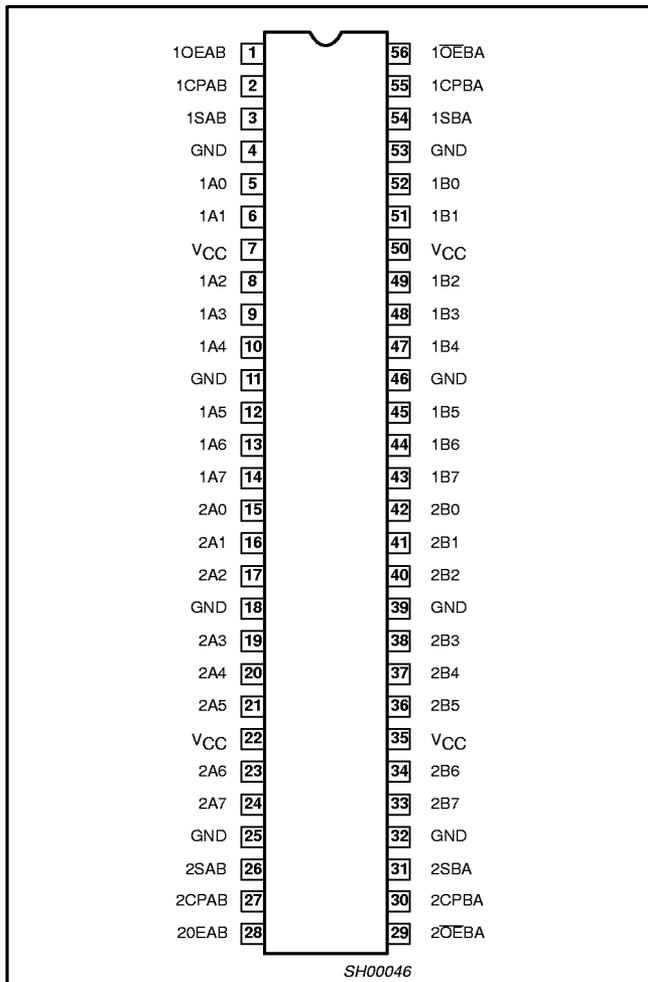


3.3V 16-bit bus transceiver/register (3-State)

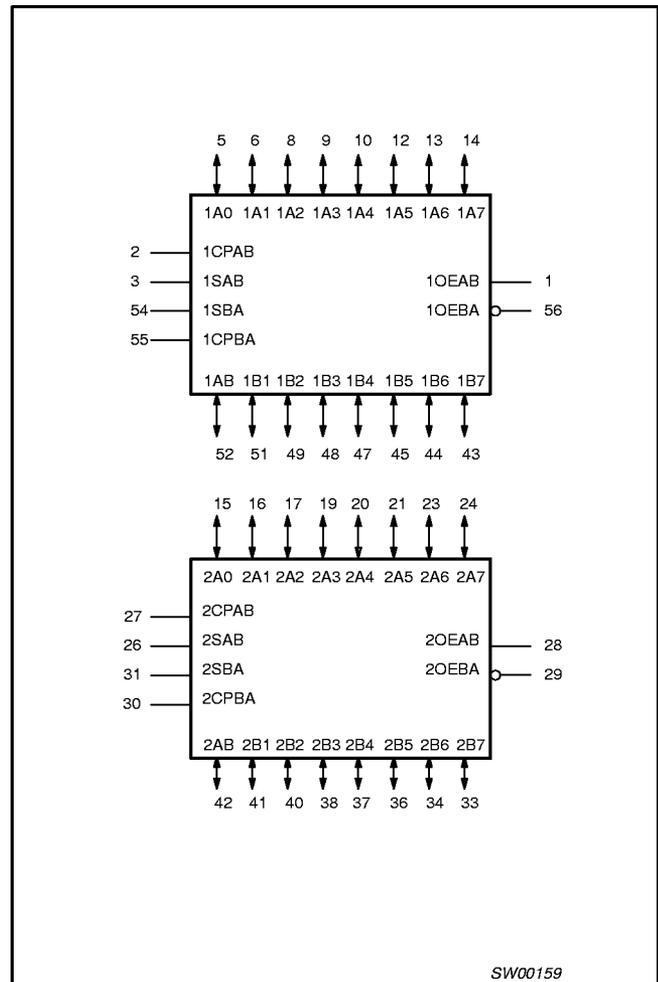
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PIN CONFIGURATION



LOGIC SYMBOL



PIN DESCRIPTION

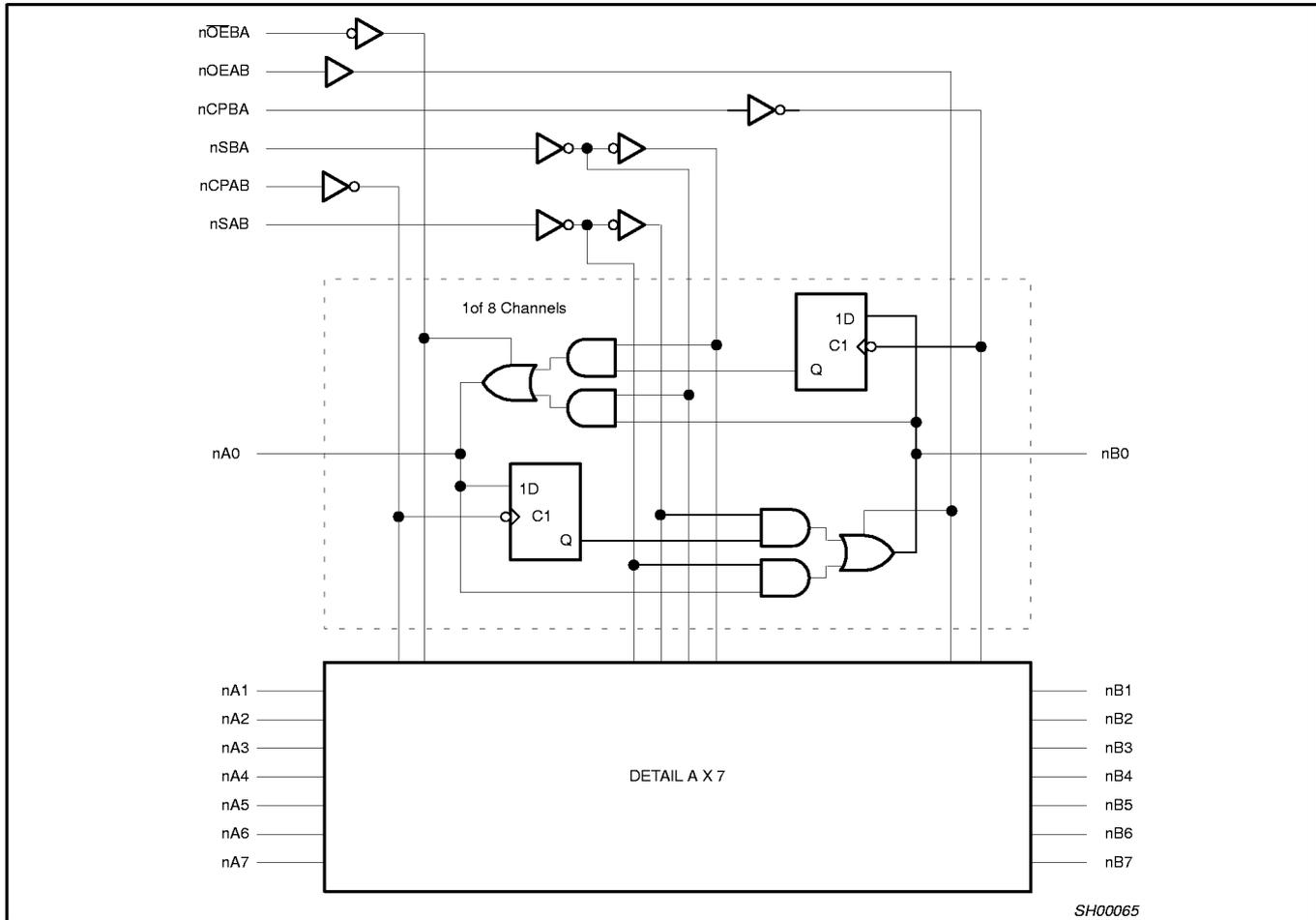
PIN NUMBER	SYMBOL	NAME AND FUNCTION
2, 55, 27, 30	1CPAB, 1CPBA, 2CPAB, 2CPBA	Clock input A to B / Clock input B to A
3, 54, 26, 31	1SAB, 1SBA, 2SAB, 2SBA	Select input A to B / Select input B to A
5, 6, 8, 9, 10, 12, 13, 14 15, 16, 17, 19, 20, 21, 23, 24	1A0 – 1A7, 2A0 – 2A7	Data inputs/outputs (A side)
52, 51, 49, 48, 47, 45, 44, 43 42, 41, 40, 38, 37, 36, 34, 33	1B0 – 1B7, 2B0 – 2B7	Data inputs/outputs (B side)
1, 56, 28, 29	1OEAB, 1OEBA, 2OEAB, 2OEBA	Output enable inputs
4, 11, 18, 25, 32, 39, 46, 53	GND	Ground (0V)
7, 22, 35, 50	V <sub>CC</sub>	Positive supply voltage

### 3.3V 16-bit bus transceiver/register (3-State)

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#### LOGIC DIAGRAM



#### FUNCTION TABLE

INPUTS						DATA I/O		OPERATING MODE
nOEAB	nOEBA	nCPAB	nCPBA	nSAB	nSBA	nAx	nBx	
L	H	H or L	H or L	X	X	Input	Input	Isolation Store A and B data
L	H	↑	↑	X	X	Input	Input	Store A, Hold B Store A in both registers
X	H	↑	H or L	**	X	Input	Unspecified output*	Store A, Hold B Store A in both registers
H	H	↑	↑	X	X	Unspecified output*	Input	Hold A, Store B Store B in both registers
L	X	H or L	↑	X	**	Unspecified output*	Input	Hold A, Store B Store B in both registers
L	L	X	X	X	L	Output	Input	Real time B data to A bus Stored B data to A bus
L	L	X	H or L	X	H	Output	Input	Real time B data to A bus Stored B data to A bus
H	H	X	X	X	L	Input	Output	Real time A data to B bus Store A data to B bus
H	H	H or L	X	L	X	Input	Output	Real time A data to B bus Store A data to B bus
H	L	H or L	H or L	H	H	Output	Output	Stored A data to B bus Stored B data to A bus

H = High voltage level

L = Low voltage level

X = Don't care

↑ = Low-to-High clock transition

\* The data output function may be enabled or disabled by various signals at the nOEBA and nOEAB inputs. Data input functions are always enabled, i.e., data at the bus pins will be stored on every Low-to-High transition of the clock.

\*\* If both Select controls (nSAB and nSBA) are Low, then clocks can occur simultaneously. If either Select control is High, the clocks must be staggered in order to load both registers.

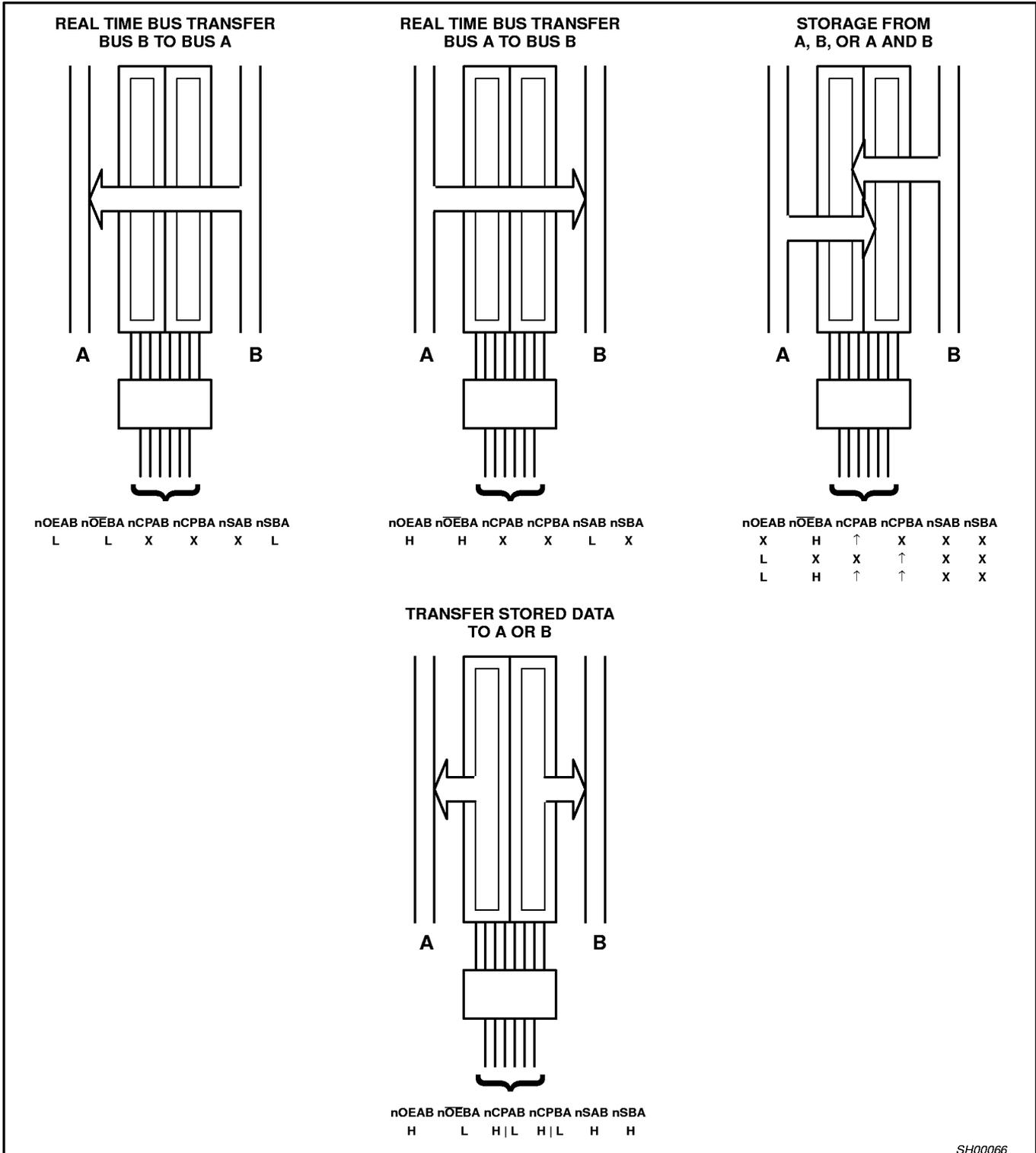
# 3.3V 16-bit bus transceiver/register (3-State)

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The following examples demonstrate the four fundamental bus-management functions that can be performed with the 74LVT16652A. The select pins determine whether data is stored or

transferred through the device in real time. The output enable pins determine the direction of the data flow.



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## 3.3V 16-bit bus transceiver/register (3-State)

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[查询 74LVT16652ADL-T 供应商](#)**ABSOLUTE MAXIMUM RATINGS<sup>1, 2</sup>**

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
$V_{CC}$	DC supply voltage		-0.5 to +4.6	V
$I_{IK}$	DC input diode current	$V_I < 0$	-50	mA
$V_I$	DC input voltage <sup>3</sup>		-0.5 to +7.0	V
$I_{OK}$	DC output diode current	$V_O < 0$	-50	mA
$V_{OUT}$	DC output voltage <sup>3</sup>	Output in Off or High state	-0.5 to +7.0	V
$I_{OUT}$	DC output current	Output in Low state	128	mA
		Output in High state	-64	
$T_{stg}$	Storage temperature range		-65 to +150	°C

**NOTES:**

- Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
- The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

**RECOMMENDED OPERATING CONDITIONS**

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
$V_{CC}$	DC supply voltage	2.7	3.6	V
$V_I$	Input voltage	0	5.5	V
$V_{IH}$	High-level input voltage	2.0		V
$V_{IL}$	Input voltage		0.8	V
$I_{OH}$	High-level output current		-32	mA
$I_{OL}$	Low-level output current		32	mA
	Low-level output current; current duty cycle $\leq 50\%$ ; $f \geq 1\text{kHz}$		64	
$\Delta t/\Delta v$	Input transition rise or fall rate; Outputs enabled		10	ns/V
$T_{amb}$	Operating free-air temperature range	-40	+85	°C

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DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT
			Temp = -40°C to +85°C			
			MIN	TYP <sup>1</sup>	MAX	
V <sub>IK</sub>	Input clamp voltage	V <sub>CC</sub> = 2.7V; I <sub>IK</sub> = -18mA		-0.85	-1.2	V
V <sub>OH</sub>	High-level output voltage	V <sub>CC</sub> = 2.7 to 3.6V; I <sub>OH</sub> = -100µA	V <sub>CC</sub> -0.2	V <sub>CC</sub>		V
		V <sub>CC</sub> = 2.7V; I <sub>OH</sub> = -8mA	2.4	2.5		
		V <sub>CC</sub> = 3.0V; I <sub>OH</sub> = -32mA	2.0	2.3		
V <sub>OL</sub>	Low-level output voltage	V <sub>CC</sub> = 2.7V; I <sub>OL</sub> = 100µA		0.07	0.2	V
		V <sub>CC</sub> = 2.7V; I <sub>OL</sub> = 24mA		0.3	0.5	
		V <sub>CC</sub> = 3.0V; I <sub>OL</sub> = 16mA		0.25	0.4	
		V <sub>CC</sub> = 3.0V; I <sub>OL</sub> = 32mA		0.3	0.5	
		V <sub>CC</sub> = 3.0V; I <sub>OL</sub> = 64mA		0.4	0.55	
V <sub>RST</sub>	Power-up output low voltage <sup>5</sup>	V <sub>CC</sub> = 3.6V; I <sub>O</sub> = 1mA; V <sub>I</sub> = GND or V <sub>CC</sub>		0.11	0.55	V
I <sub>I</sub>	Input leakage current	V <sub>CC</sub> = 3.6V; V <sub>I</sub> = V <sub>CC</sub> or GND	Control pins	0.1	±1	µA
		V <sub>CC</sub> = 0 or 3.6V; V <sub>I</sub> = 5.5V		0.1	10	
		V <sub>CC</sub> = 3.6V; V <sub>I</sub> = 5.5V	I/O Data pins <sup>4</sup>	0.1	20	
		V <sub>CC</sub> = 3.6V; V <sub>I</sub> = V <sub>CC</sub>		0.1	10	
		V <sub>CC</sub> = 3.6V; V <sub>I</sub> = 0		0.1	-5	
I <sub>OFF</sub>	Output off current	V <sub>CC</sub> = 0V; V <sub>I</sub> or V <sub>O</sub> = 0 to 4.5V		0.1	±100	µA
I <sub>HOLD</sub>	Bus Hold current A or B outputs <sup>7</sup>	V <sub>CC</sub> = 3V; V <sub>I</sub> = 0.8V	75	135		µA
		V <sub>CC</sub> = 3V; V <sub>I</sub> = 2.0V	-75	-140		
		V <sub>CC</sub> = 0V to 3.6V; V <sub>CC</sub> = 3.6V	±500			
I <sub>EX</sub>	Current into an output in the High state when V <sub>O</sub> > V <sub>CC</sub>	V <sub>O</sub> = 5.5V; V <sub>CC</sub> = 3.0V		45	125	µA
I <sub>PU/PD</sub>	Power up/down 3-State output current <sup>3</sup>	V <sub>CC</sub> ≤ 1.2V; V <sub>O</sub> = 0.5V to V <sub>CC</sub> ; V <sub>I</sub> = GND or V <sub>CC</sub> ; OE/OE = Don't care		35	±100	µA
I <sub>CCH</sub>	Quiescent supply current	V <sub>CC</sub> = 3.6V; Outputs High, V <sub>I</sub> = GND or V <sub>CC</sub> , I <sub>O</sub> = 0		0.07	0.12	mA
I <sub>CCL</sub>		V <sub>CC</sub> = 3.6V; Outputs Low, V <sub>I</sub> = GND or V <sub>CC</sub> , I <sub>O</sub> = 0		4.9	6	
I <sub>CCZ</sub>		V <sub>CC</sub> = 3.6V; Outputs Disabled; V <sub>I</sub> = GND or V <sub>CC</sub> , I <sub>O</sub> = 0 <sup>6</sup>		0.07	0.12	
ΔI <sub>CC</sub>	Additional supply current per input pin <sup>2</sup>	V <sub>CC</sub> = 3V to 3.6V; One input at V <sub>CC</sub> -0.6V, Other inputs at V <sub>CC</sub> or GND		0.1	0.2	mA

NOTES:

1. All typical values are at V<sub>CC</sub> = 3.3V and T<sub>amb</sub> = 25°C.
2. This is the increase in supply current for each input at the specified voltage level other than V<sub>CC</sub> or GND
3. This parameter is valid for any V<sub>CC</sub> between 0V and 1.2V with a transition time of up to 10msec. From V<sub>CC</sub> = 1.2V to V<sub>CC</sub> = 3.3V ± 0.3V a transition time of 100µsec is permitted. This parameter is valid for T<sub>amb</sub> = 25°C only.
4. Unused pins at V<sub>CC</sub> or GND.
5. For valid test results, data must not be loaded into the flip-flops (or latches) after applying power.
6. I<sub>CCZ</sub> is measured with outputs pulled to V<sub>CC</sub> or GND.
7. This is the bus hold overdrive current required to force the input to the opposite logic state.

# 3.3V 16-bit bus transceiver/register (3-State)

74LVT16652A

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## AC CHARACTERISTICS

GND = 0V,  $t_R = t_F = 2.5\text{ns}$ ,  $C_L = 50\text{pF}$ ,  $R_L = 500\Omega$ ;  $T_{\text{amb}} = -40^\circ\text{C}$  to  $+85^\circ\text{C}$ .

SYMBOL	PARAMETER	WAVEFORM	LIMITS				UNIT
			$V_{CC} = 3.3V \pm 0.3V$			$V_{CC} = 2.7V$	
			MIN	TYP <sup>1</sup>	MAX	MAX	
$f_{\text{MAX}}$	Maximum clock frequency	1	150	180			MHz
$t_{\text{PLH}}$ $t_{\text{PHL}}$	Propagation delay nAx to nBx or nBx to nAx	2	0.5 0.5	1.9 1.9	3.7 3.7	4.0 4.0	ns
$t_{\text{PLH}}$ $t_{\text{PHL}}$	Propagation delay nCPAB to nBx or nCPBA to nAx	1	1.5 1.5	2.7 2.4	4.5 4.5	4.9 4.9	ns
$t_{\text{PLH}}$ $t_{\text{PHL}}$	Propagation delay nSAB to nBx or nSBA to nAx	3	1.0 1.0	2.3 2.8	4.8 4.8	5.4 5.4	ns
$t_{\text{PZH}}$ $t_{\text{PZL}}$	Output enable time nOEBA to nAx	5 6	1.0 1.0	2.7 2.5	4.6 4.6	5.0 5.0	ns
$t_{\text{PHZ}}$ $t_{\text{PLZ}}$	Output disable time nOEBA to nAx	5 6	1.5 1.5	3.9 2.9	4.9 4.9	4.8 4.6	ns
$t_{\text{PZH}}$ $t_{\text{PZL}}$	Output enable time nOEAB to nBx	5 6	1.0 1.0	2.9 2.7	4.6 4.6	5.0 5.0	ns
$t_{\text{PHZ}}$ $t_{\text{PLZ}}$	Output disable time nOEAB to nBx	5 6	1.5 1.5	3.1 2.8	4.9 4.9	5.2 4.6	ns

**NOTE:**

1. All typical values are at  $V_{CC} = 3.3V$  and  $T_{\text{amb}} = 25^\circ\text{C}$ .

## AC SETUP REQUIREMENTS

GND = 0V,  $t_R = 2.5\text{ns}$ ,  $t_F = 2.5\text{ns}$ ,  $C_L = 50\text{pF}$ ,  $R_L = 500\Omega$ ,  $T_{\text{amb}} = -40^\circ\text{C}$  to  $+85^\circ\text{C}$

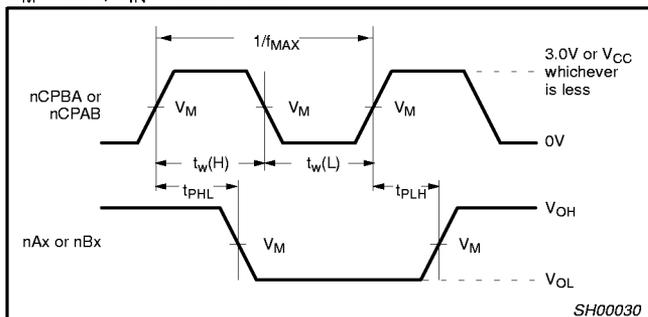
SYMBOL	PARAMETER	WAVEFORM	LIMITS			UNIT
			$V_{CC} = 3.3V \pm 0.3V$		$V_{CC} = 2.7V$	
			MIN	TYP	MIN	
$t_s(H)$ $t_s(L)$	Setup time 1 nAx to nCPAB, nBx to nCPBA	4	1.0 1.9	0.6 0.5	1.1 2.4	ns
$t_h(H)$ $t_h(L)$	Hold time 1 nAx to nCPAB, nBx to nCPBA	4	1.0 1.0	0.4 0.5	1.0 1.0	ns
$t_w(H)$ $t_w(L)$	Pulse width, High or Low nCPAB or nCPBA	1	2.6 2.8	2.2 2.4	2.6 2.8	ns

**NOTE:**

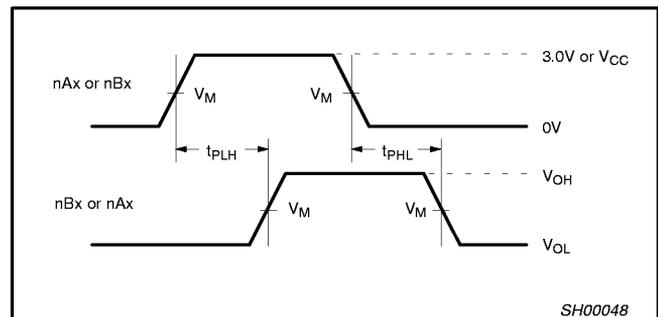
1. This data sheet limit may vary among suppliers.

## AC WAVEFORMS

$V_M = 1.5V$ ,  $V_{IN} = \text{GND}$  to  $3.0V$



**Waveform 1. Propagation Delay, Clock Input to Output, Clock Pulse Width, and Maximum Clock Frequency**

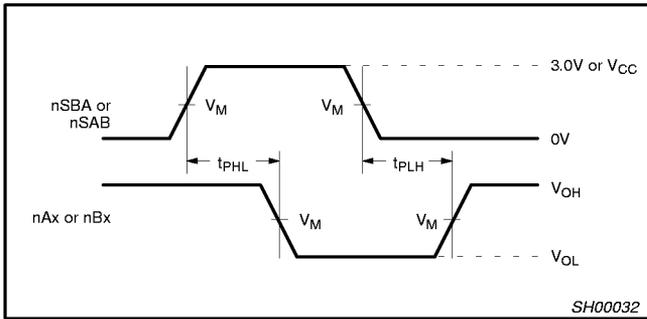


**Waveform 2. Propagation Delay, nAx to nBx or nBx to nAx**

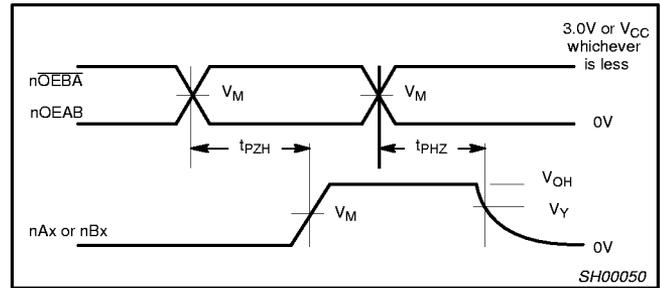
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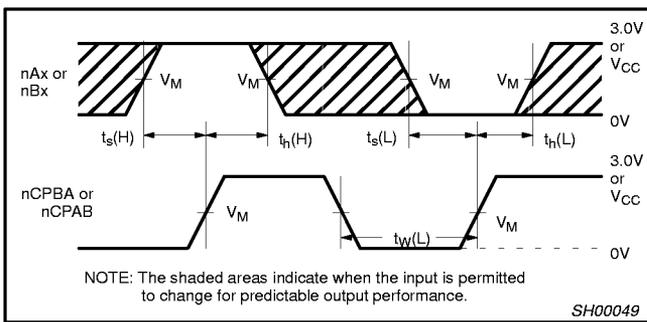
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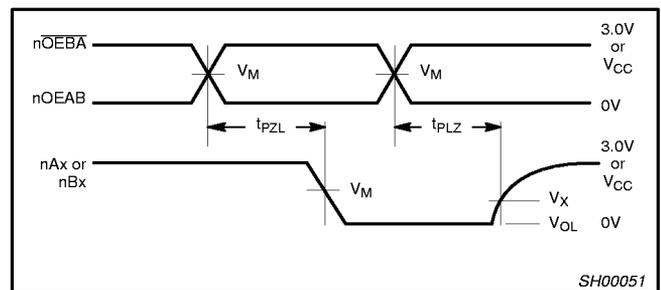
Waveform 3. Propagation Delay, SBA to nAx or SAB to nBx



Waveform 5. 3-State Output Enable Time to High Level and Output Disable Time from High Level



Waveform 4. Data Setup and Hold Times



Waveform 6. 3-State Output Enable Time to Low Level and Output Disable Time from Low Level

TEST CIRCUIT AND WAVEFORMS

**Test Circuit for 3-State Outputs**

**V<sub>M</sub> = 1.5V  
Input Pulse Definition**

**SWITCH POSITION**

TEST	SWITCH
t <sub>PHZ</sub> /t <sub>PZH</sub>	GND
t <sub>PLZ</sub> /t <sub>PZL</sub>	6V
t <sub>PLH</sub> /t <sub>PHL</sub>	open

**DEFINITIONS**

R<sub>L</sub> = Load resistor; see AC CHARACTERISTICS for value.

C<sub>L</sub> = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R<sub>T</sub> = Termination resistance should be equal to Z<sub>OUT</sub> of pulse generators.

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t <sub>w</sub>	t <sub>R</sub>	t <sub>F</sub>
74LVT16	2.7V	≤10MHz	500ns	≤2.5ns	≤2.5ns

SW00003

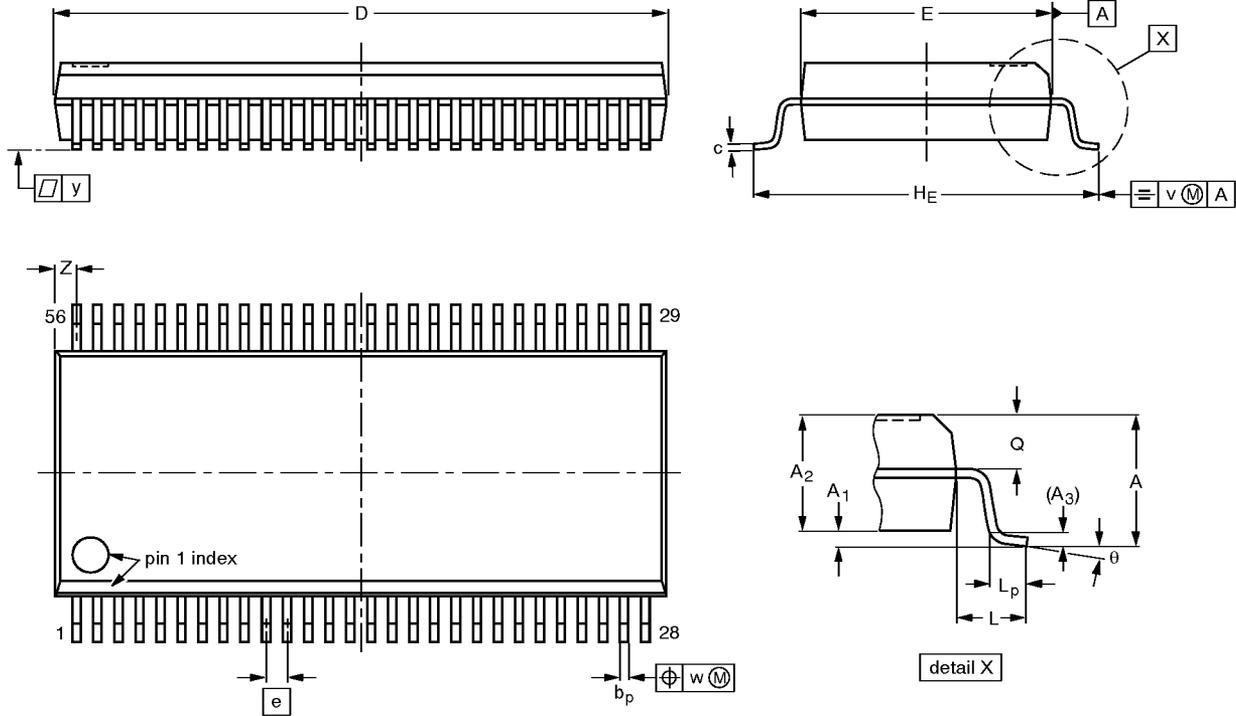
3.3V LVT 16-bit bus transceiver and registers

74LVT16652A

上海(Shanghai) 74LVT16652ADL-T"供应商

SSOP56: plastic shrink small outline package; 56 leads; body width 7.5 mm

SOT371-1



DIMENSIONS (mm are the original dimensions)

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(1)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z <sup>(1)</sup>	θ
mm	2.8	0.4 0.2	2.35 2.20	0.25	0.3 0.2	0.22 0.13	18.55 18.30	7.6 7.4	0.635	10.4 10.1	1.4	1.0 0.6	1.2 1.0	0.25	0.18	0.1	0.85 0.40	8° 0°

Note

1. Plastic or metal protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT371-1		MO-118AB				93-11-02 95-02-04

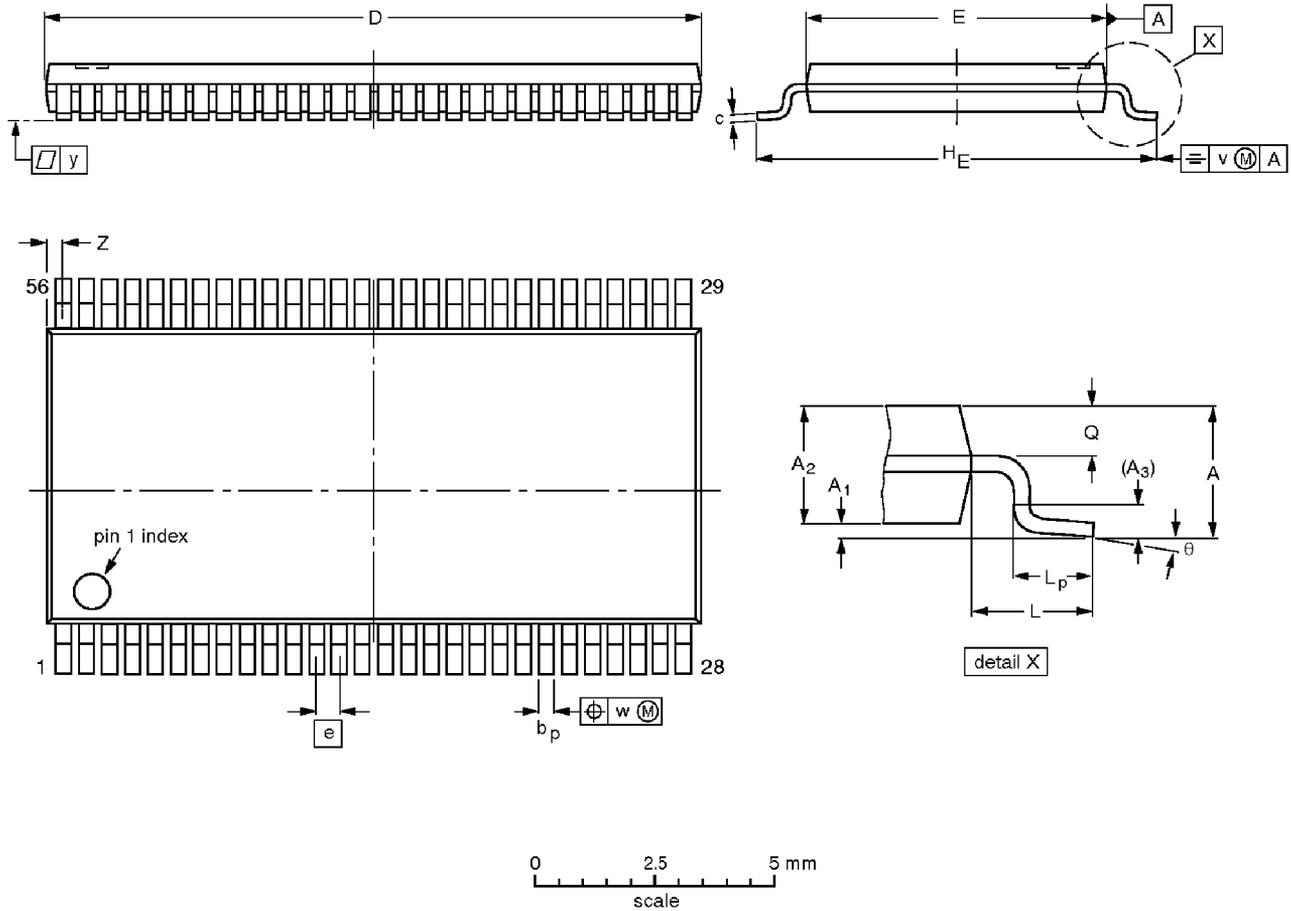
3.3V LVT 16-bit bus transceiver and registers

74LVT16652A

上海(Shanghai) "74LVT16652ADL-T" 供应商

TSSOP56: plastic thin shrink small outline package; 56 leads; body width 6.1mm

SOT364-1



DIMENSIONS (mm are the original dimensions).

UNIT	A max.	A <sub>1</sub>	A <sub>2</sub>	A <sub>3</sub>	b <sub>p</sub>	c	D <sup>(1)</sup>	E <sup>(2)</sup>	e	H <sub>E</sub>	L	L <sub>p</sub>	Q	v	w	y	Z	θ
mm	1.2	0.15 0.05	1.05 0.85	0.25	0.28 0.17	0.2 0.1	14.1 13.9	6.2 6.0	0.5	8.3 7.9	1.0	0.8 0.4	0.50 0.35	0.25	0.08	0.1	0.5 0.1	8° 0°

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT364-1		MO-153EE				<del>93-02-03</del> 95-02-10