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CY14B104L, CY14B104N

4 Mbit (512K x 8/256K x 16) nvSRAM

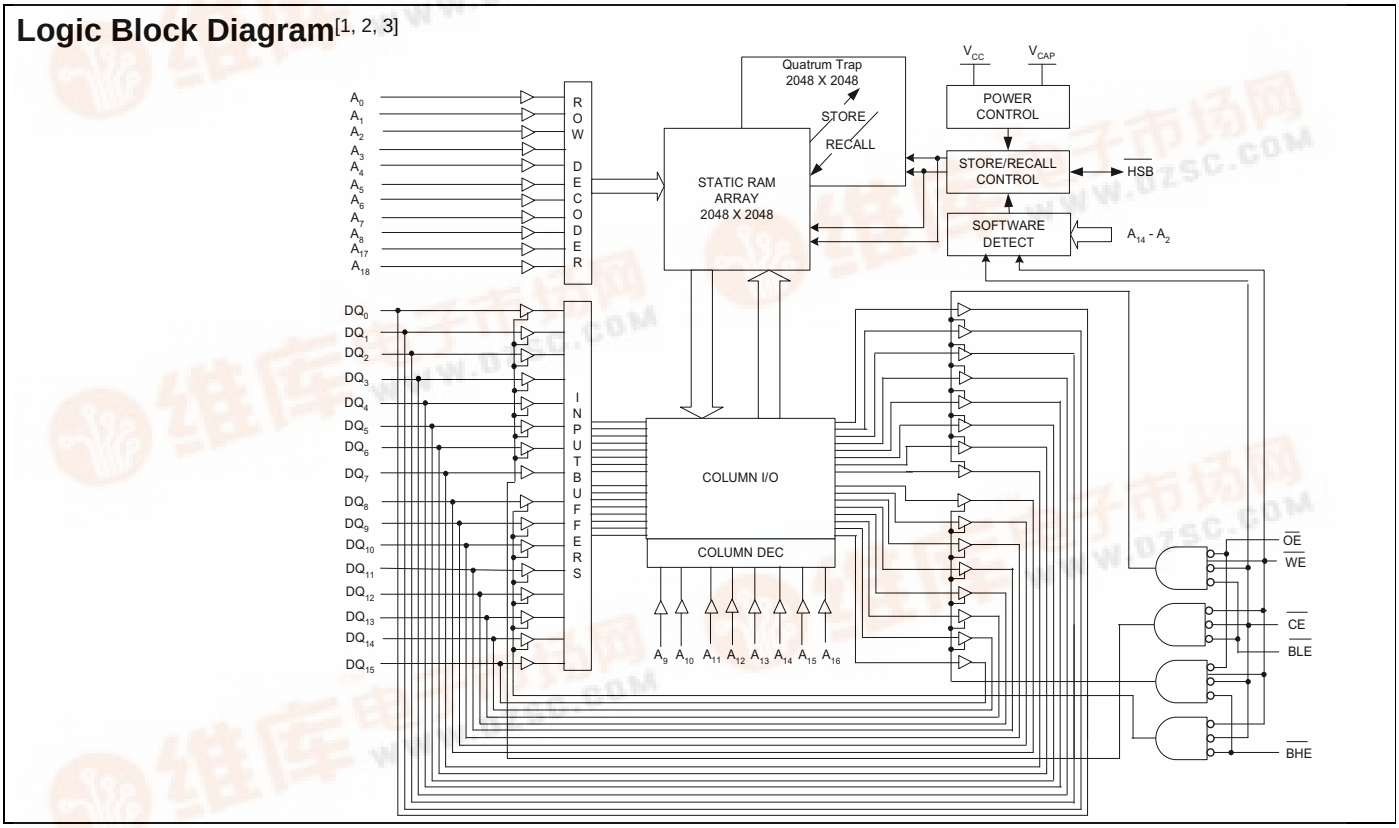
Features

- 20 ns, 25 ns, and 45 ns Access Times
- Internally organized as 512K x 8 (CY14B104L) or 256K x 16 (CY14B104N)
- Hands off Automatic STORE on power down with only a small Capacitor
- STORE to QuantumTrap® nonvolatile elements initiated by software, device pin, or AutoStore® on power down
- RECALL to SRAM initiated by software or power up
- Infinite Read, Write, and Recall Cycles
- 200,000 STORE cycles to QuantumTrap
- 20 year data retention
- Single 3V +20% to –10% operation
- Commercial and Industrial Temperatures
- 48-ball FBGA and 44/54-pin TSOP II packages
- Pb-free and RoHS compliance

Functional Description

The Cypress CY14B104L/CY14B104N is a fast static RAM, with a nonvolatile element in each memory cell. The memory is organized as 512K bytes of 8 bits each or 256K words of 16 bits each. The embedded nonvolatile elements incorporate QuantumTrap technology, producing the world's most reliable nonvolatile memory. The SRAM provides infinite read and write cycles, while independent nonvolatile data resides in the highly reliable QuantumTrap cell. Data transfers from the SRAM to the nonvolatile elements (the STORE operation) takes place automatically at power down. On power up, data is restored to the SRAM (the RECALL operation) from the nonvolatile memory. Both the STORE and RECALL operations are also available under software control.

Logic Block Diagram[1, 2, 3]



Notes

1. Address A_0 - A_{18} for x8 configuration and Address A_0 - A_{17} for x16 configuration.
2. Data DQ_0 - DQ_7 for x8 configuration and Data DQ_0 - DQ_{15} for x16 configuration.
3. BHE and BLE are applicable for x16 configuration only.

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Pinouts

Figure 1. Pin Diagram - 48 FBGA

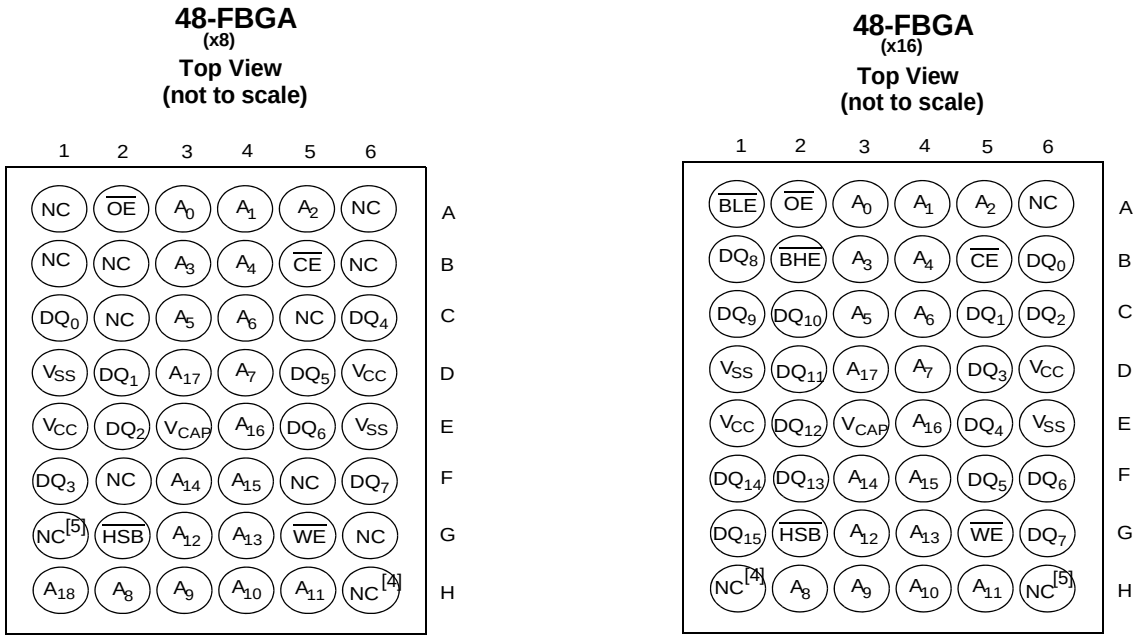
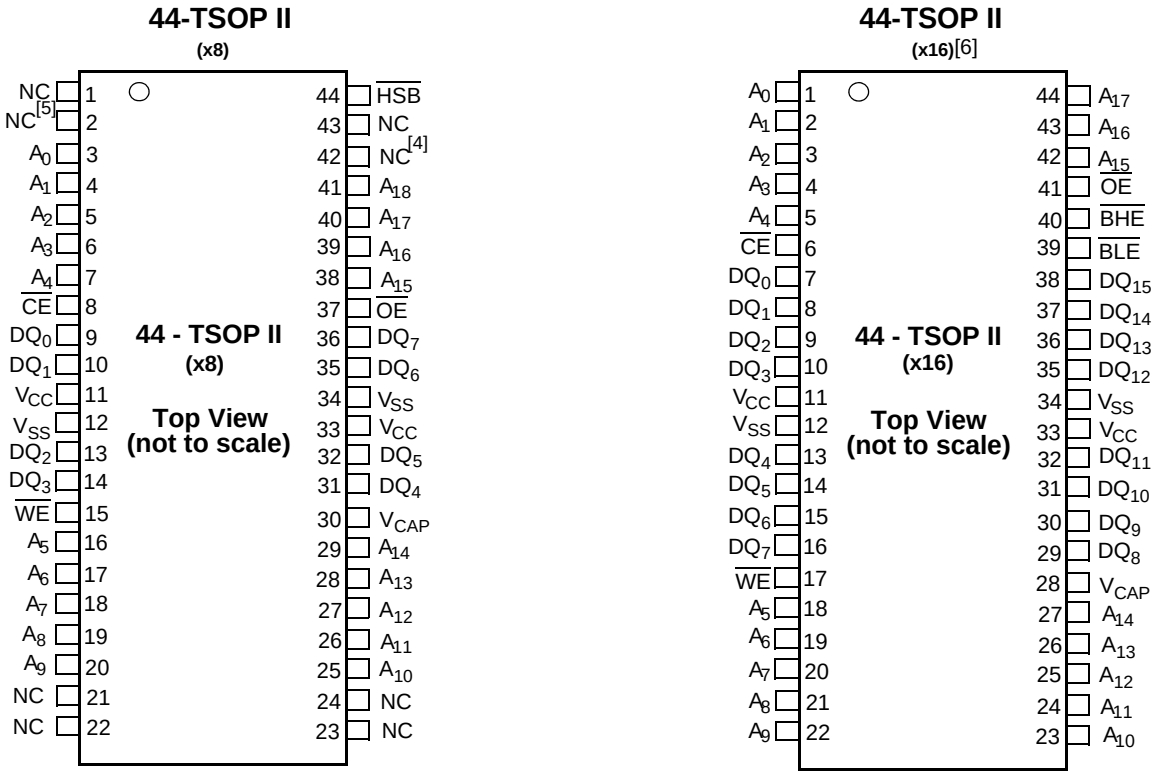


Figure 2. Pin Diagram - 44 Pin TSOP II



Notes
4. Address expansion for 8 Mbit. NC pin not connected to die.
5. Address expansion for 16 Mbit. NC pin not connected to die.
6. HSB pin is not available in 44-TSOP II (x16) package.

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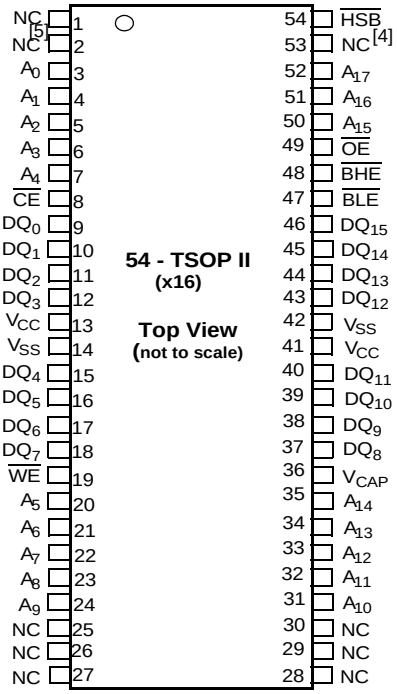
Pinouts (continued)

Figure 3. Pin Diagram - 54 Pin TSOP II (x16)



Pin Definitions

Pin Name	IO Type	Description
$A_0 – A_{18}$	Input	**Address Inputs Used to Select one of the 524,288 bytes of the nvSRAM for x8 Configuration**.
$A_0 – A_{17}$		**Address Inputs Used to Select one of the 262,144 words of the nvSRAM for x16 Configuration**.
$DQ_0 – DQ_7$	Input/Output	**Bidirectional Data IO Lines for x8 Configuration**. Used as input or output lines depending on operation.
$DQ_0 – DQ_{15}$		**Bidirectional Data IO Lines for x16 Configuration**. Used as input or output lines depending on operation.
$\overline{WE}$	Input	**Write Enable Input, Active LOW**. When selected LOW, data on the IO pins is written to the specific address location.
$\overline{CE}$	Input	**Chip Enable Input, Active LOW**. When LOW, selects the chip. When HIGH, deselects the chip.
$\overline{OE}$	Input	**Output Enable, Active LOW**. The active LOW $\overline{OE}$ input enables the data output buffers during read cycles. IO pins are tri-stated on deasserting $\overline{OE}$ HIGH.
$\overline{BHE}$	Input	**Byte High Enable, Active LOW**. Controls DQ_{15} - DQ_8.
$\overline{BLE}$	Input	**Byte Low Enable, Active LOW**. Controls DQ_7 - DQ_0.
V_{SS}	Ground	**Ground for the Device**. Must be connected to the ground of the system.
V_{CC}	Power Supply	**Power Supply Inputs to the Device**.
$\overline{HSB}$[6]	Input/Output	**Hardware Store Busy ($\overline{HSB}$)**. When LOW this output indicates that a hardware store is in progress. When pulled LOW external to the chip it initiates a nonvolatile STORE operation. A weak internal pull up resistor keeps this pin HIGH if not connected (connection optional). After each store operation HSB will be driven HIGH for short time with standard output high current.
V_{CAP}	Power Supply	**AutoStore Capacitor**. Supplies power to the nvSRAM during power loss to store data from SRAM to nonvolatile elements.
NC	No Connect	**No Connect**. This pin is not connected to the die.

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Device Operation

The CY14B104L/CY14B104N nvSRAM is made up of two functional components paired in the same physical cell. They are an SRAM memory cell and a nonvolatile QuantumTrap cell. The SRAM memory cell operates as a standard fast static RAM. Data in the SRAM is transferred to the nonvolatile cell (the STORE operation), or from the nonvolatile cell to the SRAM (the RECALL operation). Using this unique architecture, all cells are stored and recalled in parallel. During the STORE and RECALL operations, SRAM read and write operations are inhibited. The CY14B104L/CY14B104N supports infinite reads and writes similar to a typical SRAM. In addition, it provides infinite RECALL operations from the nonvolatile cells and up to 200K STORE operations. See the "Truth Table For SRAM Operations" on page 15 for a complete description of read and write modes.

SRAM Read

The CY14B104L/CY14B104N performs a read cycle when $\overline{CE}$ and $\overline{OE}$ are LOW and $\overline{WE}$ and $\overline{HSB}$ are HIGH. The address specified on pins A_{0-18} or A_{0-17} determines which of the 524,288 data bytes or 262,144 words of 16 bits each are accessed. Byte enables ($\overline{BHE}$, $\overline{BLE}$) determine which bytes are enabled to the output, in the case of 16-bit words. When the read is initiated by an address transition, the outputs are valid after a delay of t_{AA} (read cycle 1). If the read is initiated by $\overline{CE}$ or $\overline{OE}$, the outputs are valid at t_{ACE} or at t_{DOE}, whichever is later (read cycle 2). The data output repeatedly responds to address changes within the t_{AA} access time without the need for transitions on any control input pins. This remains valid until another address change or until $\overline{CE}$ or $\overline{OE}$ is brought HIGH, or $\overline{WE}$ or $\overline{HSB}$ is brought LOW.

SRAM Write

A write cycle is performed when $\overline{CE}$ and $\overline{WE}$ are LOW and $\overline{HSB}$ is HIGH. The address inputs must be stable before entering the write cycle and must remain stable until $\overline{CE}$ or $\overline{WE}$ goes HIGH at the end of the cycle. The data on the common IO pins $DQ_{0–15}$ are written into the memory if the data is valid t_{SD} before the end of a $\overline{WE}$ controlled write or before the end of an $\overline{CE}$ controlled write. The Byte Enable inputs ($\overline{BHE}$, $\overline{BLE}$) determine which bytes are written, in the case of 16bit words. It is recommended that $\overline{OE}$ be kept HIGH during the entire write cycle to avoid data bus contention on common IO lines. If $\overline{OE}$ is left LOW, internal circuitry turns off the output buffers t_{HZWE} after $\overline{WE}$ goes LOW.

AutoStore Operation

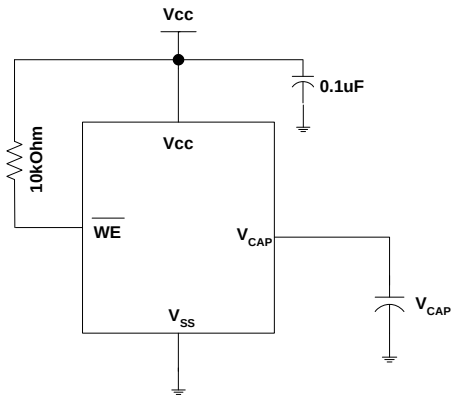
The CY14B104L/CY14B104N stores data to the nvSRAM using one of the following three storage operations: Hardware Store activated by $\overline{HSB}$; Software Store activated by an address sequence; AutoStore on device power down. The AutoStore operation is a unique feature of QuantumTrap technology and is enabled by default on the CY14B104L/CY14B104N.

During a normal operation, the device draws current from V_{CC} to charge a capacitor connected to the V_{CAP} pin. This stored charge is used by the chip to perform a single STORE operation. If the voltage on the V_{CC} pin drops below V_{SWITCH}, the part automatically disconnects the V_{CAP} pin from V_{CC}. A STORE operation is initiated with power provided by the V_{CAP} capacitor.

Figure 4 shows the proper connection of the storage capacitor (V_{CAP}) for automatic store operation. Refer to DC Electrical Characteristics on page 7 for the size of V_{CAP}. The voltage on the V_{CAP} pin is driven to V_{CC} by a regulator on the chip. A pull up should be placed on $\overline{WE}$ to hold it inactive during power up. This pull up is only effective if the $\overline{WE}$ signal is tri-state during power up. Many MPU's will tri-state their controls on power up. This should be verified when using the pull up. When the nvSRAM comes out of power-on-recall, the MPU must be active or the $\overline{WE}$ held inactive until the MPU comes out of reset.

To reduce unnecessary nonvolatile stores, AutoStore and hardware store operations are ignored unless at least one write operation has taken place since the most recent STORE or RECALL cycle. Software initiated STORE cycles are performed regardless of whether a write operation has taken place. The $\overline{HSB}$ signal is monitored by the system to detect if an AutoStore cycle is in progress.

Figure 4. AutoStore Mode



Hardware STORE Operation

The CY14B104L/CY14B104N provides the $\overline{HSB}$[6] pin to control and acknowledge the STORE operations. Use the HSB pin to request a hardware STORE cycle. When the HSB pin is driven LOW, the CY14B104L/CY14B104N conditionally initiates a STORE operation after t_{DELAY}. An actual STORE cycle only begins if a write to the SRAM has taken place since the last STORE or RECALL cycle. The $\overline{HSB}$ pin also acts as an open drain driver that is internally driven LOW to indicate a busy condition when the STORE (initiated by any means) is in progress.

When $\overline{HSB}$ is driven LOW by any means, SRAM read and write operations that are in progress are given time to complete before the STORE operation is initiated. After $\overline{HSB}$ goes LOW, the CY14B104L/CY14B104N continues SRAM operations for t_{DELAY}.

During any STORE operation, regardless of how it is initiated, the CY14B104L/CY14B104N continues to drive the $\overline{HSB}$ pin LOW, releasing it only when the STORE is complete. Upon completion of the STORE operation, the CY14B104L/CY14B104N remains disabled until the $\overline{HSB}$ pin returns HIGH. Leave the $\overline{HSB}$ unconnected if it is not used.

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Hardware RECALL (Power Up)

During power up or after any low power condition (V_{CC}< V_{SWITCH}), an internal RECALL request is latched. When V_{CC} again exceeds the sense voltage of V_{SWITCH}, a RECALL cycle is automatically initiated and takes $t_{HRECALL}$ to complete. During this time, HSB is driven LOW by the HSB driver.

Software STORE

Transfer data from the SRAM to the nonvolatile memory with a software address sequence. The CY14B104L/CY14B104N software STORE cycle is initiated by executing sequential CE controlled read cycles from six specific address locations in exact order. During the STORE cycle an erase of the previous nonvolatile data is performed, followed by a program of the nonvolatile elements. After a STORE cycle is initiated, further input and output are disabled until the cycle is completed.

Because a sequence of READs from specific addresses is used for STORE initiation, it is important that no other read or write accesses intervene in the sequence. Further, no read or write operations must be done after the sixth address read for a duration of soft-sequence processing time (t_{SS}). If these conditions are not met, the sequence is aborted and no STORE or RECALL takes place.

To initiate the software STORE cycle, the following addresses and read sequence must be performed.

1. Read Address 0x4E38 Valid READ
2. Read Address 0xB1C7 Valid READ
3. Read Address 0x83E0 Valid READ
4. Read Address 0x7C1F Valid READ
5. Read Address 0x703F Valid READ
6. Read Address 0x8FC0 Initiate STORE Cycle

The software sequence may be clocked with CE controlled reads or OE controlled reads. After the sixth address in the sequence is entered, the STORE cycle commences and the chip is disabled. HSB will be driven LOW. It is important to use read cycles and not write cycles in the sequence, although it is not necessary that OE be LOW for a valid sequence. After the t_{STORE} cycle time is fulfilled, the SRAM is activated again for the read and write operation.

Software RECALL

Transfer the data from the nonvolatile memory to the SRAM with a software address sequence. A software RECALL cycle is initiated with a sequence of read operations in a manner similar to the software STORE initiation. To initiate the RECALL cycle, the following sequence of CE controlled read operations must be performed.

1. Read Address 0x4E38 Valid READ
2. Read Address 0xB1C7 Valid READ
3. Read Address 0x83E0 Valid READ
4. Read Address 0x7C1F Valid READ
5. Read Address 0x703F Valid READ
6. Read Address 0x4C63 Initiate RECALL Cycle

Internally, RECALL is a two step procedure. First, the SRAM data is cleared; then, the nonvolatile information is transferred into the SRAM cells. After the t_{RECALL} cycle time, the SRAM is again ready for read and write operations. The RECALL operation does not alter the data in the nonvolatile elements.

Table 1. Mode Selection

CE	WE	OE, BHE, BLE[3]	A_{15} - A_0[7]	Mode	IO	Power
H	X	X	X	Not Selected	Output High Z	Standby
L	H	L	X	Read SRAM	Output Data	Active
L	L	X	X	Write SRAM	Input Data	Active
L	H	L	0x4E38 0xB1C7 0x83E0 0x7C1F 0x703F 0x8B45	Read SRAM Read SRAM Read SRAM Read SRAM Read SRAM AutoStore Disable	Output Data Output Data Output Data Output Data Output Data Output Data	Active[8, 9]

Notes

7. While there are 19 address lines on the CY14B104L (18 address lines on the CY14B104N), only the 13 address lines (A_{14} - A_2) are used to control software modes. The rest of the address lines are don't care.
8. The six consecutive address locations must be in the order listed. WE must be HIGH during all six cycles to enable a nonvolatile cycle.
9. IO state depends on the state of OE, BHE, and BLE. The IO table shown assumes OE, BHE, and BLE LOW.

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Table 1. Mode Selection (continued)

$\overline{CE}$	$\overline{WE}$	$\overline{OE}$, $\overline{BHE}$, $\overline{BLE}$[3]	A_{15} - A_0[7]	Mode	IO	Power
L	H	L	0x4E38 0xB1C7 0x83E0 0x7C1F 0x703F 0x4B46	Read SRAM Read SRAM Read SRAM Read SRAM Read SRAM AutoStore Enable	Output Data Output Data Output Data Output Data Output Data Output Data	Active[8, 9]
L	H	L	0x4E38 0xB1C7 0x83E0 0x7C1F 0x703F 0x8FC0	Read SRAM Read SRAM Read SRAM Read SRAM Read SRAM Nonvolatile Store	Output Data Output Data Output Data Output Data Output Data Output High Z	Active I_{CC2}[8, 9]
L	H	L	0x4E38 0xB1C7 0x83E0 0x7C1F 0x703F 0x4C63	Read SRAM Read SRAM Read SRAM Read SRAM Read SRAM Nonvolatile Recall	Output Data Output Data Output Data Output Data Output Data Output High Z	Active[8, 9]

Preventing AutoStore

The AutoStore function is disabled by initiating an AutoStore disable sequence. A sequence of read operations is performed in a manner similar to the software STORE initiation. To initiate the AutoStore disable sequence, the following sequence of $\overline{CE}$ controlled read operations must be performed:

1. Read address 0x4E38 Valid READ
2. Read address 0xB1C7 Valid READ
3. Read address 0x83E0 Valid READ
4. Read address 0x7C1F Valid READ
5. Read address 0x703F Valid READ
6. Read address 0x8B45 AutoStore Disable

The AutoStore is re-enabled by initiating an AutoStore enable sequence. A sequence of read operations is performed in a manner similar to the software RECALL initiation. To initiate the AutoStore enable sequence, the following sequence of $\overline{CE}$ controlled read operations must be performed:

1. Read address 0x4E38 Valid READ
2. Read address 0xB1C7 Valid READ
3. Read address 0x83E0 Valid READ
4. Read address 0x7C1F Valid READ
5. Read address 0x703F Valid READ
6. Read address 0x4B46 AutoStore Enable

If the AutoStore function is disabled or re-enabled, a manual STORE operation (hardware or software) must be issued to save the AutoStore state through subsequent power down cycles. The part comes from the factory with AutoStore enabled.

Data Protection

The CY14B104L/CY14B104N protects data from corruption during low voltage conditions by inhibiting all externally initiated STORE and write operations. The low voltage condition is detected when $V_{CC} < V_{SWITCH}$. If the CY14B104L/CY14B104N is in a write mode (both $\overline{CE}$ and $\overline{WE}$ are LOW) at power up, after a RECALL or STORE, the write is inhibited until the SRAM is enabled after t_{LZHSB} (HSB to output active). This protects against inadvertent writes during power up or brown out conditions.

Noise Considerations

Refer to CY application note AN1064.

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Maximum Ratings

Exceeding maximum ratings may impair the useful life of the device. These user guidelines are not tested.

Storage Temperature ..... –65°C to +150°C

Maximum Accumulated Storage Time

At 150°C Ambient Temperature 1000h

At 85°C Ambient Temperature ..... 20 Years

Ambient Temperature with Power Applied ..... –55°C to +150°C

Supply Voltage on V_{CC} Relative to GND .....–0.5V to 4.1V

Voltage Applied to Outputs in High-Z State..... –0.5V to V_{CC} + 0.5V

Input Voltage..... –0.5V to V_{CC} + 0.5V

Transient Voltage (<20 ns) on Any Pin to Ground Potential ..... –2.0V to V_{CC} + 2.0V

Package Power Dissipation Capability (T_A = 25°C) 1.0W

Surface Mount Pb Soldering Temperature (3 Seconds) ..... +260°C

DC Output Current (1 output at a time, 1s duration).... 15 mA

Static Discharge Voltage..... > 2001V (per MIL-STD-883, Method 3015)

Latch Up Current ..... > 200 mA

Operating Range

Range	Ambient Temperature	V_{CC}
Commercial	0°C to +70°C	2.7V to 3.6V
Industrial	–40°C to +85°C	2.7V to 3.6V

DC Electrical Characteristics

Over the Operating Range (V_{CC} = 2.7V to 3.6V)

Parameter	Description	Test Conditions		Min	Max	Unit
I_{CC1}	Average V_{CC} Current	t_{RC} = 20 ns t_{RC} = 25 ns t_{RC} = 45 ns Values obtained without output loads (I_{OUT} = 0 mA)	Commercial		65 65 50	mA mA mA
			Industrial		70 70 52	mA mA mA
I_{CC2}	Average V_{CC} Current during STORE	All Inputs Don't Care, V_{CC} = Max Average current for duration t_{STORE}			10	mA
I_{CC3}[10]	Average V_{CC} Current at t_{RC}= 200 ns, 3V, 25°C typical	All inputs cycling at CMOS levels. Values obtained without output loads (I_{OUT} = 0 mA).			35	mA
I_{CC4}	Average V_{CAP} Current during AutoStore Cycle	All Inputs Don't Care, V_{CC} = Max Average current for duration t_{STORE}			5	mA
I_{SB}	V_{CC} Standby Current	$\overline{CE} \geq (V_{CC} - 0.2V)$. All others $V_{IN} \leq 0.2V$ or $\geq (V_{CC} - 0.2V)$. Standby current level after nonvolatile cycle is complete. Inputs are static. f = 0 MHz.			5	mA
I_{IX}[11]	Input Leakage Current (except HSB)	V_{CC} = Max, $V_{SS} \leq V_{IN} \leq V_{CC}$		–1	+1	µA
	Input Leakage Current (for HSB)	V_{CC} = Max, $V_{SS} \leq V_{IN} \leq V_{CC}$		–100	+1	µA
I_{OZ}	Off-State Output Leakage Current	V_{CC} = Max, $V_{SS} \leq V_{OUT} \leq V_{CC}$, $\overline{CE}$ or $\overline{OE} \geq V_{IH}$ or $\overline{BHE}/\overline{BLE} \geq V_{IH}$ or $\overline{WE} \leq V_{IL}$		–1	+1	µA
V_{IH}	Input HIGH Voltage			2.0	V_{CC} + 0.5	V
V_{IL}	Input LOW Voltage			V_{SS} – 0.5	0.8	V
V_{OH}	Output HIGH Voltage	I_{OUT} = –2 mA		2.4		V
V_{OL}	Output LOW Voltage	I_{OUT} = 4 mA			0.4	V
V_{CAP}[12]	Storage Capacitor	Between V_{CAP} pin and V_{SS}, 5V Rated		61	180	µF

Notes

10. Typical conditions for the active current shown on the DC Electrical characteristics are average values at 25°C (room temperature), and V_{CC} = 3V. Not 100% tested.
11. The $\overline{HSB}$ pin has I_{OUT} = -2 µA for V_{OH} of 2.4V when both active HIGH and LOW drivers are disabled. When they are enabled standard V_{OH} and V_{OL} are valid. This parameter is characterized but not tested.
12. V_{CAP} (Storage capacitor) nominal value is 68 µF.

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Data Retention and Endurance

Parameter	Description	Min	Unit
$DATA_R$	Data Retention	20	Years
NV_C	Nonvolatile STORE Operations	200	K

Capacitance

In the following table, the capacitance parameters are listed.[13]

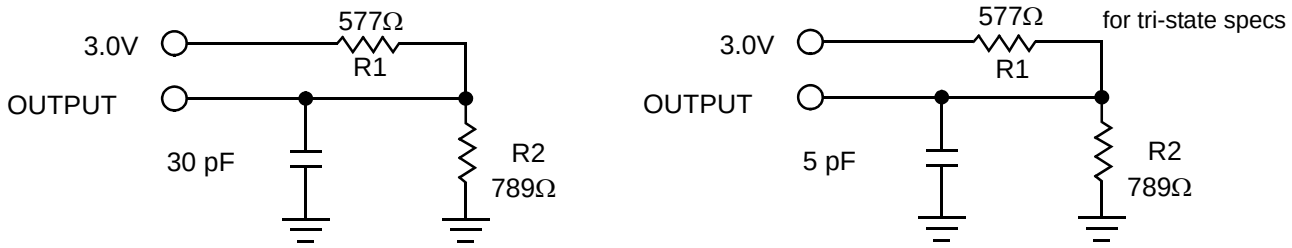
Parameter	Description	Test Conditions	Max	Unit
C_{IN}	Input Capacitance	T_A = 25°C, f = 1 MHz, V_{CC} = 0 to 3.0V	7	pF
C_{OUT}	Output Capacitance		7	pF

Thermal Resistance

In the following table, the thermal resistance parameters are listed. [13]

Parameter	Description	Test Conditions	48-FBGA	44-TSOP II	54-TSOP II	Unit
Θ_{JA}	Thermal Resistance (Junction to Ambient)	Test conditions follow standard test methods and procedures for measuring thermal impedance, in accordance with EIA/JESD51.	28.82	31.11	30.73	°C/W
Θ_{JC}	Thermal Resistance (Junction to Case)		7.84	5.56	6.08	°C/W

Figure 5. AC Test Loads



AC Test Conditions

Input Pulse Levels..... 0V to 3V
Input Rise and Fall Times (10% - 90%)..... ≤3 ns
Input and Output Timing Reference Levels..... 1.5V

Note
13. These parameters are guaranteed but not tested.

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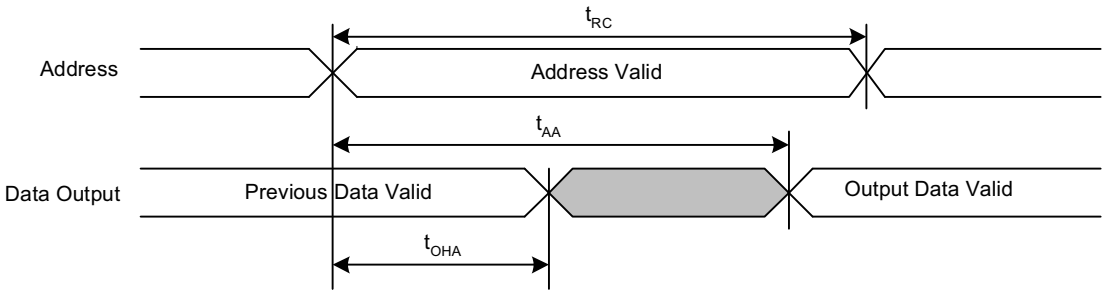
AC Switching Characteristics

Parameters		Description	20 ns		25 ns		45 ns		Unit
Cypress Parameters	Alt Parameters		Min	Max	Min	Max	Min	Max	
SRAM Read Cycle									
t_{ACE}	t_{ACS}	Chip Enable Access Time		20		25		45	ns
t_{RC}[14]	t_{RC}	Read Cycle Time	20		25		45		ns
t_{AA}[15]	t_{AA}	Address Access Time		20		25		45	ns
t_{DOE}	t_{OE}	Output Enable to Data Valid		10		12		20	ns
t_{OHA}[15]	t_{OH}	Output Hold After Address Change	3		3		3		ns
t_{LZCE}[16]	t_{LZ}	Chip Enable to Output Active	3		3		3		ns
t_{HZCE}[16]	t_{HZ}	Chip Disable to Output Inactive		8		10		15	ns
t_{LZOE}[16]	t_{OLZ}	Output Enable to Output Active	0		0		0		ns
t_{HZOE}[16]	t_{OHZ}	Output Disable to Output Inactive		8		10		15	ns
t_{PU}[13]	t_{PA}	Chip Enable to Power Active	0		0		0		ns
t_{PD}[13]	t_{PS}	Chip Disable to Power Standby		20		25		45	ns
t_{DBE}	-	Byte Enable to Data Valid		10		12		20	ns
t_{LZBE}	-	Byte Enable to Output Active	0		0		0		ns
t_{HZBE}	-	Byte Disable to Output Inactive		8		10		15	ns
SRAM Write Cycle									
t_{WC}	t_{WC}	Write Cycle Time	20		25		45		ns
t_{PWE}	t_{WP}	Write Pulse Width	15		20		30		ns
t_{SCE}	t_{CW}	Chip Enable To End of Write	15		20		30		ns
t_{SD}	t_{DW}	Data Setup to End of Write	8		10		15		ns
t_{HD}	t_{DH}	Data Hold After End of Write	0		0		0		ns
t_{AW}	t_{AW}	Address Setup to End of Write	15		20		30		ns
t_{SA}	t_{AS}	Address Setup to Start of Write	0		0		0		ns
t_{HA}	t_{WR}	Address Hold After End of Write	0		0		0		ns
t_{HZWE}[16,17]	t_{WZ}	Write Enable to Output Disable		8		10		15	ns
t_{LZWE}[16]	t_{OW}	Output Active after End of Write	3		3		3		ns
t_{BW}	-	Byte Enable to End of Write	15		20		30		ns

Switching Waveforms

Figure 6. SRAM Read Cycle #1: Address Controlled[14, 15, 18]



Notes
14. WE must be HIGH during SRAM read cycles.
15. Device is continuously selected with CE, OE and BHE / BLE LOW.
16. Measured ±200 mV from steady state output voltage.
17. If WE is LOW when CE goes LOW, the outputs remain in the high impedance state.
18. HSB must remain HIGH during READ and WRITE cycles.

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Figure 7. SRAM Read Cycle #2: $\overline{CE}$ and $\overline{OE}$ Controlled[3, 14, 18]

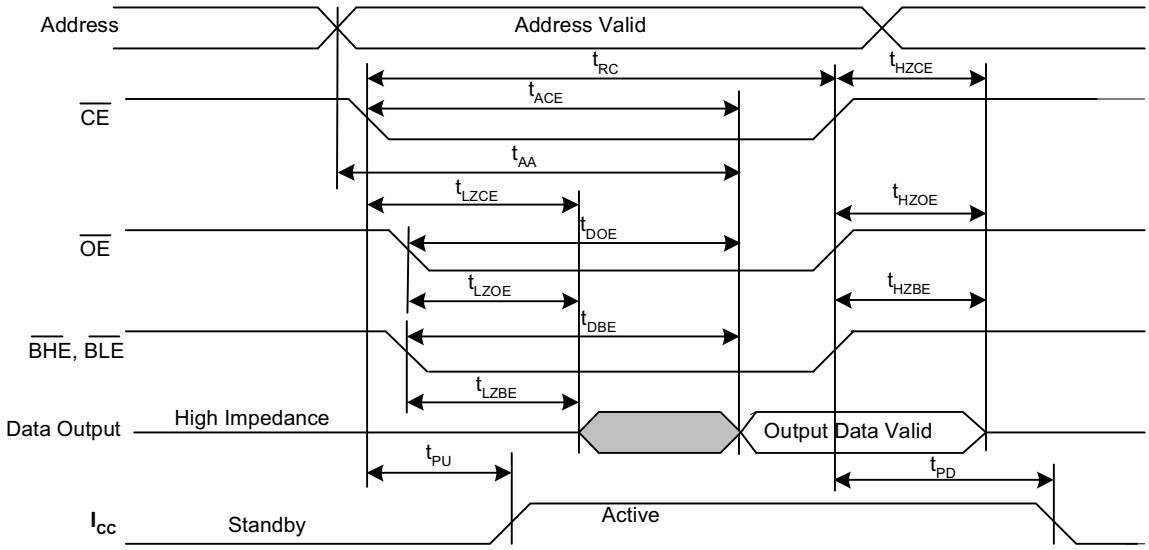
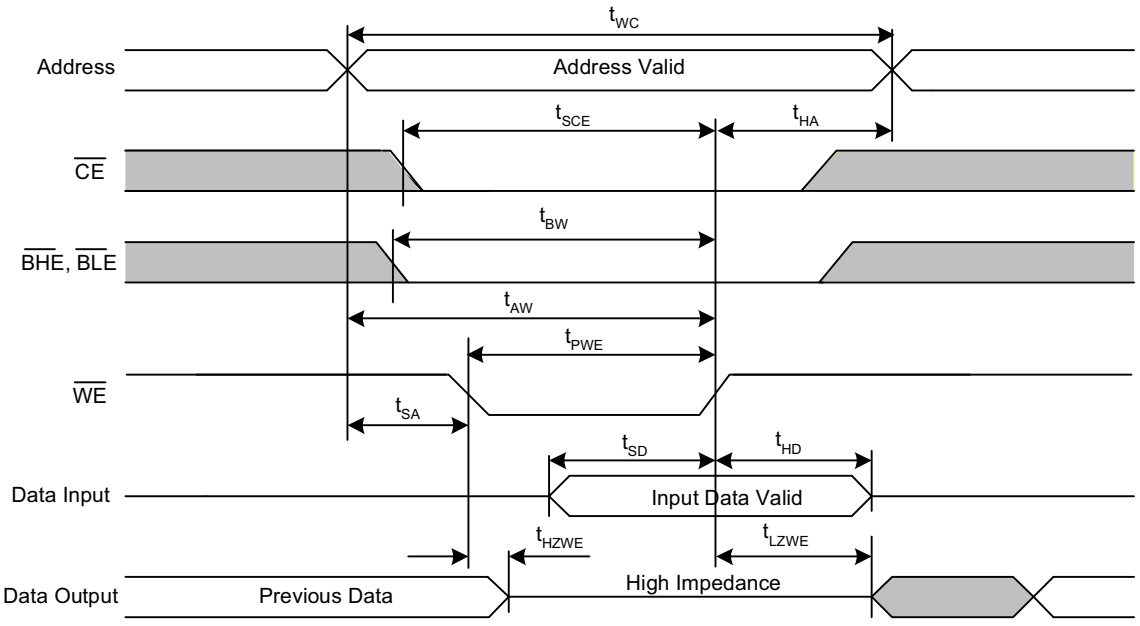


Figure 8. SRAM Write Cycle #1: $\overline{WE}$ Controlled[3, 17, 18, 19]



Notes
19. $\overline{CE}$ or $\overline{WE}$ must be $\geq V_{IH}$ during address transitions.

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Figure 9. SRAM Write Cycle #2: $\overline{CE}$ Controlled[3, 17, 18, 19]

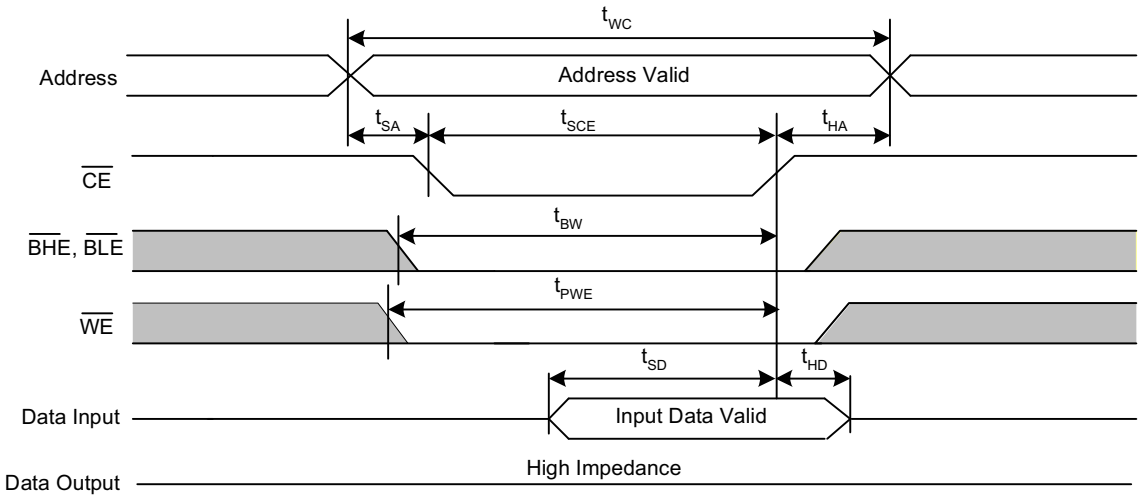
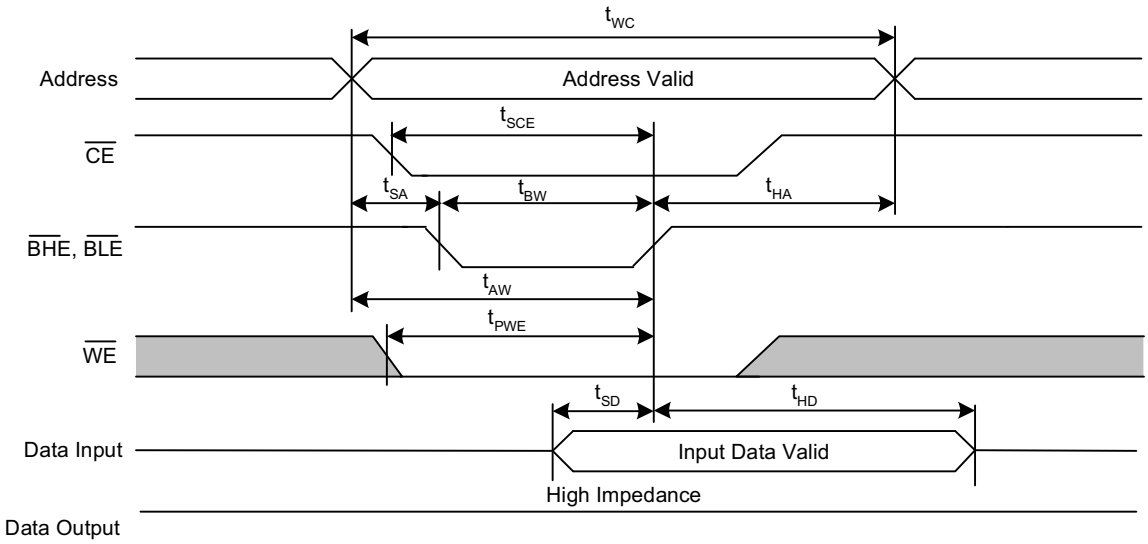


Figure 10. SRAM Write Cycle #3: $\overline{BHE}$ and $\overline{BLE}$ Controlled[3, 17, 18, 19]



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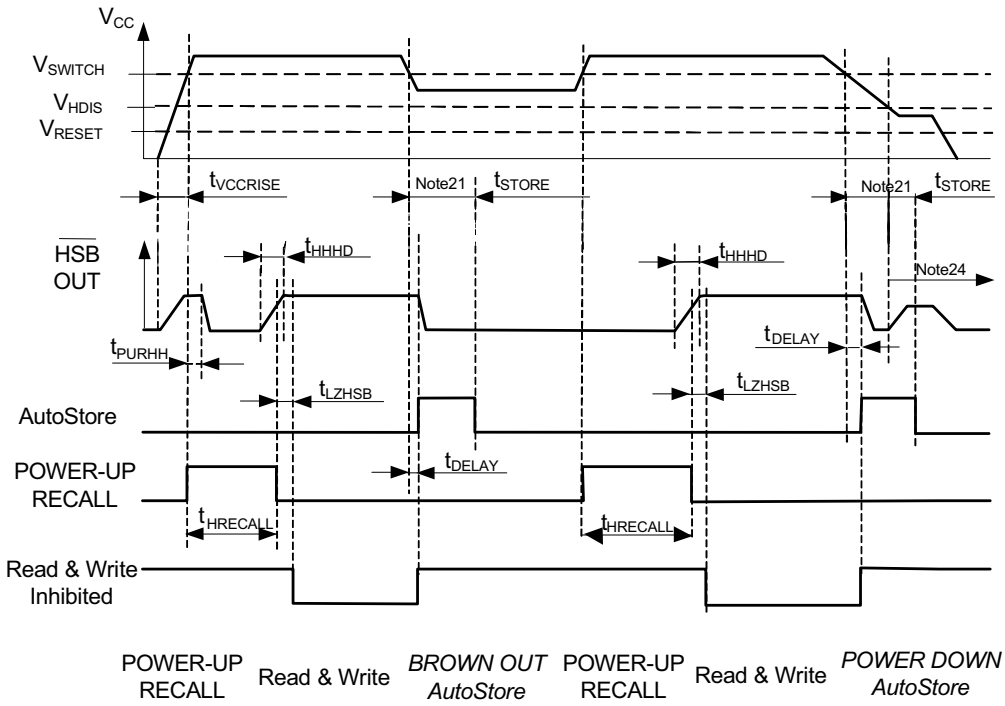
AutoStore/Power Up RECALL

Parameters	Description	CY14B104L/CY14B104N		Unit
		Min	Max	
$t_{HRECALL}$ [20]	Power Up RECALL Duration		20	ms
t_{STORE} [21]	STORE Cycle Duration		8	ms
t_{DELAY} [22]	Time Allowed to Complete SRAM Cycle	1	70	µs
V_{SWITCH}	Low Voltage Trigger Level		2.65	V
$t_{VCCRISE}$	VCC Rise Time	150		µs
V_{HDIS} [13]	$\overline{HSB}$ Output Driver Disable Voltage		1.9	V
t_{HHHD}	$\overline{HSB}$ High Active Time		500	ns
t_{PURHH}	$\overline{HSB}$ Hold Time after Power-Up Recall Start	70		µs
t_{LZHSB}	$\overline{HSB}$ To Output Active Time		5	µs

Switching Waveforms

Figure 11. AutoStore or Power Up RECALL [23]



Notes
20. $t_{HRECALL}$ starts from the time V_{CC} rises above V_{SWITCH}.
21. If an SRAM write has not taken place since the last nonvolatile cycle, no AutoStore or Hardware Store takes place.
22. On a Hardware STORE, Software STORE/RECALL, AutoStore Enable/Disable and AutoStore initiation, SRAM operation continues to be enabled for time t_{DELAY}.
23. Read and Write cycles are ignored during STORE, RECALL, and while V_{CC} is below V_{SWITCH}.
24. $\overline{HSB}$ pin is driven HIGH to V_{CC} only by internal 100 kΩ resistor, $\overline{HSB}$ driver is disabled.

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Software Controlled STORE/RECALL Cycle

In the following table, the software controlled STORE/RECALL cycle parameters are listed.[25, 26]

Parameters	Description	20 ns		25 ns		45 ns		Unit
		Min	Max	Min	Max	Min	Max	
t_{RC}	STORE/RECALL Initiation Cycle Time	20		25		45		ns
t_{SA}	Address Setup Time	0		0		0		ns
t_{CW}	Clock Pulse Width	15		20		30		ns
t_{HA}	Address Hold Time	0		0		0		ns
t_{RECALL}	RECALL Duration		200		200		200	µs
t_{SS} [27, 28]	Soft Sequence Processing Time		100		100		100	µs

Switching Waveforms

Figure 12. $\overline{CE}$ and $\overline{OE}$ Controlled Software STORE/RECALL Cycle[26]

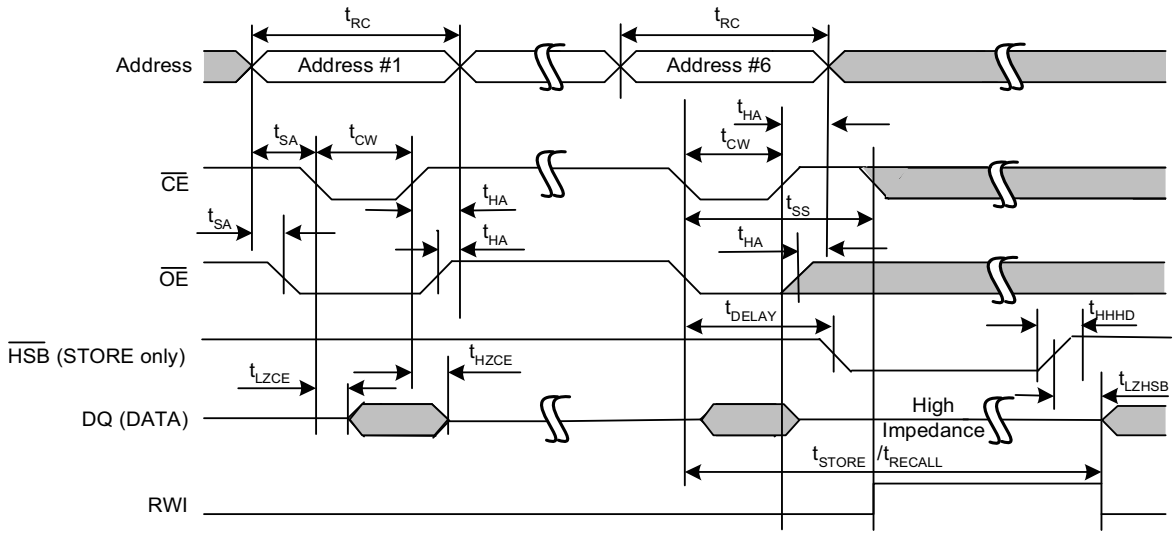
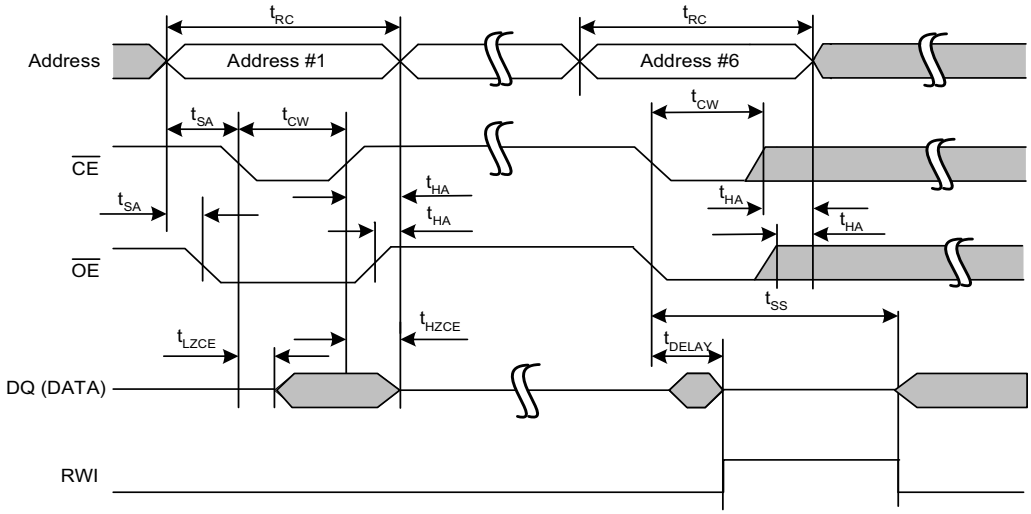


Figure 13. Autostore Enable / Disable Cycle



Notes

25. The software sequence is clocked with $\overline{CE}$ controlled or $\overline{OE}$ controlled reads.
26. The six consecutive addresses must be read in the order listed in Table 1 on page 5. $\overline{WE}$ must be HIGH during all six consecutive cycles. After the sixth address read cycle, no further read or write operation must be performed for t_{SS} duration. If these conditions are not met, the software sequence is aborted.

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Hardware STORE Cycle

Parameters	Description	CY14B104L/CY14B104N		Unit
		Min	Max	
t_{PHSB}	Hardware STORE Pulse Width	15		ns
t_{HLBL}	Hardware STORE LOW to STORE Busy		500	ns

Switching Waveforms

Figure 14. Hardware STORE Cycle[21]

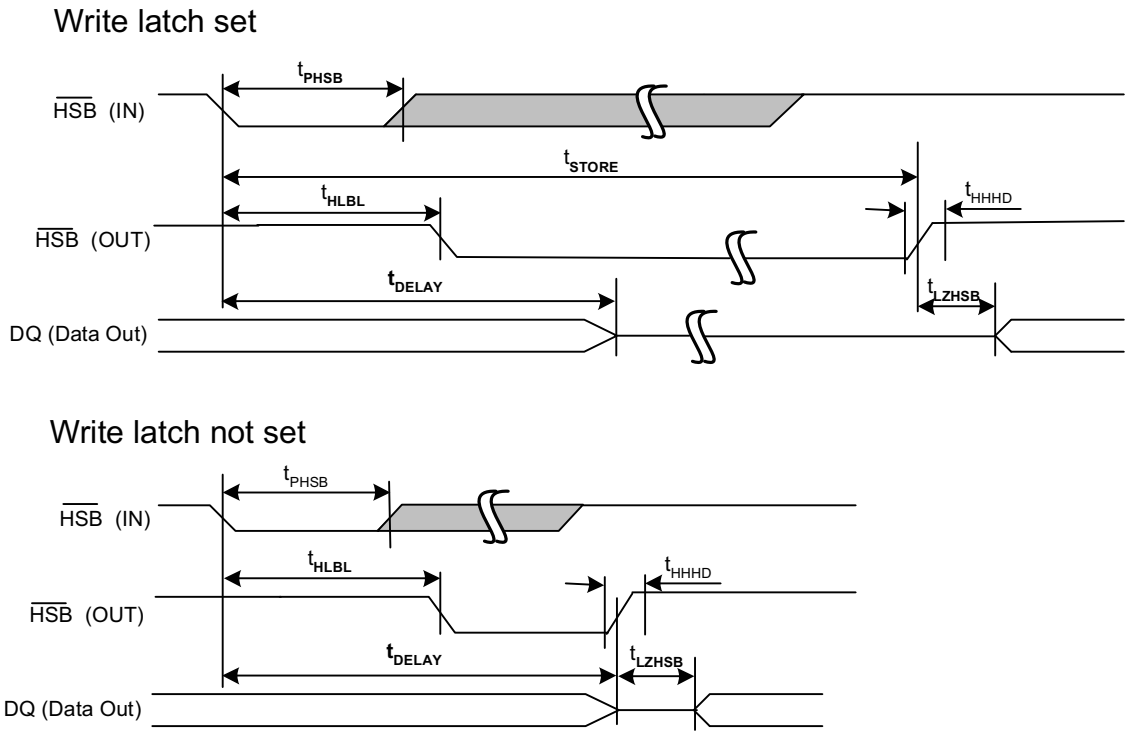
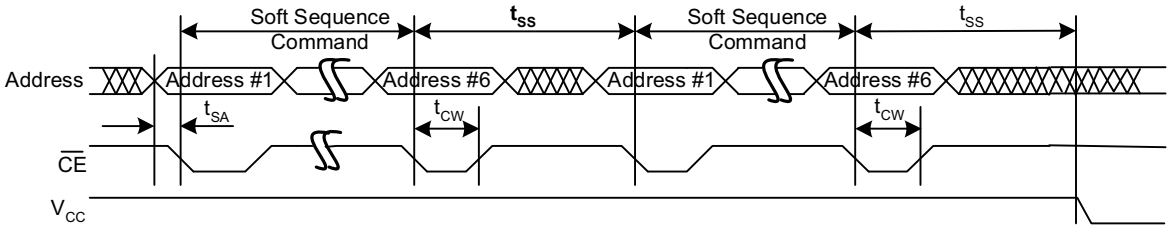


Figure 15. Soft Sequence Processing[27, 28]



Notes
27. This is the amount of time it takes to take action on a soft sequence command. V_{CC} power must remain HIGH to effectively register command.
28. Commands such as STORE and RECALL lock out IO until operation is complete which further increases this time. See the specific command.

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Truth Table For SRAM Operations

$\overline{HSB}$ should remain HIGH for SRAM Operations.

For x8 Configuration

$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	Inputs/Outputs[2]	Mode	Power
H	X	X	High Z	Deselect/Power down	Standby
L	H	L	Data Out (DQ_0–DQ_7);	Read	Active
L	H	H	High Z	Output Disabled	Active
L	L	X	Data in (DQ_0–DQ_7);	Write	Active

For x16 Configuration

$\overline{CE}$	$\overline{WE}$	$\overline{OE}$	$\overline{BHE}$	$\overline{BLE}$	Inputs/Outputs[2]	Mode	Power
H	X	X	X	X	High-Z	Deselect/Power down	Standby
L	X	X	H	H	High-Z	Output Disabled	Active
L	H	L	L	L	Data Out (DQ_0–DQ_{15})	Read	Active
L	H	L	H	L	Data Out (DQ_0–DQ_7); DQ_8–DQ_{15} in High-Z	Read	Active
L	H	L	L	H	Data Out (DQ_8–DQ_{15}); DQ_0–DQ_7 in High-Z	Read	Active
L	H	H	L	L	High-Z	Output Disabled	Active
L	H	H	H	L	High-Z	Output Disabled	Active
L	H	H	L	H	High-Z	Output Disabled	Active
L	L	X	L	L	Data In (DQ_0–DQ_{15})	Write	Active
L	L	X	H	L	Data In (DQ_0–DQ_7); DQ_8–DQ_{15} in High-Z	Write	Active
L	L	X	L	H	Data In (DQ_8–DQ_{15}); DQ_0–DQ_7 in High-Z	Write	Active

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Ordering Information

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
20	CY14B104L-ZS20XCT	51-85087	44-pin TSOP II	Commercial
	CY14B104L-ZS20XIT	51-85087	44-pin TSOP II	Industrial
	CY14B104L-ZS20XI	51-85087	44-pin TSOP II	
	CY14B104L-BA20XCT	51-85128	48-ball FBGA	Commercial
	CY14B104L-BA20XIT	51-85128	48-ball FBGA	Industrial
	CY14B104L-BA20XI	51-85128	48-ball FBGA	
	CY14B104L-ZSP20XCT	51-85160	54-pin TSOP II	Commercial
	CY14B104L-ZSP20XIT	51-85160	54-pin TSOP II	Industrial
	CY14B104L-ZSP20XI	51-85160	54-pin TSOP II	
	CY14B104N-ZS20XCT	51-85087	44-pin TSOP II	Commercial
	CY14B104N-ZS20XIT	51-85087	44-pin TSOP II	Industrial
	CY14B104N-ZS20XI	51-85087	44-pin TSOP II	
	CY14B104N-BA20XCT	51-85128	48-ball FBGA	Commercial
	CY14B104N-BA20XIT	51-85128	48-ball FBGA	Industrial
	CY14B104N-BA20XI	51-85128	48-ball FBGA	
	CY14B104N-ZSP20XCT	51-85160	54-pin TSOP II	Commercial
	CY14B104N-ZSP20XIT	51-85160	54-pin TSOP II	Industrial
	CY14B104N-ZSP20XI	51-85160	54-pin TSOP II	
25	CY14B104L-ZS25XCT	51-85087	44-pin TSOP II	Commercial
	CY14B104L-ZS25XIT	51-85087	44-pin TSOP II	Industrial
	CY14B104L-ZS25XI	51-85087	44-pin TSOP II	
	CY14B104L-BA25XIT	51-85128	48-ball FBGA	Industrial
	CY14B104L-BA25XI	51-85128	48-ball FBGA	
	CY14B104N-BA25XCT	51-85128	48-ball FBGA	Commercial
	CY14B104L-ZSP25XCT	51-85160	54-pin TSOP II	Commercial
	CY14B104L-ZSP25XIT	51-85160	54-pin TSOP II	Industrial
	CY14B104L-ZSP25XI	51-85160	54-pin TSOP II	
	CY14B104N-ZS25XCT	51-85087	44-pin TSOP II	Commercial
	CY14B104N-ZS25XIT	51-85087	44-pin TSOP II	Industrial
	CY14B104N-ZS25XI	51-85087	44-pin TSOP II	
	CY14B104N-BA25XCT	51-85128	48-ball FBGA	Commercial
	CY14B104N-BA25XIT	51-85128	48-ball FBGA	Industrial
	CY14B104N-BA25XI	51-85128	48-ball FBGA	
	CY14B104N-ZSP25XCT	51-85160	54-pin TSOP II	Commercial
	CY14B104N-ZSP25XIT	51-85160	54-pin TSOP II	Industrial
	CY14B104N-ZSP25XI	51-85160	54-pin TSOP II	

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Ordering Information (continued)

Speed (ns)	Ordering Code	Package Diagram	Package Type	Operating Range
45	CY14B104L-ZS45XCT	51-85087	44-pin TSOP II	Commercial
	CY14B104L-ZS45XIT	51-85087	44-pin TSOP II	Industrial
	CY14B104L-ZS45XI	51-85087	44-pin TSOP II	
	CY14B104L-BA45XCT	51-85128	48-ball FBGA	Commercial
	CY14B104L-BA45XIT	51-85128	48-ball FBGA	Industrial
	CY14B104L-BA45XI	51-85128	48-ball FBGA	
	CY14B104L-ZSP45XCT	51-85160	54-pin TSOP II	Commercial
	CY14B104L-ZSP45XIT	51-85160	54-pin TSOP II	Industrial
	CY14B104L-ZSP45XI	51-85160	54-pin TSOP II	
	CY14B104N-ZS45XCT	51-85087	44-pin TSOP II	Commercial
	CY14B104N-ZS45XIT	51-85087	44-pin TSOP II	Industrial
	CY14B104N-ZS45XI	51-85087	44-pin TSOP II	
	CY14B104N-BA45XCT	51-85128	48-ball FBGA	Commercial
	CY14B104N-BA45XIT	51-85128	48-ball FBGA	Industrial
	CY14B104N-BA45XI	51-85128	48-ball FBGA	
	CY14B104N-ZSP45XCT	51-85160	54-pin TSOP II	Commercial
	CY14B104N-ZSP45XIT	51-85160	54-pin TSOP II	Industrial
	CY14B104N-ZSP45XI	51-85160	54-pin TSOP II	

All parts are Pb-free. The above table contains Preliminary information. Please contact your local Cypress sales representative for availability of these parts.

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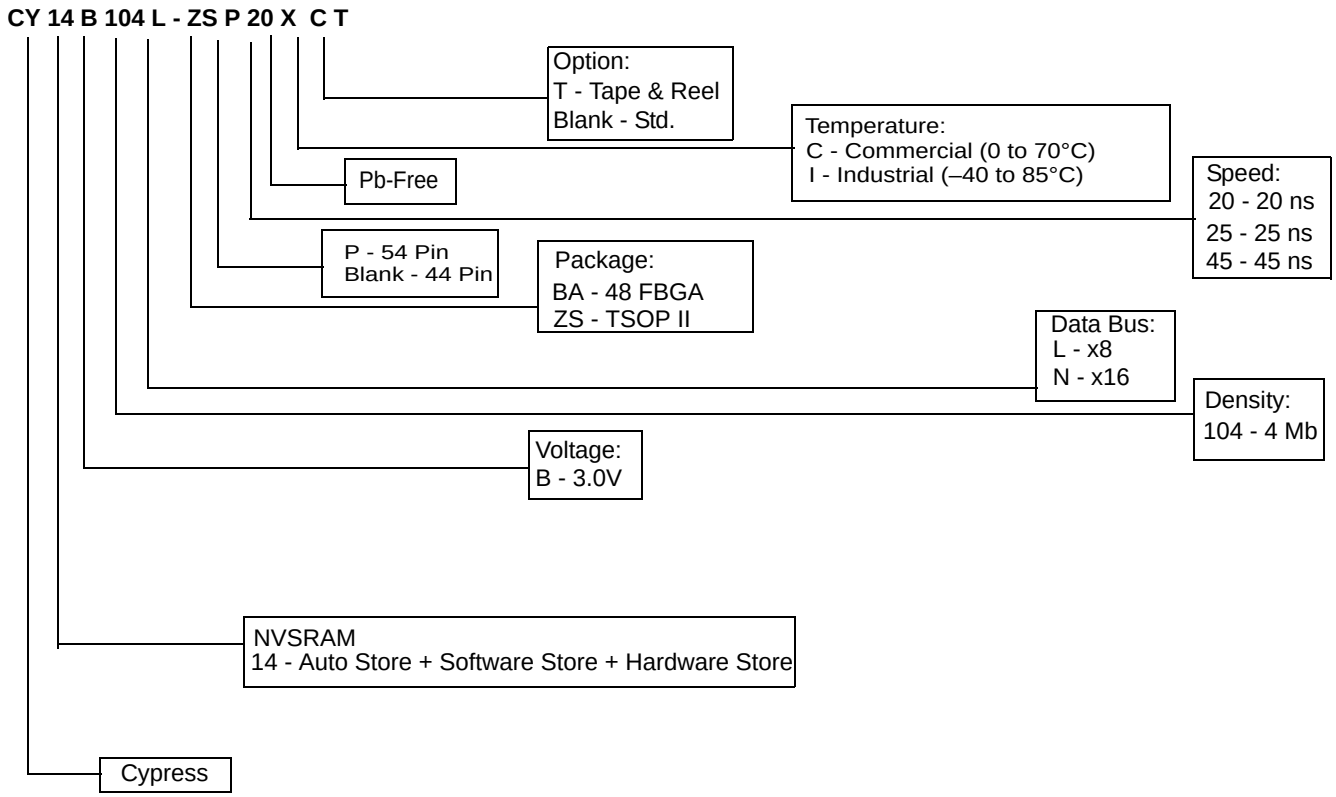
Part Numbering Nomenclature



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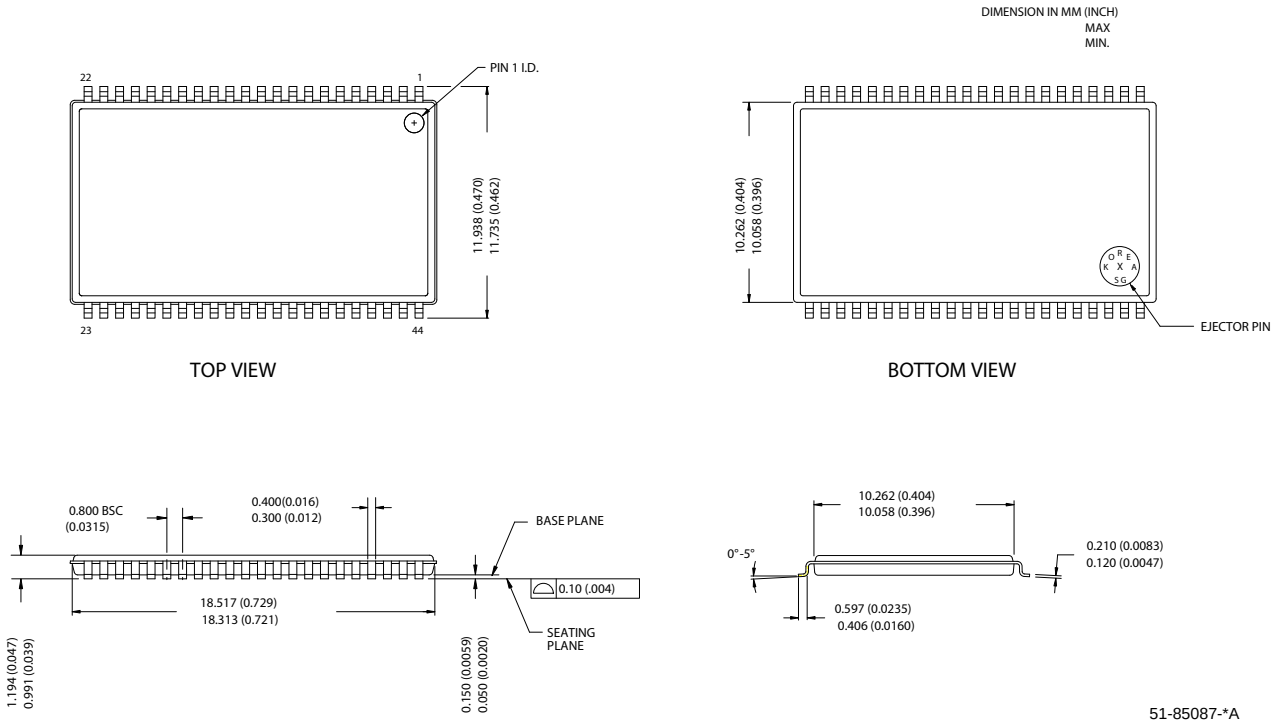
Package Diagrams

Figure 16. 44-Pin TSOP II (51-85087)



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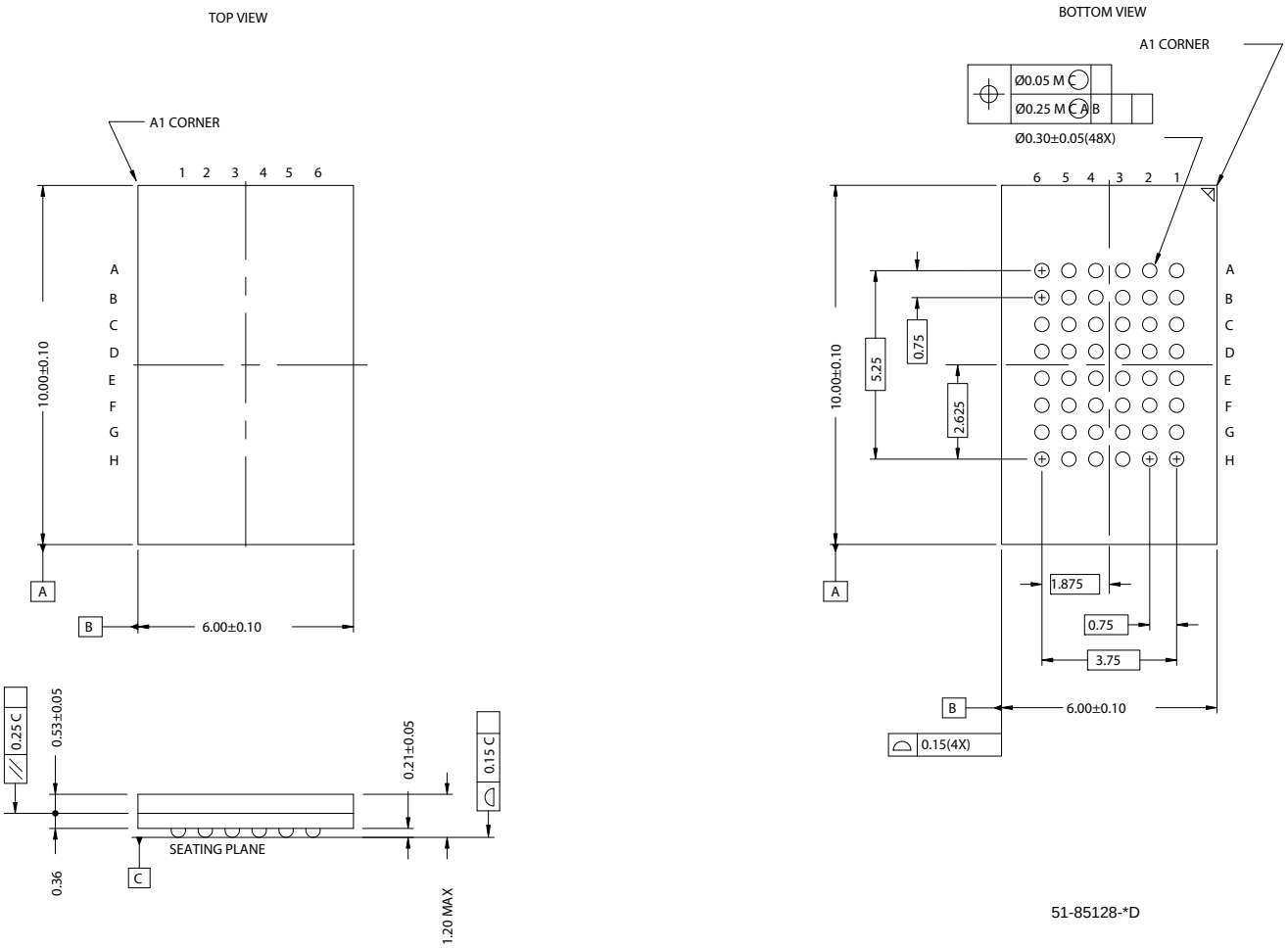
Package Diagrams (continued)

Figure 17. 48-Ball FBGA - 6 mm x 10 mm x 1.2 mm (51-85128)



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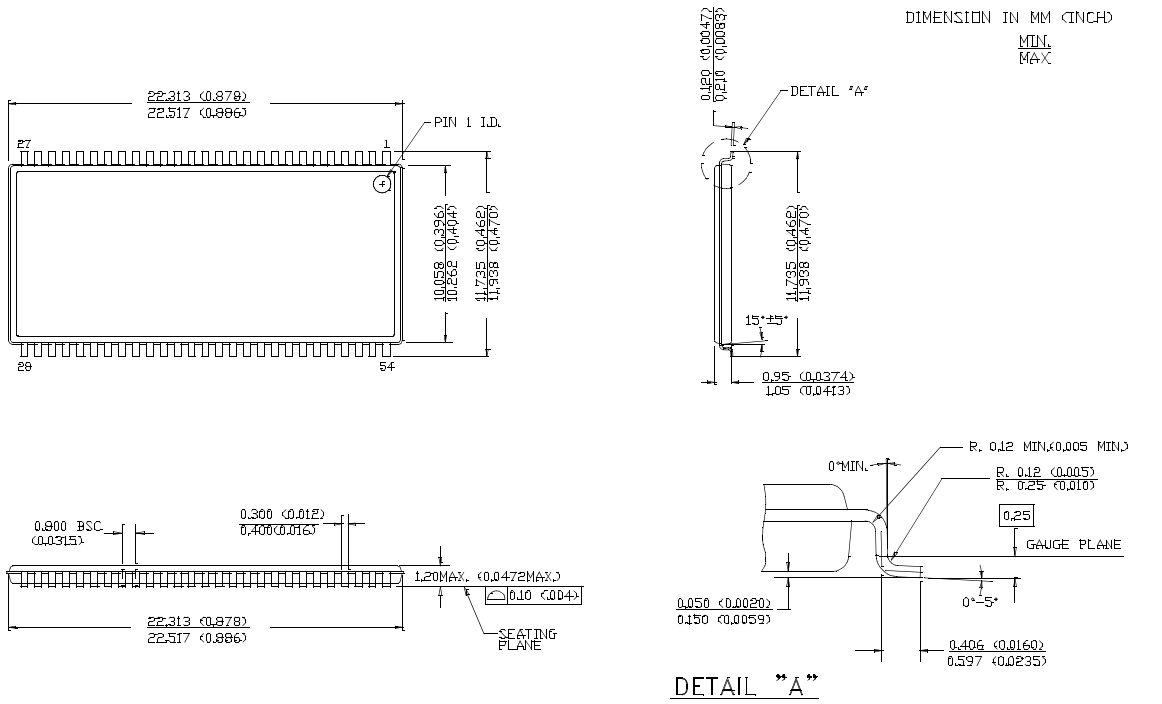
Package Diagrams (continued)

Figure 18. 54-Pin TSOP II (51-85160)



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Document History Page

Document Title: CY14B104L/CY14B104N 4 Mbit (512K x 8/256K x 16) nvSRAM Document Number: 001-07102				
Rev.	**ECN No.**	**Submission Date**	**Orig. of Change**	**Description of Change**
**	431039	See ECN	TUP	New Data Sheet
*A	489096	See ECN	TUP	Removed 48 SSOP Package Added 48 FBGA and 54 TSOPII Packages Updated Part Numbering Nomenclature and Ordering Information Added Soft Sequence Processing Time Waveform
*B	499597	See ECN	PCI	Removed 35 ns speed bin Added 55 ns speed bin. Updated AC table for the same Changed “Unlimited” read/write to “infinite” read/write Features section: Changed typical I_{CC} at 200-ns cycle time to 8 mA Changed STORE cycles from 500K to 200K cycles Shaded Commercial grade in operating range table Modified Icc/Is specs 48 FBGA package nomenclature changed from BW to BV Modified part nomenclature table. Changes reflected in ordering information table
*C	517793	See ECN	TUP	Removed 55ns speed bin Changed pinout for 44TSOPII and 54TSOPII packages Changed I_{SB} to 1mA Changed I_{CC4} to 3mA Changed V_{CAP} min to 35µF Changed V_{IH} max to Vcc + 0.5V Changed t_{STORE} to 15ms Changed t_{PWE} to 10ns Changed t_{SCE} to 15ns Changed t_{SD} to 5ns Changed t_{AW} to 10ns Removed t_{HLBL} Added Timing Parameters for $\overline{BHE}$ and $\overline{BLE}$ - t_{DBE}, t_{LZBE}, t_{HZBE}, t_{BW} Removed min specification for Vswitch Changed t_{GLAX} to 1ns Added t_{DELAY} max of 70us Changed t_{SS} specification from 70us min to 70us max
*D	774001	See ECN	UHA	Changed the data sheet from Advance information to Preliminary 48 FBGA package code changed from BV to BA Removed 48 FBGA package in X8 configuration in ordering information. Changed t_{DBE} to 10ns in 15ns part Changed t_{HZBE} in 15ns part to 7ns and in 25ns part to10ns Changed t_{BW} in 15ns part to 15ns and in 25ns part to 20ns Changed t_{GLAX} to t_{GHAX} Changed the value of I_{CC3} to 25mA Changed the value of t_{AW} in 15ns part to15ns Changed A_{18} and A_{19} Pins in FBGA Pin Configuration to NC
*E	914220	See ECN	UHA	Included all the information for 45 ns part in this data sheet

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Rev.	**ECN No.**	**Submission Date**	**Orig. of Change**	**Description of Change**
*F	1889928	See ECN	vsutmp8/AE-SA	Added Footnotes 1, 2 and 3. Updated logic block diagram Added 48-FBGA (X8) Pin Diagram Changed 8Mb Address expansion Pin from Pin 43 to Pin 42 for 44-TSOP II (x8). Updated pin definitions table. Corrected typo in V_{IL} min spec Changed the value of I_{CC3} from 25mA to 13mA Changed I_{SB} value from 1mA to 2mA Rearranging of Footnotes. Updated ordering information table
*G	2267286	See ECN	GVCH/PYRS	Added $\overline{BHE}$ and $\overline{BLE}$ Information in Pin Definitions Table Updated Figure 4 (Autostore mode) Updated footnote 6 Changed I_{CC2} & I_{CC4} from 3 mA to 6 mA Changed I_{CC3} from 13 mA to 15 mA Changed Vcap from 35uF min and 57uF max value to 54uF min and 82uF max value Changed I_{SB} from 2 mA to 3 mA Added input leakage current (I_{IX}) for $\overline{HSB}$ in DC Electrical Characteristics table Corrected typo in t_{DBE} value from 22 ns to 20 ns for 45 ns part Corrected typo in t_{HZBE} value from 22 ns to 15 ns for 45 ns part Corrected typo in t_{AW} value from 15 ns to 10ns for 15 ns part Changed t_{RECALL} from 100 to 200 us Added footnotes 9 and 25; Reframed footnote 14 and 21 Added footnote 14 to figure 7 (SRAM WRITE Cycle #1)
*H	2483627	See ECN	GVCH/PYRS	Removed 8 mA typical I_{CC} at 200 ns cycle time in Feature section Referenced footnote 8 to I_{CC3} in DC Characteristics table Changed I_{CC3} from 15 mA to 35 mA Changed Vcap minimum value from 54 uF to 61 uF Changed t_{AVAV} to t_{RC} Figure 11:Changed t_{SA} to t_{AS} and $t_{SCE\ to}$ t_{CW}
*I	2519319	06/20/08	GVCH/PYRS	Added 20 ns access speed in “Features” Added I_{CC1} for t_{RC}=20 ns for both industrial and Commercial temperature Grade updated Thermal resistance table values for 48-FBGA, 44-TSOP II and 54-TSOP II Packages Added AC Switching Characteristics specs for 20 ns access speed Added software controlled STORE/RECALL cycle specs for 20 ns access speed Updated ordering information and part numbering nomenclature

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Document Title: CY14B104L/CY14B104N 4 Mbit (512K x 8/256K x 16) nvSRAM Document Number: 001-07102				
Rev.	**ECN No.**	**Submission Date**	**Orig. of Change**	**Description of Change**
*J	2600941	11/04/08	GVCH/PYRS	Removed 15 ns access speed Updated Logic block diagram Updated footnote 1 Added footnote 2 and 5 Pin definition: Updated $\overline{WE}$, $\overline{HSB}$ and NC pin description Page 4:Updated SRAM READ, SRAM WRITE, Autostore operation description Page 4:Updated Hardware store operation and Hardware RECALL (Power-up) description Footnote 1 referenced for Mode selection Table Page 6:updated Data protection description Maximum Ratings: Added Max. Accumulated storage time Changed I_{CC2} from 6mA to 10mA Changed I_{CC4} from 6mA to 5mA Changed I_{SB} from 3mA to 5mA Updated I_{CC1}, I_{CC3} , $I_{SB}$and I_{OZ} Test conditions Changed V_{CAP} max value from 82uf to 180uF Updated footnote 10 and 11 Added footnote 12 Added Data retention and Endurance Table Updated Input Rise and Fall time in AC test Conditions Referenced footnote 15 to t_{OHA} parameter Updated All switching waveforms Added Figure 10 (SRAM WRITE CYCLE:$\overline{BHE}$ and $\overline{BLE}$ controlled) Changed t_{DELAY} to 20ns, 25ns, 25ns for 15ns, 20ns, 45ns part respectively Changed t_{STORE} from 15ms to 8ms Added V_{HDIS}, t_{HHHD} and t_{LZHSB} parameters Updated footnote 21 Added footnote 24 Software controlled STORE/RECALL cycle table: Changed t_{AS} to t_{SA} Changed t_{GHAX} to t_{HA} Added t_{DHSB} parameter Changed t_{HLHX} to t_{PHSB} Updated t_{SS} from 70us to 100us Added Truth table for SRAM operations Updated ordering information and part numbering nomenclature
*K	2612931	11/26/08	AESA	Removed Preliminary form header.
*L	2625431	12/19/08	GVCH/DSG	Changed t_{DELAY} to 1us (min) and 70us (max) for all three access time Page 4: Removed the text relating to write requested after $\overline{HSB}$ goes LOW are inhibited. Page 5: modified software store description to indicate no further read/writes permitted for t_{SS} duration after sixth read cycle. Added parameter t_{PURHH} to AutoStore power-Up recall table Updated Figures 11, 12 and 13. Added t_{HLBL} parameter Removed t_{DHSB} parameter Updated Figure 14;Hardware store cycle Changed Simtek trademarks to Cypress

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