International
IOR Rectifier

February 17th, 2010

Automotive Grade
AUIRS2112S

HIGH- AND LOW-SIDE DRIVER

Features

- Drives IGBT/MOSFET power devices
- Floating channel designed for bootstrap operation
- Fully operational to +600 V
- Tolerant to negative transient voltage – dV/dt immune
- Gate drive supply range from 10 V to 20 V
- Undervoltage lockout for both channels
- 3.3 V input logic compatible
- Separate logic supply range from 3.3 V to 20 V
- Logic and power ground +/- 5 V offset
- CMOS Schmitt-triggered inputs with pull-down
- shutdown logic
- Matched propagation delay for both channels
- Output in phase with inputs
- Leadfree, RoHS compliant
- Automotive qualified*

Typical Applications

- Piezo, Common Rail Injection
- MOSFET and IGBT gate drivers

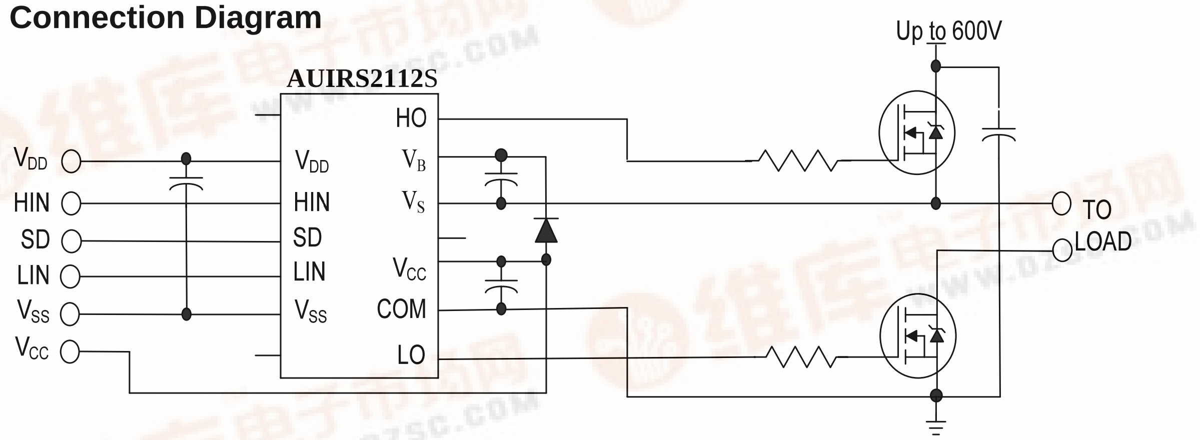
Product Summary

Topology	High and Low Side Driver
V_{OFFSET}	≤ 600 V
V_{OUT}	10 V – 20 V
I_{o+} & I_{o-} (typical)	290 mA & 600 mA
t_{ON} & t_{OFF} (typical)	140 ns & 140 ns

Package Options

16-Lead SOIC Wide Body
AUIRS2112S

Typical Connection Diagram



(Refer to Lead Assignments for correct pin configuration). This/These diagram(s) show electrical connections only. Please refer to our Application Notes and Design Tips for proper circuit board layout.

* Qualification standards can be found on IR's web site www.irf.com

Description

The AUIRS2112S is a high voltage, high speed power MOSFET and IGBT driver with independent high- and low-side referenced output channels. Proprietary HVIC and latch immune CMOS technologies enable ruggedized monolithic construction. The logic input is compatible with standard CMOS or LSTTL output, down to 3.3 V logic. The output drivers feature a high pulse current buffer stage designed for minimum driver cross-conduction. Propagation delays are matched to simplify use in high frequency applications. The floating channel can be used to drive an N-channel power MOSFET or IGBT in the high side configuration which operates up to 600 V.

Qualification Information†

Qualification Level		Automotive (per AEC-Q100††)	
		Comments: This family of ICs has passed an Automotive qualification. IR's Industrial and Consumer qualification level is granted by extension of the higher Automotive level.	
Moisture Sensitivity Level		SOIC16W	MSL3††† 260°C (per IPC/JEDEC J-STD-020)
ESD	Machine Model	Class M2 (Pass +/-150 V) (per AEC-Q100-003)	
	Human Body Model	Class H1B (Pass +/-1000V) (per AEC-Q100-002)	
	Charged Device Model	Class C4 (Pass +/-1000V) (per AEC-Q100-011)	
IC Latch-Up Test		Class II, Level B†††† (per AEC-Q100-004)	
RoHS Compliant		Yes	

† Qualification standards can be found at International Rectifier's web site http://www.irf.com/

†† Exceptions to AEC-Q100 requirements are noted in the qualification report.

††† Higher MSL ratings may be available for the specific package types listed here. Please contact your International Rectifier sales representative for further information.

†††† Input pins can withstand up to 40 mA.

Absolute Maximum Ratings

Absolute Maximum Ratings indicate sustained limits beyond which damage to the device may occur. All voltage parameters are absolute voltages referenced to COM lead. Stresses beyond those listed under " Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only; and functional operation of the device at these or any other condition beyond those indicated in the "Recommended Operating Conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability. The thermal resistance and power dissipation ratings are measured under board mounted and still air conditions. Ambient temperature (T_A) is 25°C, unless otherwise specified.

Symbol	Definition	Min.	Max.	Units
V_B	High-side floating supply voltage	-0.3	625	V
V_S	High-side floating supply offset voltage	V_B - 25	V_B + 0.3	
V_{HO}	High-side floating output voltage	V_S - 0.3	V_B + 0.3	
V_{CC}	Low-side fixed supply voltage	-0.3	25	
V_{LO}	Low-side output voltage	-0.3	V_{CC} + 0.3	
V_{DD}	Logic supply voltage	-0.3	V_{SS} + 25	
V_{SS}	Logic supply offset voltage	V_{CC} - 25	V_{CC} + 0.3	
V_{IN}	Logic input voltage (HIN, LIN & SD)	V_{SS} -0.3	V_{DD} + 0.3	
dV_S/dt	Allowable offset supply voltage transient (Fig. 2)	—	50	V/ns
P_D	Package power dissipation @ TA ≤ 25°C	—	1.25	W
Rth_{JA}	Thermal resistance, junction to ambient	—	100	°C/W
T_J	Junction temperature	—	150	°C
T_S	Storage temperature	-55	150	
T_L	Lead temperature (soldering, 10 seconds)	—	300	
Rth_{JC}	Thermal resistance, junction to case	---	12.72	°C/W

Recommended Operation Conditions

The input/output logic timing diagram is shown in Figure 1. For proper operation the device should be used within the recommended conditions. The V_S and V_{SS} offset rating are tested with all supplies biased at 15 V differential.

Symbol	Definition	Min.	Max.	Units
V_B	High-side floating supply absolute voltage	V_S +10	V_S +20	V
V_S	High-side floating supply offset voltage	†	600	
V_{HO}	High-side floating output voltage	V_S	V_B	
V_{CC}	Low-side fixed supply voltage	10	20	
V_{LO}	Low-side output voltage	0	V_{CC}	
V_{DD}	Logic supply voltage	V_{SS} + 3	V_{SS} + 20	
V_{SS}	Logic ground offset voltage	-5 (††)	5	
V_{IN}	Logic input voltage (HIN, LIN & SD)	V_{SS}	V_{DD}	
T_A	Ambient temperature	-40	125	°C

† Logic operational for V_S of -5 V to +600 V. Logic state held for V_S of -5 V to – V_{BS} (Static). Please refer to 'Tolerability to Negative VS Transients' section.

†† When V_{DD} < 5 V, the minimum V_{SS} offset is limited to $–V_{DD}$.

Dynamic Electrical Characteristics

Unless otherwise noted, these specifications apply for an operating junction temperature range of -40°C ≤ Tj ≤ 125°C with bias conditions of V_{BIAS} (V_{CC}, $V_{BS,}$ V_{DD}) = 15 V, C_L = 1000 pF. The dynamic electrical characteristics are measured using the test circuit shown in Fig. 3.

Symbol	Definition	Min	Typ	Max	Units	Test Conditions
t_{on}	Turn-on propagation delay	—	140	230	ns	V_S = 0 V
t_{off}	Turn-off propagation delay	—	140	210		V_S = 600 V
t_{sd}	Shutdown propagation delay	—	140	220		
t_r	Turn-on rise time	—	60	140		
t_f	Turn-off fall time	—	30	60		
MT	Delay matching , HS & LS turn-on/off	—	—	50		

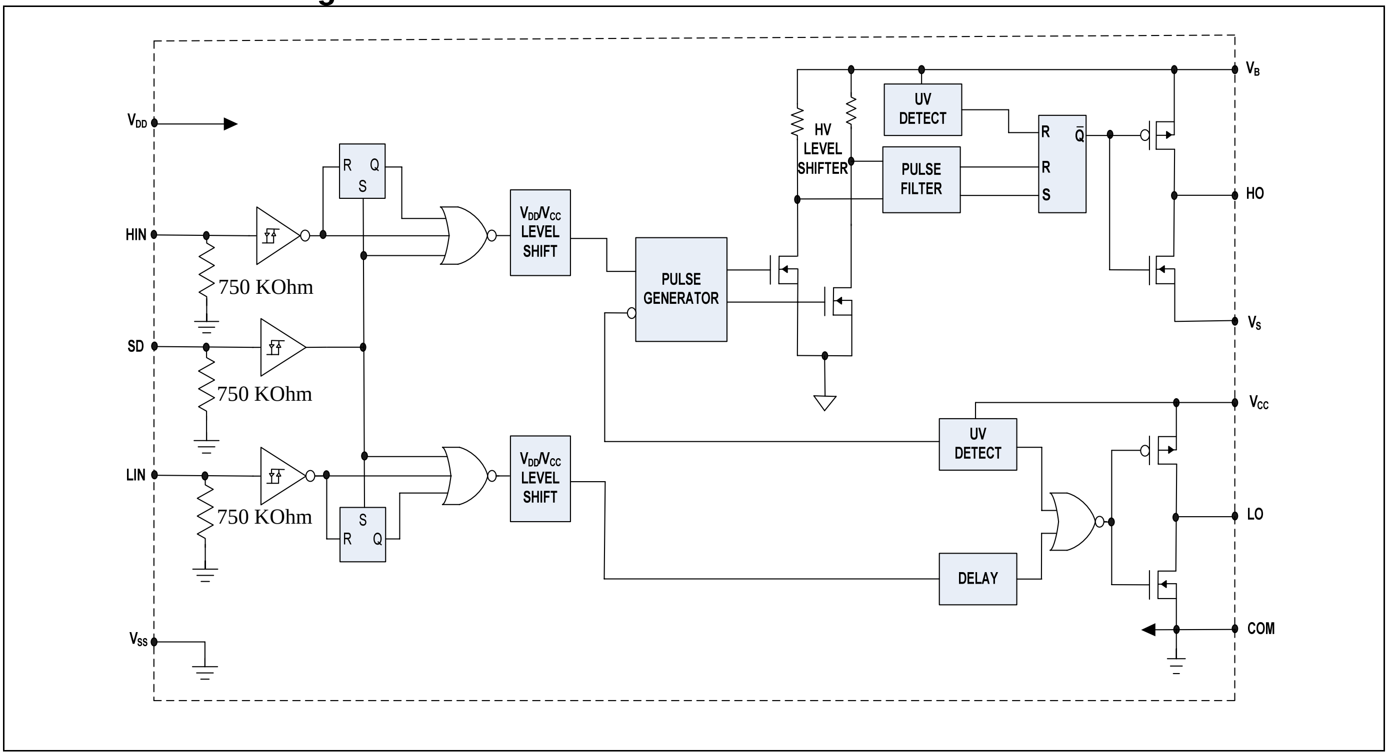
Static Electrical Characteristics

Unless otherwise noted, these specifications apply for an operating junction temperature range of -40°C ≤ Tj ≤ 125°C with bias conditions of V_{BIAS} (V_{CC}, $V_{BS,}$ V_{DD}) = 15 V, C_L = 1000 pF, V_{SS} = COM. The $V_{IL,}$ V_{IH} and I_{IN} parameters are referenced to V_{SS} and are applicable to all three logic input leads: HIN, LIN and SD. The $V_{O,}$ and I_O parameters are referenced to COM and are applicable to the respective output leads: HO or LO.

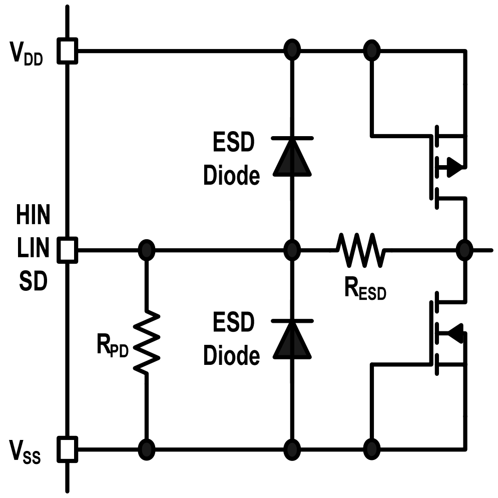
Symbol	Definition	Min	Typ	Max	Units	Test Conditions
V_{IH}	Logic "1" input voltage	9.5	—	—	V	
V_{IL}	Logic "0" input voltage	—	—	6.0		
V_{OH}	High level output voltage, V_{BIAS} - V_O	—	0.05	0.2		I_O = 2 mA
V_{OL}	Low level output voltage, V_O	—	0.02	0.1		
I_{LK}	Offset supply leakage current	—	—	50	µA	V_B = V_S = 600 V
I_{QBS}	Quiescent V_{BS} supply current	—	50	100		V_{IN} = 0 V or V_{DD}
I_{QCC}	Quiescent V_{CC} supply current	—	80	160		
I_{QDD}	Quiescent V_{DD} supply current	—	2.0	10		
I_{IN+}	Logic "1" input bias current	—	15	30		V_{IN} = V_{DD}
I_{IN-}	Logic "0" input bias current	—	—	1.0		V_{IN} = 0 V
V_{BSUV+}	V_{BS} supply undervoltage positive going threshold	7.4	8.5	9.6	V	
V_{BSUV-}	V_{BS} supply undervoltage negative going threshold	7.0	8.1	9.2		
V_{CCUV+}	V_{CC} supply undervoltage positive going threshold	7.6	8.6	9.6		
V_{CCUV-}	V_{CC} supply undervoltage negative going threshold	7.2	8.2	9.2		
I_{O+} (†)	Output high short circuit pulsed current	200	290	—	mA	V_O = 0 V, V_{IN} = V_{DD} PW ≤ 10 us, T_J = 25°C
I_{O-} (†)	Output low short circuit pulsed current	420	600	—		V_O = 15 V, V_{IN} = 0 V PW ≤ 10 us, T_J = 25°C

(†) Guaranteed by design

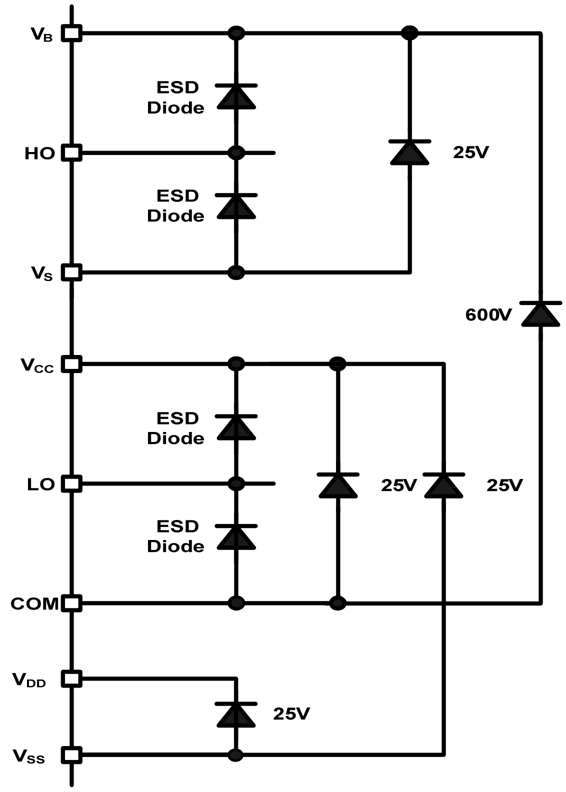
Functional Block Diagram: AUIRS2112S



Input/Output Pin Equivalent Circuit Diagrams



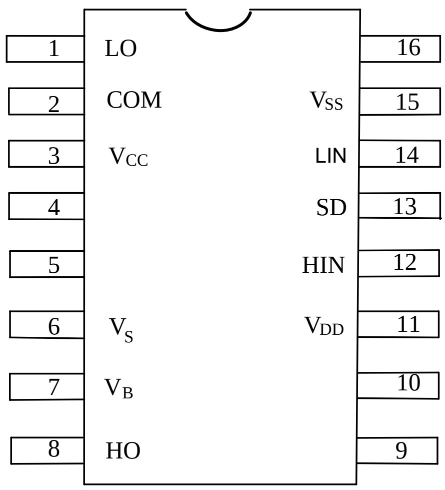
R_{PD} = 950KΩ, R_{ESD} = 250Ω



Lead Definitions

Symbol	Description
V_{DD}	Logic supply
HIN	Logic input for high-side gate driver output (HO), in phase
SD	Logic input for shutdown
LIN	Logic input for low-side gate driver output (LO), in phase
V_{SS}	Logic ground
V_B	High-side floating supply
HO	High-side gate drive output
V_S	High-side floating supply return
V_{CC}	Low-side supply
LO	Low-side gate drive output
COM	Low-side return

Lead Assignments



16 Lead SOIC Wide Body

AUIRS2112S

Application Information and Additional Details

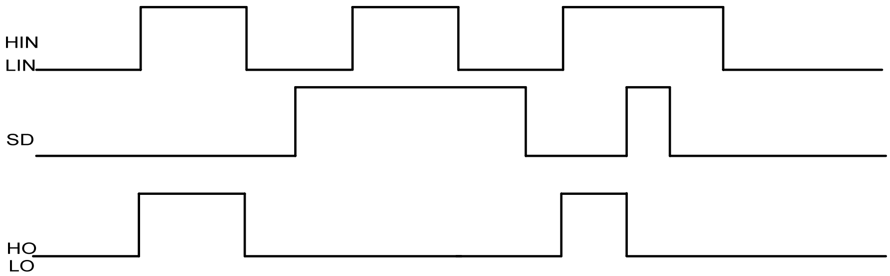


Figure 1: Input/Output Timing Diagram

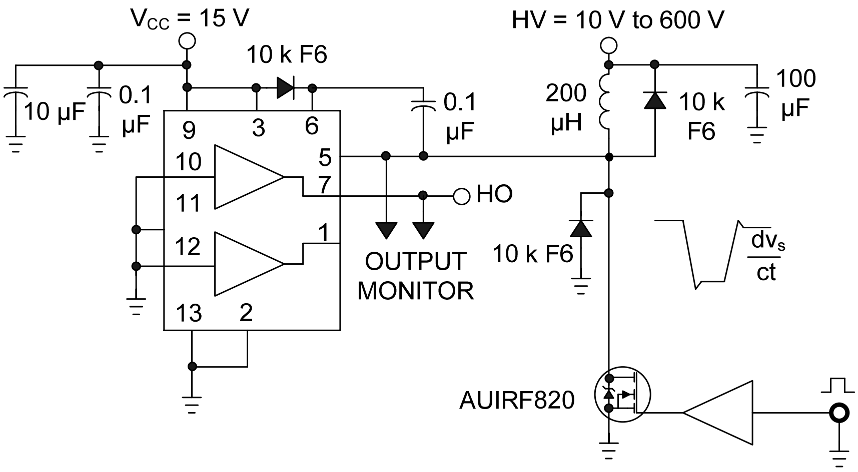


Figure 2: Floating Supply Voltage Transient Test Circuit

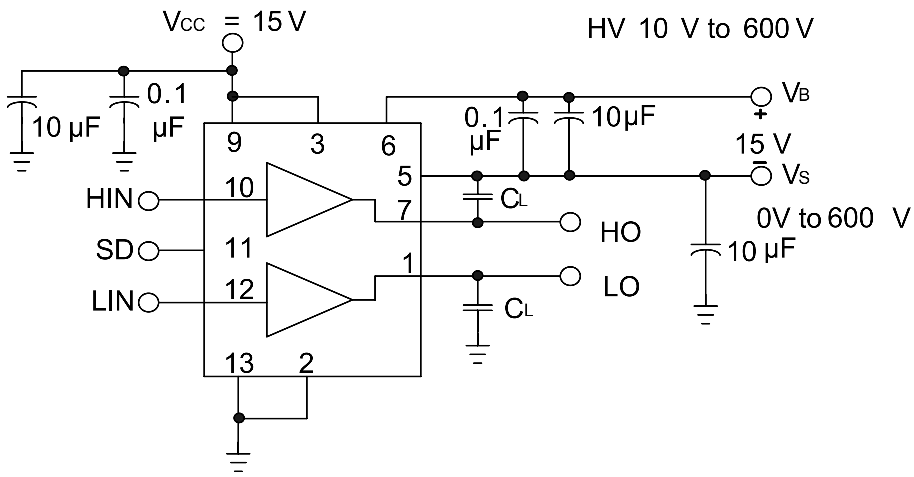


Figure 3: Switching Time Test Circuit

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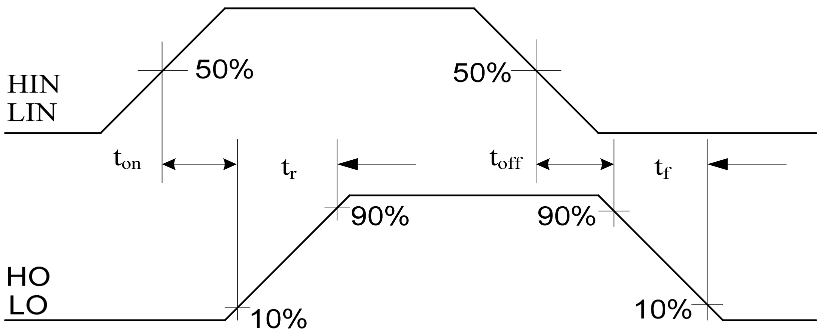

Figure 4: Switching Time Waveform Definitions

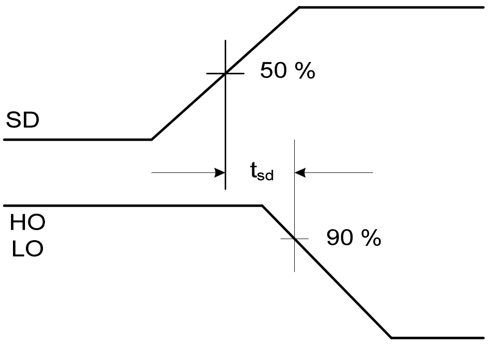

Figure 5: Shutdown Waveform

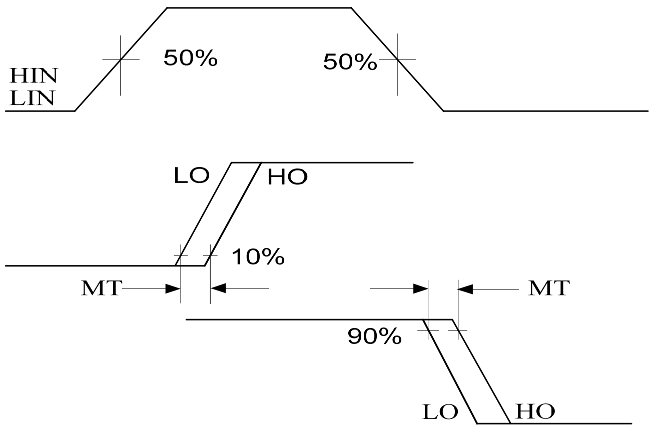

Figure 6: Delay Matching Waveform Definitions

Tolerability to Negative VS Transients

The AUIRS2112S has been seen to withstand negative Vs transient conditions on the order of -25V for a period of 150 ns (V_{BIAS} (V_{CC}, V_{BS}) = 15V and T_A = 25°C).
An illustration of the AUIRS2112S performance can be seen in Figure 7, where points above the line represent pulses that the circuit can withstand.
Even though the AUIRS2112S has been shown able to handle these negative Vs transient conditions, it is highly recommended that the circuit designer always limit the negative Vs transients as much as possible by careful PCB layout and component use.

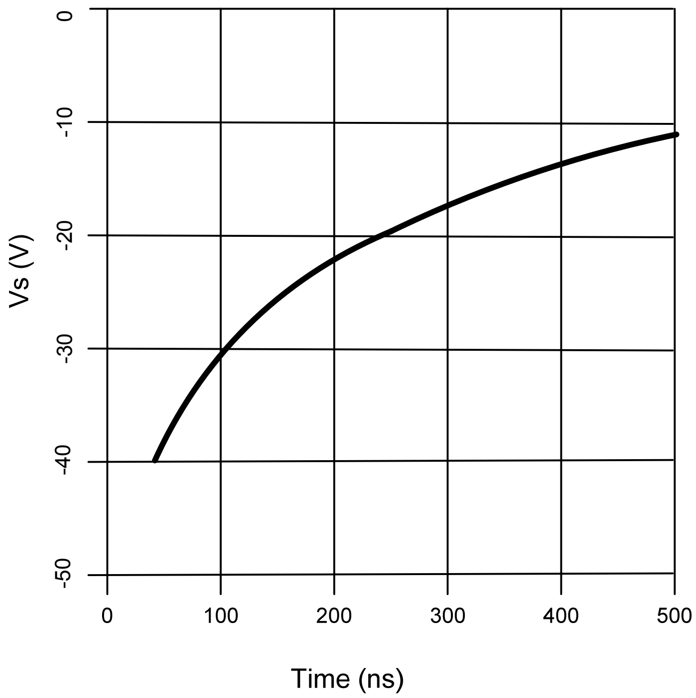

Figure 7: -Vs Transient results

Parameter Trends vs. Temperature and vs. Supply Voltage

Figures illustrated in this chapter provide information on the experimental performance of the AUIRS2112S HVIC. The line plotted in each figure is generated from actual lab data. A large number of individual samples were tested at three temperatures (-40 ºC, 25 ºC, and 125 ºC) with supply voltage of 15V in order to generate the experimental curve. The line consists of three data points (one data point at each of the tested temperatures) that have been connected together to illustrate the understood trend. The individual data points on the Typ. curve were determined by calculating the averaged experimental value of the parameter (for a given temperature).

An individual sample was used to generate curves of parameter trends vs. supply voltage; tests were done at room temperature.

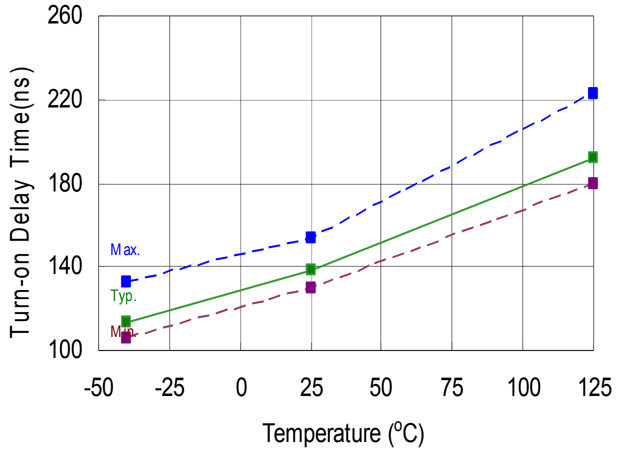

Figure 8A. Turn-on Propagation Delay Time vs. Temperature

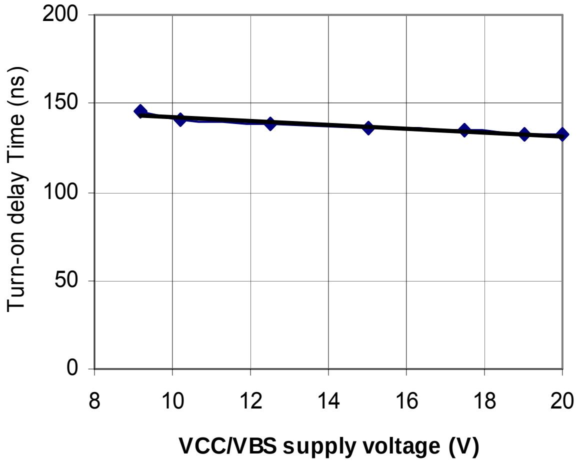

Figure 8B. Turn-on Propagation Delay Time vs. V_{CC}/V_{BS} Supply Voltage

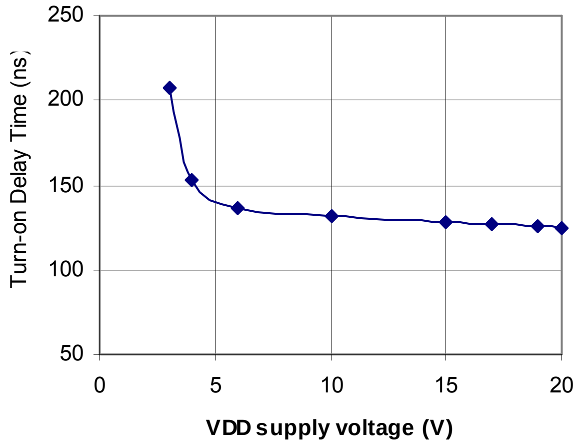

Figure 8C. Turn-on Propagation Delay Time vs. V_{DD} Supply Voltage

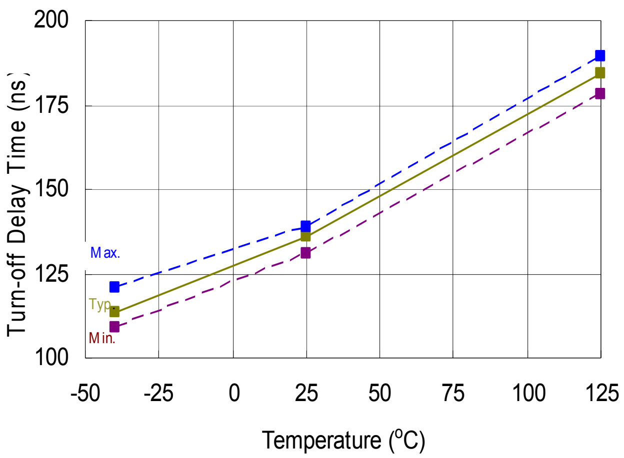

Figure 9A. Turn-off Propagation Delay Time vs. Temperature

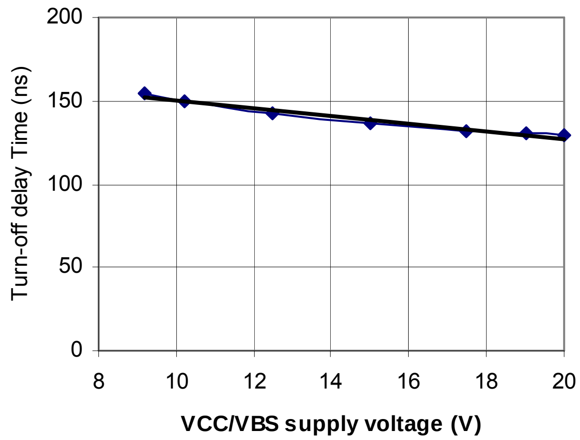

Figure 9B. Turn-off Propagation Delay Time vs. V_{CC}/V_{BS} Supply Voltage

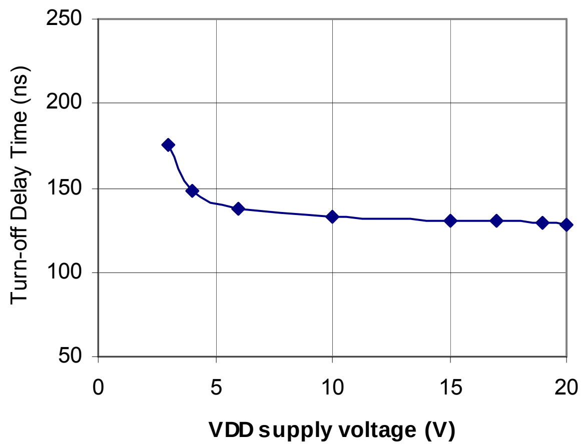

Figure 9C. Turn-off Propagation Delay Time vs. V_{DD} Supply Voltage

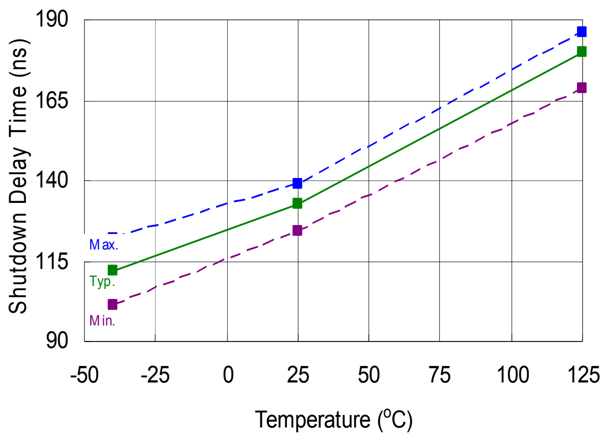

Figure 10A. Shutdown Delay Time vs. Temperature

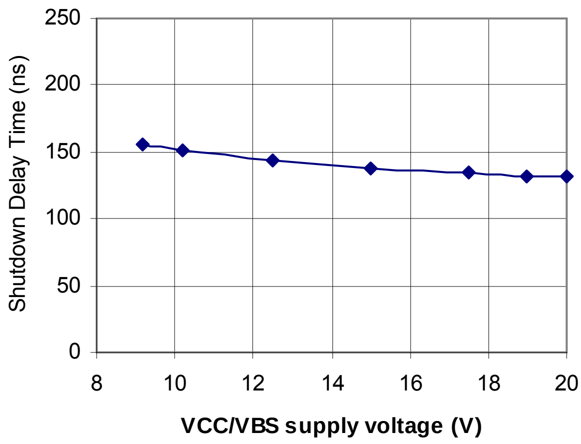

Figure 10B. Shutdown Delay Time vs. V_{CC}/V_{BS} Supply Voltage

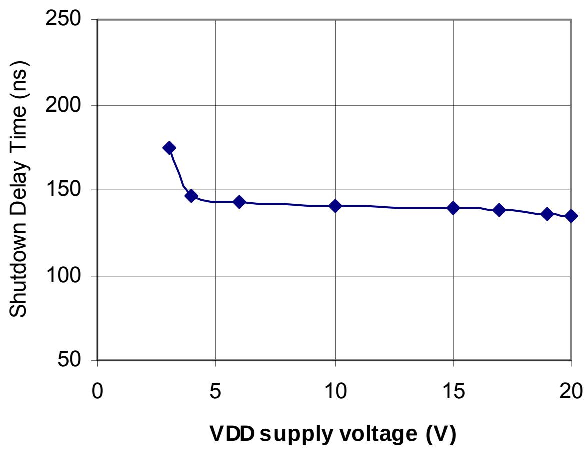

Figure 10C. Shutdown Delay Time vs. V_{DD} Supply Voltage

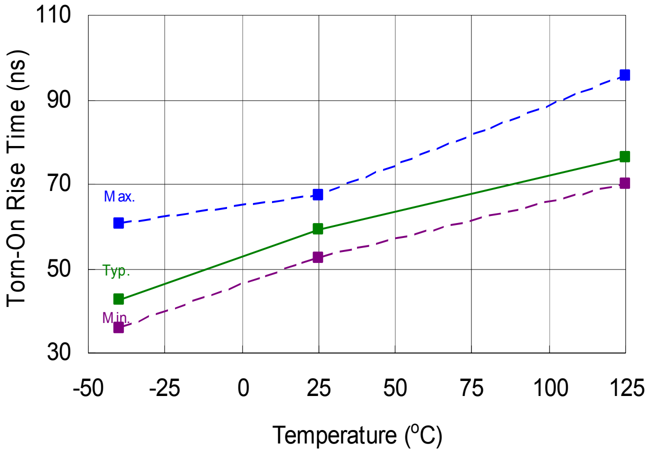

Figure 11A. Turn-on Rise Time vs. Temperature

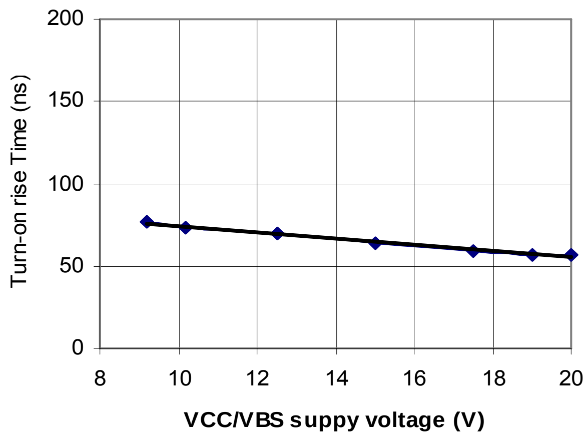

Figure 11B. Turn-on Rise Time vs. Voltage

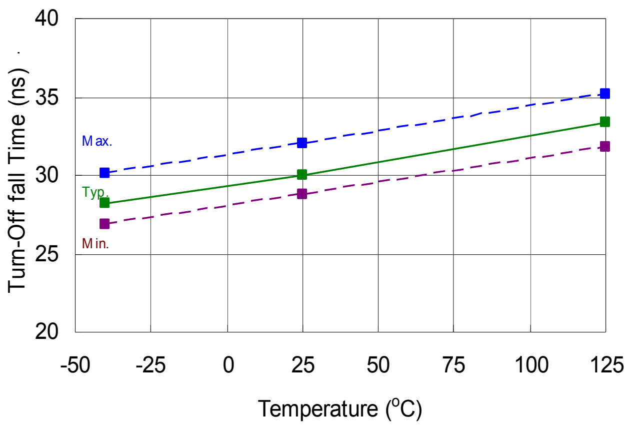

Figure 12A. Turn-off Fall Time vs. Temperature

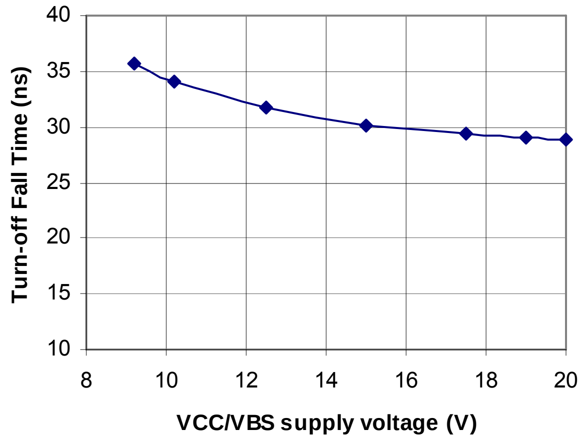

Figure 12B. Turn-off Fall Time vs. Voltage

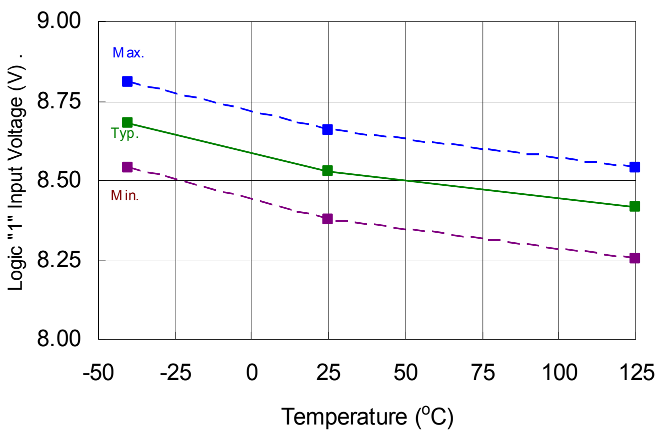

Figure 13A. Logic “1” Input Threshold vs. Temperature

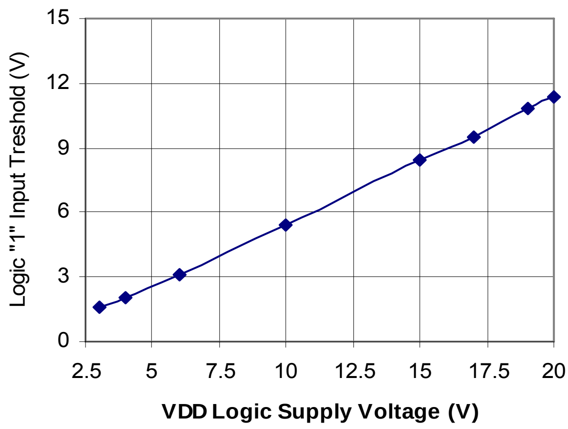

Figure 13B. Logic “1” Input Threshold vs. Voltage

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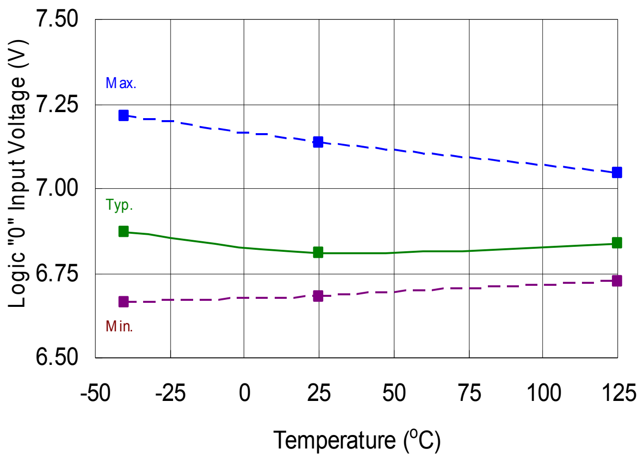


Figure 14A. Logic "0" Input Threshold vs. Temperature

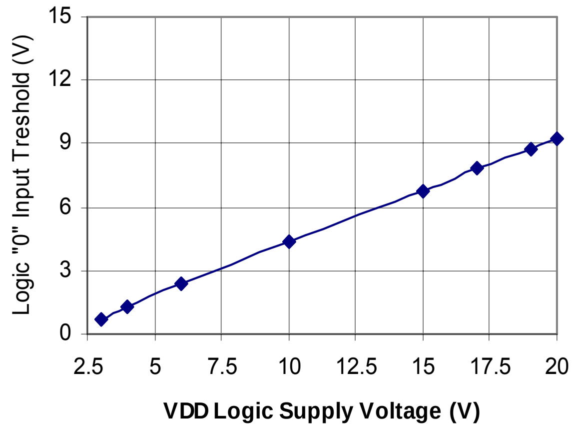


Figure 14B. Logic "0" Input Threshold vs. Voltage

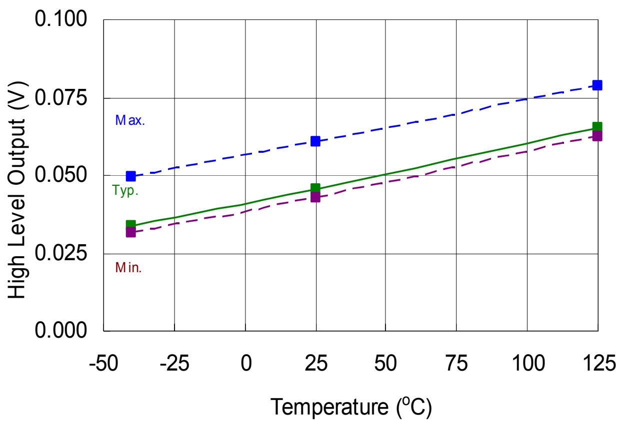


Figure 15. High Level Output Voltage vs. Temperature (I_O = 2 mA)

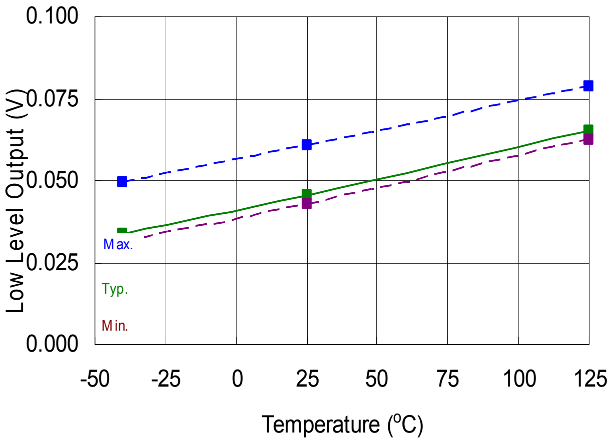


Figure 16. Low Level Output Voltage vs. Temperature (I_O = 2 mA)

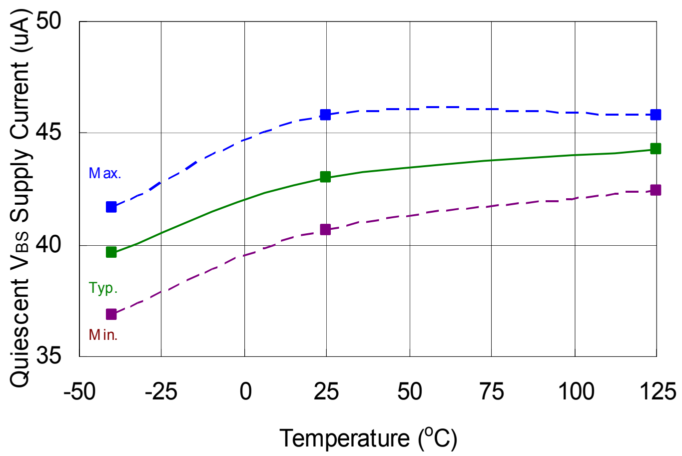


Figure 17A. V_{BS} Supply Current vs. Temperature

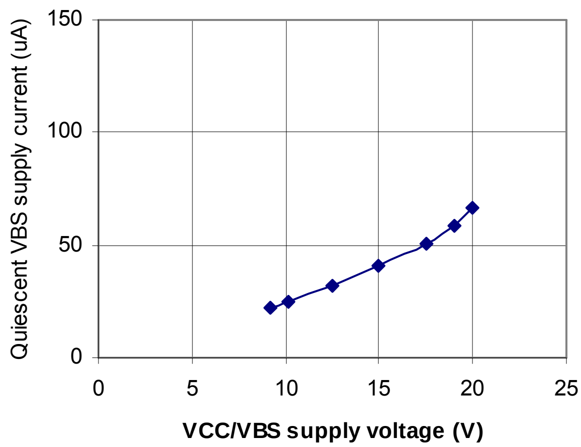


Figure 17B. V_{BS} Supply Current vs. Voltage

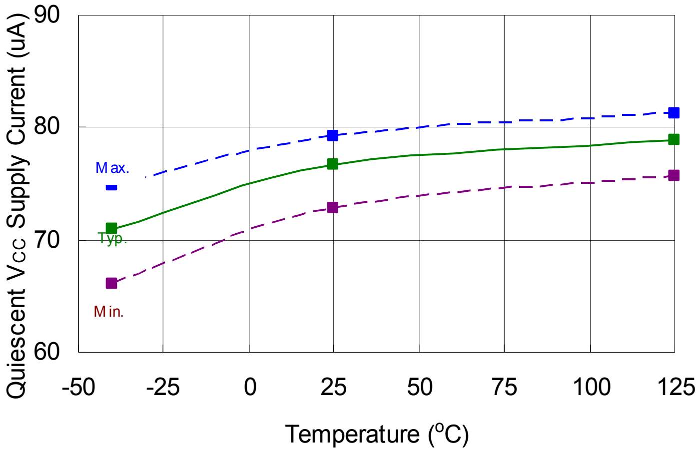


Figure 18A. V_{CC} Supply Current vs. Temperature

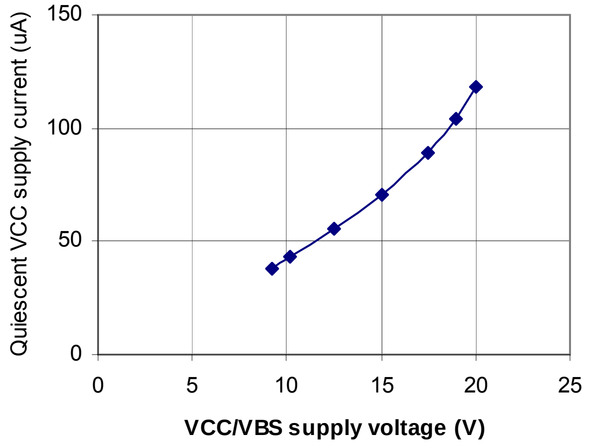


Figure 18B. V_{CC} Supply Current vs. Voltage

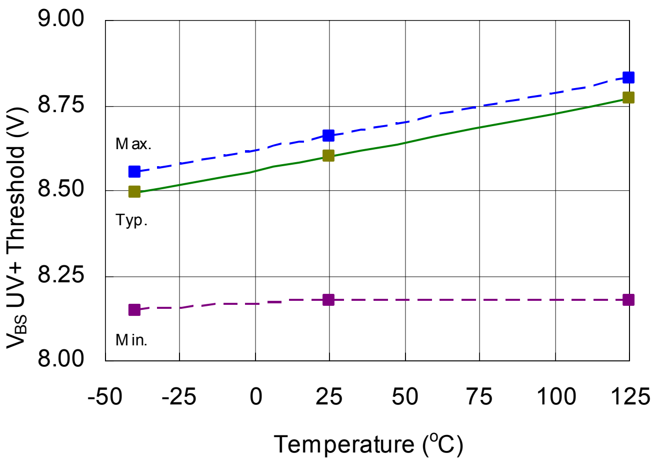


Figure 19. V_{BS} Undervoltage (+) vs. Temperature

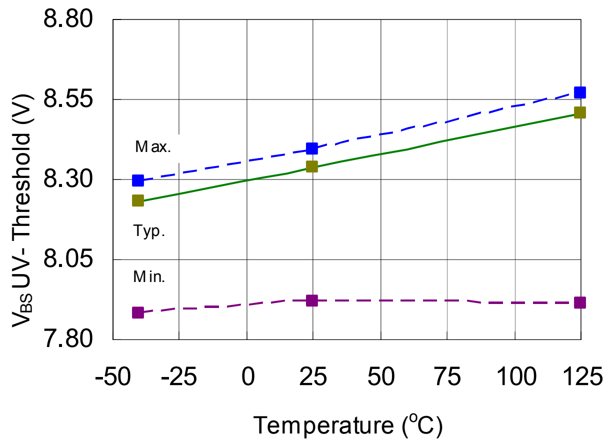


Figure 20. V_{BS} Undervoltage (-) vs. Temperature

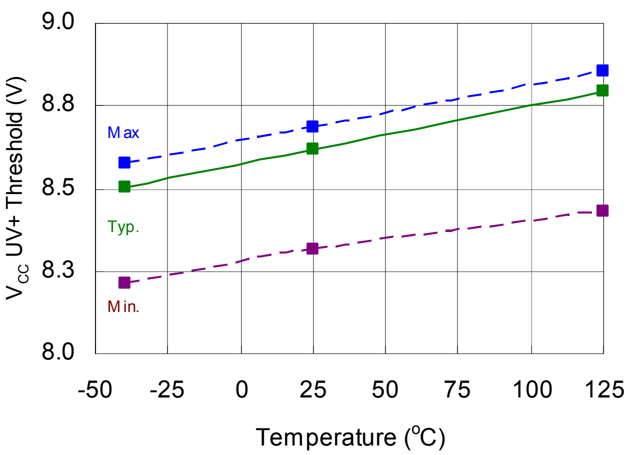


Figure 21. V_{CC} Undervoltage (+) vs. Temperature

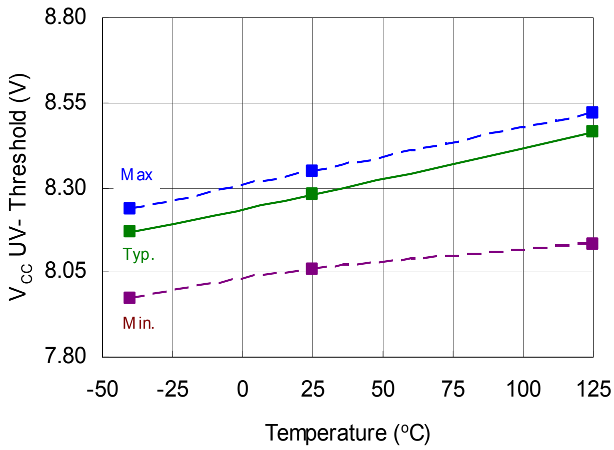


Figure 22. V_{CC} Undervoltage (-) vs. Temperature

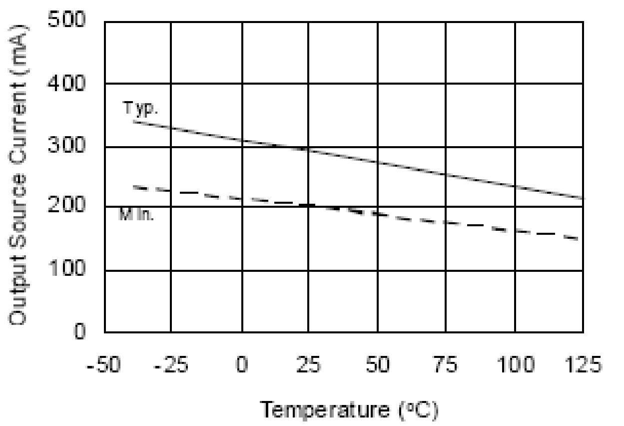


Figure 23A. Output Source Current vs. Temperature

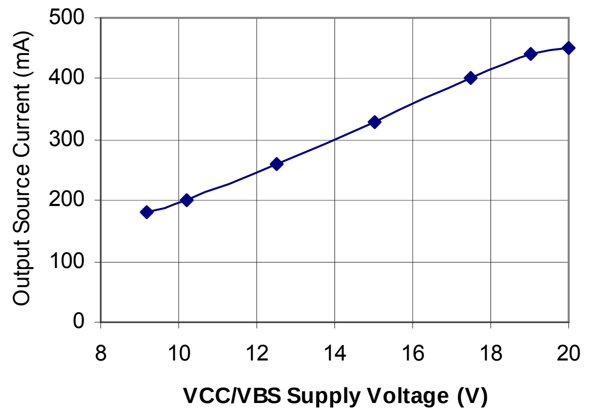


Figure 23B. Output Source Current vs. Supply Voltage

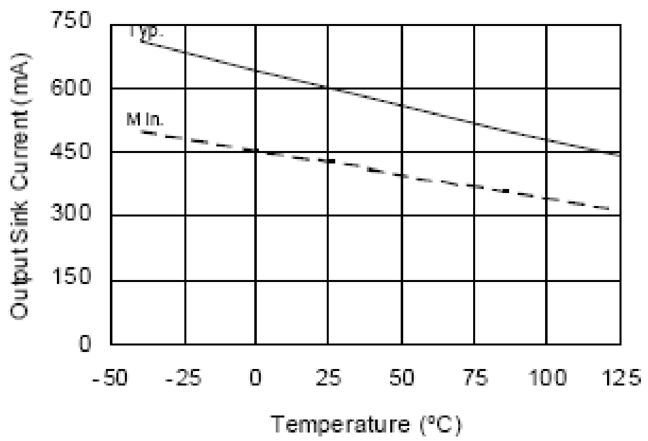


Figure 24A. Output Sink Current vs. Temperature

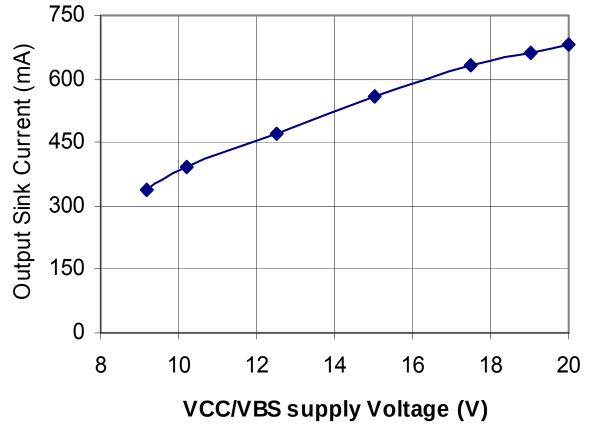


Figure 24B. Output Sink Current vs. Supply Voltage

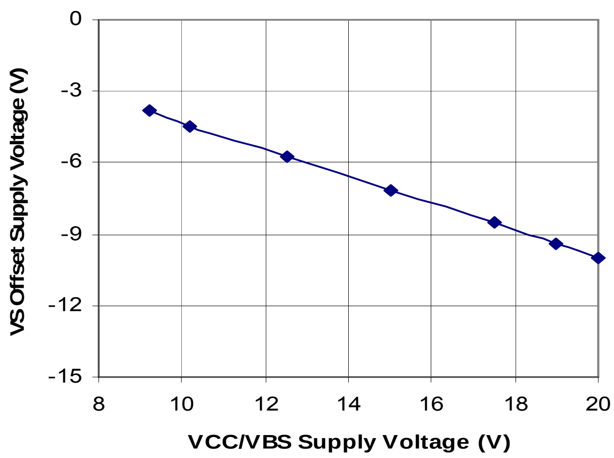


Figure 25. Maximum V_S Negative Offset vs VCC/VBS Supply Voltage

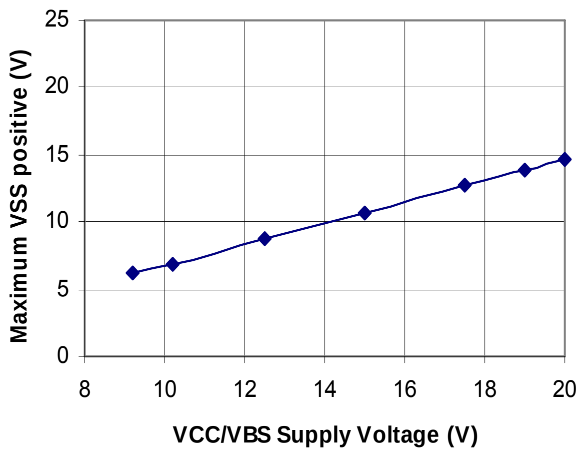
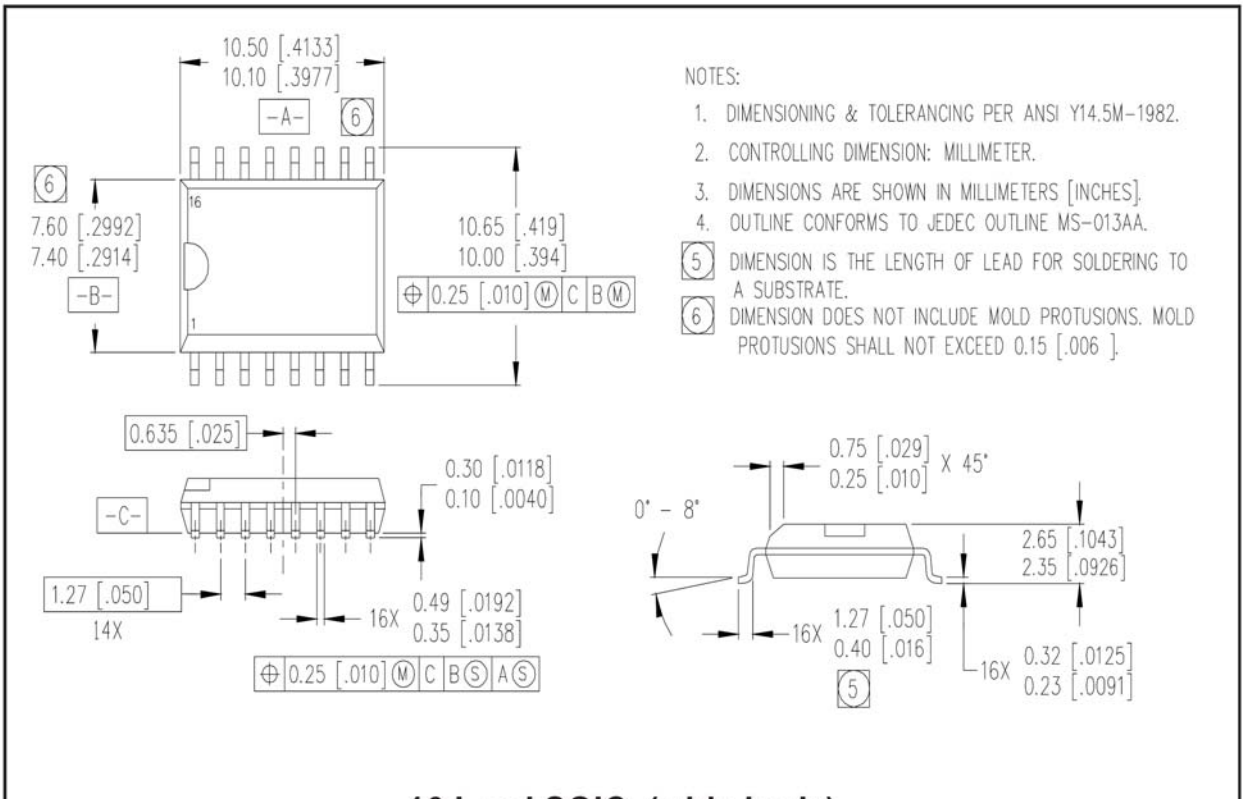


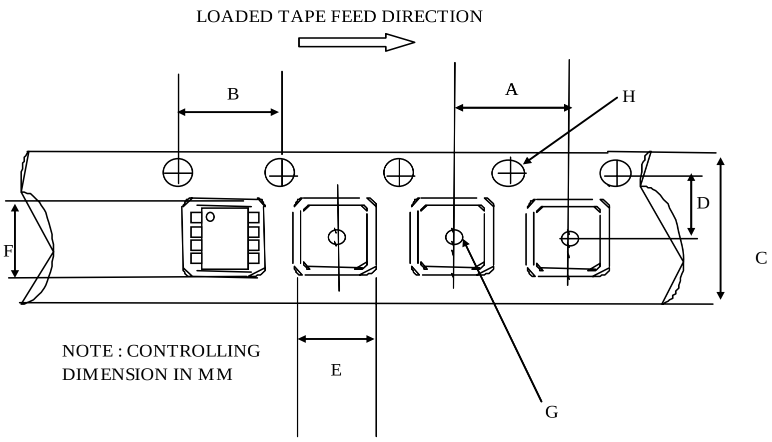
Figure 26. Maximum V_{SS} Positive Offset vs VCC/VBS Supply Voltage

Package Details: SOIC16W



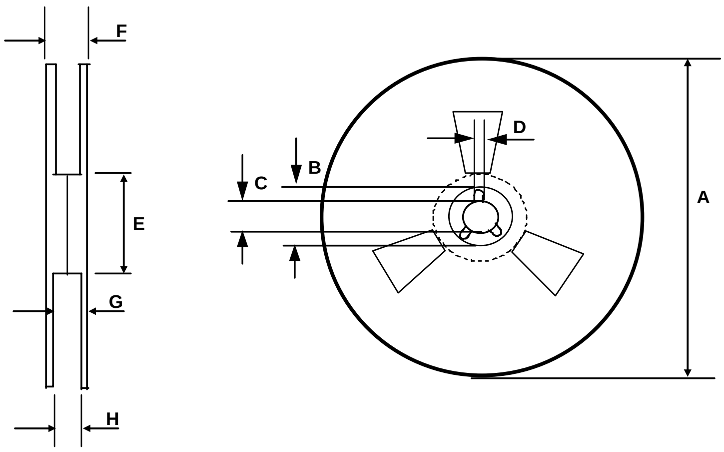
16 Lead SOIC (wide body)

Tape and Reel Details: SOIC16W



CARRIER TAPE DIMENSION FOR 16SOICW

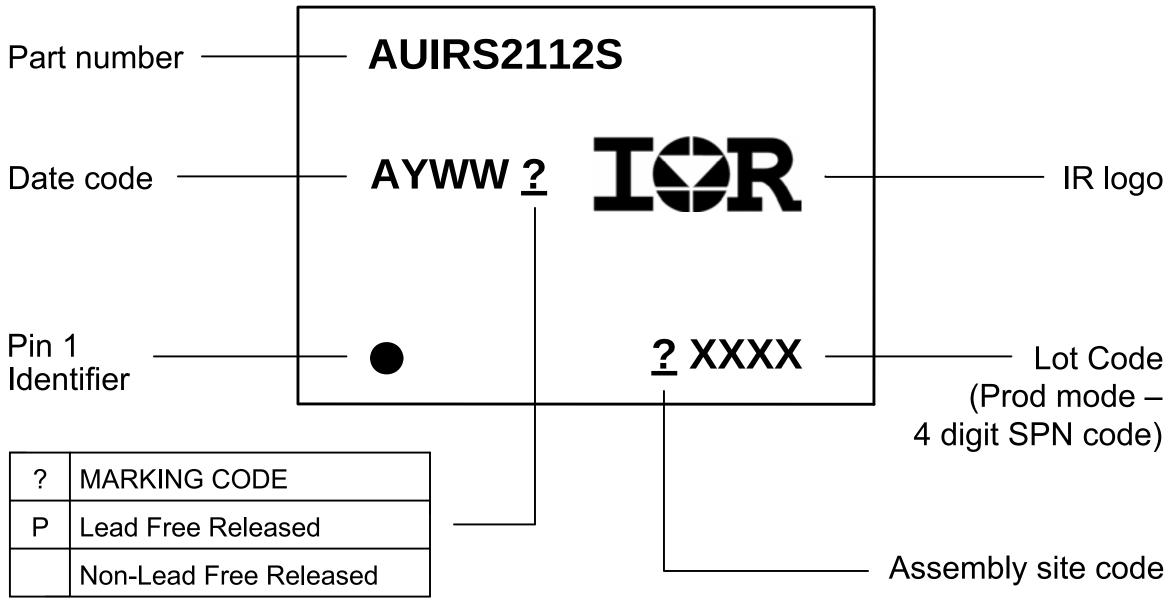
	Metric		Imperial	
Code	Min	Max	Min	Max
A	11.90	12.10	0.468	0.476
B	3.90	4.10	0.153	0.161
C	15.70	16.30	0.618	0.641
D	7.40	7.60	0.291	0.299
E	10.80	11.00	0.425	0.433
F	10.60	10.80	0.417	0.425
G	1.50	n/a	0.059	n/a
H	1.50	1.60	0.059	0.062



REEL DIMENSIONS FOR 16SOICW

	Metric		Imperial	
Code	Min	Max	Min	Max
A	329.60	330.25	12.976	13.001
B	20.95	21.45	0.824	0.844
C	12.80	13.20	0.503	0.519
D	1.95	2.45	0.767	0.096
E	98.00	102.00	3.858	4.015
F	n/a	22.40	n/a	0.881
G	18.50	21.10	0.728	0.830
H	16.40	18.40	0.645	0.724

Part Marking Information



Ordering Information

Base Part Number	Package Type	Standard Pack		Complete Part Number
		Form	Quantity	
AUIRS2112S	SOIC16W	Tube/Bulk	45	AUIRS2112S
		Tape and Reel	1000	AUIRS2112STR

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