

REVISIONS

LTR	DESCRIPTION	DATE (YR-MO-DA)	APPROVED

REV																				
SHEET																				
REV																				
SHEET	15	16																		
REV STATUS OF SHEETS	REV																			
	SHEET		1	2	3	4	5	6	7	8	9	10	11	12	13	14				
PMIC N/A	PREPARED BY Gary L. Gross				DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216															
<b>STANDARD MICROCIRCUIT DRAWING</b>  THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE  AMSC N/A	CHECKED BY Charles F. Saffle																			
	APPROVED BY Monica L. Poelking				MICROCIRCUIT, DIGITAL, LOW VOLTAGE CMOS, QUADRUPLE 2-INPUT EXCLUSIVE-OR GATE, MONOLITHIC SILICON															
	DRAWING APPROVAL DATE 97-11-25																			
	REVISION LEVEL				SIZE <b>A</b>	CAGE CODE <b>67268</b>	<b>5962-97619</b>													
				SHEET		1 OF 16														

DSCC FORM 2233  
APR 97

5962-E090-98

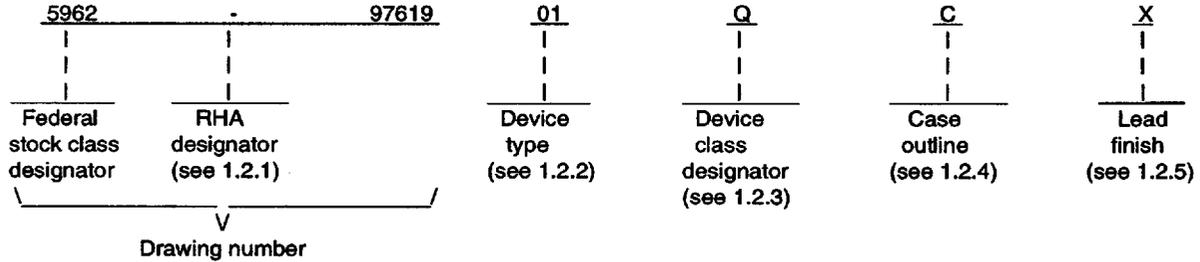
DISTRIBUTION STATEMENT A. Approved for public release; distribution is unlimited.

9004708 0033719 420

1. SCOPE

1.1 **Scope.** This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 **PIN.** The PIN is as shown in the following example:



1.3 Absolute maximum ratings. 1/ 2/ 3/

Supply voltage range ( $V_{CC}$ )	-0.5 V dc to +6.5 V dc
DC input voltage range ( $V_{IN}$ )	-0.5 V dc to +6.5 V dc 4/
DC output voltage range ( $V_{OUT}$ )	-0.5 V dc to $V_{CC} + 0.5$ V dc 4/ 5/
DC input clamp current ( $I_{IK}$ ) ( $V_{IN} < 0.0$ V)	-50 mA
DC output clamp current ( $I_{OK}$ ) ( $V_{OUT} < 0.0$ V or $V_{OUT} > V_{CC}$ )	$\pm 50$ mA
Continuous output current ( $I_{OL}$ ) ( $V_{OUT} = 0.0$ V to $V_{CC}$ )	$\pm 50$ mA
Continuous current through $V_{CC}$ or GND	$\pm 100$ mA
Maximum power dissipation at $T_A = +55^\circ\text{C}$ (in still air)	500 mW 6/
Storage temperature range ( $T_{STG}$ )	$-65^\circ\text{C}$ to $+150^\circ\text{C}$
Lead temperature (soldering, 10 seconds)	$+300^\circ\text{C}$
Thermal resistance, junction-to-case ( $\theta_{JC}$ )	See MIL-STD-1835
Junction temperature ( $T_J$ )	$+150^\circ\text{C}$

1.4 Recommended operating conditions. 2/ 3/ 7/

Supply voltage range ( $V_{CC}$ ):	
Operating	+2.0 V dc to +3.6 V dc
Data retention only (minimum)	+1.5 V dc
Minimum high level input voltage ( $V_{IH}$ ) ( $V_{CC} = 2.7$ V to 3.6 V)	+2.0 V dc
Maximum low level input voltage ( $V_{IL}$ ) ( $V_{CC} = 2.7$ V to 3.6 V)	+0.8 V dc
Input voltage range ( $V_{IN}$ )	0.0 V to +5.5 V dc
Output voltage range ( $V_{OUT}$ )	0.0 V to $V_{CC}$
Maximum high level output current ( $I_{OH}$ ):	
$V_{CC} = 2.7$ V	-12 mA
$V_{CC} = 3.0$ V	-24 mA
Maximum low level output current ( $I_{OL}$ ):	
$V_{CC} = 2.7$ V	+12 mA
$V_{CC} = 3.0$ V	+24 mA
Input transition rise or fall time ( $\Delta t/\Delta V$ )	0.0 ns/V to 9.0 ns/V
Case operating temperature range ( $T_C$ )	$-55^\circ\text{C}$ to $+125^\circ\text{C}$

1.5 Digital logic testing for device classes Q and V.

Fault coverage measurement of manufacturing logic tests (MIL-STD-883, test method 5012)	XX percent 8/
---	---------------

- 1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.
- 2/ Unless otherwise noted, all voltages are referenced to GND.
- 3/ The limits for the parameters specified herein shall apply over the full specified  $V_{CC}$  range and case temperature range of  $-55^\circ\text{C}$  to  $+125^\circ\text{C}$ .
- 4/ The input and output negative voltage ratings may be exceeded provided that the input and output clamp current ratings are observed.
- 5/ The value of  $V_{CC}$  is provided in the recommended operating conditions table.
- 6/ The maximum package power dissipation is calculated using a junction temperature of  $150^\circ\text{C}$  and a board trace length of 750 mils.
- 7/ Unused inputs must be held high or low to prevent them from floating.
- 8/ Values will be added when they become available.

<b>STANDARD MICROCIRCUIT DRAWING</b>	<b>SIZE A</b>	<b>5962- 97619</b>
<b>DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000</b>	<b>REVISION LEVEL</b>	<b>SHEET 3</b>

DSCC FORM 2234  
APR 97

■ 9004708 0033721 089 ■

**2. APPLICABLE DOCUMENTS**

**2.1 Government specification, standards, and handbooks.** The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation.

**SPECIFICATION**

**DEPARTMENT OF DEFENSE**

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

**STANDARDS**

**DEPARTMENT OF DEFENSE**

- MIL-STD-883 - Test Method Standard Microcircuit.
- MIL-STD-973 - Configuration Management.
- MIL-STD-1835 - Interface Standard for Microcircuit Case Outlines.

**HANDBOOKS**

**DEPARTMENT OF DEFENSE**

- MIL-HDBK-103 - List of Standard Microcircuit Drawings (SMD's).
- MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, and handbooks are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

**2.2 Order of precedence.** In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

**3. REQUIREMENTS**

**3.1 Item requirements.** The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

**3.2 Design, construction, and physical dimensions.** The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

**3.2.1 Case outlines.** The case outlines shall be in accordance with 1.2.4 herein.

**3.2.2 Terminal connections.** The terminal connections shall be as specified on figure 1.

**3.2.3 Truth table.** The truth table shall be as specified on figure 2.

**3.2.4 Logic diagram.** The logic diagram shall be as specified on figure 3.

**3.2.5 Ground bounce test circuit and waveforms.** The ground bounce test circuit and waveforms shall be as specified on figure 4.

<b>STANDARD MICROCIRCUIT DRAWING</b>  <b>DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000</b>	<b>SIZE A</b>		<b>5962- 97619</b>
		<b>REVISION LEVEL</b>	<b>SHEET 4</b>

DSCC FORM 2234  
APR 97

■ 9004708 0033722 T15 ■

[查询"5962-9761901Q2A"供应商](#)

3.2.6 Switching waveforms and test circuit. The switching waveforms and test circuit shall be as specified on figure 5.

3.2.7 Radiation exposure circuit. The radiation exposure circuit shall be as specified when available.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-HDBK-103. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DSCC-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-973.

3.9 Verification and review for device class M. For device class M, DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 36 (see MIL-PRF-38535, appendix A).

<b>STANDARD MICROCIRCUIT DRAWING</b>	<b>SIZE A</b>		<b>5962- 97619</b>
		<b>REVISION LEVEL</b>	<b>SHEET 5</b>
<b>DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000</b>			

DSCC FORM 2234  
APR 97

■ 9004708 0033723 951 ■

TABLE I. Electrical performance characteristics.

Test and MIL-STD-883 test method <sup>1/</sup>	Symbol	Test conditions <sup>2/</sup> -55°C ≤ T <sub>C</sub> ≤ +125°C +2.0 V ≤ V <sub>CC</sub> ≤ +3.6 V unless otherwise specified	Device type	V <sub>CC</sub>	Group A subgroups	Limits <sup>3/</sup>		Unit
						Min	Max	
High level output voltage 3006	V <sub>OH</sub>	For all inputs affecting output under test, V <sub>IN</sub> = 2.0 V or 0.8 V I <sub>OH</sub> = -100 μA, For all other inputs, V <sub>IN</sub> = V <sub>CC</sub> or GND.	All	2.7 V and 3.6 V	1,2,3	V <sub>CC</sub> - 0.2		V
		For all inputs affecting output under test, V <sub>IN</sub> = 2.0 V or 0.8 V I <sub>OH</sub> = -12 mA, For all other inputs, V <sub>IN</sub> = V <sub>CC</sub> or GND.	All	2.7 V	1,2,3	2.2		
				3.0 V		2.4		
For all inputs affecting output under test, V <sub>IN</sub> = 2.0 V or 0.8 V I <sub>OH</sub> = -24 mA, For all other inputs, V <sub>IN</sub> = V <sub>CC</sub> or GND.	All	3.0 V	1,2,3	2.2				
Low level output voltage 3007	V <sub>OL</sub>	For all inputs affecting output under test, V <sub>IN</sub> = 2.0 V or 0.8 V I <sub>OL</sub> = 100 μA, For all other inputs, V <sub>IN</sub> = V <sub>CC</sub> or GND.	All	2.7 V and 3.6 V	1,2,3		0.2	V
		For all inputs affecting output under test, V <sub>IN</sub> = 2.0 V or 0.8 V I <sub>OL</sub> = 12 mA, For all other inputs, V <sub>IN</sub> = V <sub>CC</sub> or GND.	All	2.7 V	1,2,3		0.4	
				3.0 V			0.55	
For all inputs affecting output under test, V <sub>IN</sub> = 2.0 V or 0.8 V I <sub>OL</sub> = 24 mA, For all other inputs, V <sub>IN</sub> = V <sub>CC</sub> or GND.	All	3.0 V	1,2,3					
Input current high 3010	I <sub>IH</sub>	For input under test, V <sub>IN</sub> = 5.5 V. For all other inputs, V <sub>IN</sub> = V <sub>CC</sub> or GND.	All	3.6 V	1,2,3		+5.0	μA
Input current low 3009	I <sub>IL</sub>	For input under test, V <sub>IN</sub> = GND. For all other inputs, V <sub>IN</sub> = V <sub>CC</sub> or GND.	All	3.6 V	1,2,3		-5.0	
Quiescent supply current 3005	I <sub>CC</sub>	For all inputs, V <sub>IN</sub> = V <sub>CC</sub> or GND I <sub>OUT</sub> = 0.0 A	All	3.6 V	1,2,3		10.0	μA
Quiescent supply current delta TTL input levels 3005	ΔI <sub>CC</sub>	One input at V <sub>CC</sub> - 0.6 V, other inputs at V <sub>CC</sub> or GND	All	2.7 V and 3.6 V	1,2,3		500	μA

See footnotes at end of table.

<b>STANDARD MICROCIRCUIT DRAWING</b>  <b>DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000</b>	<b>SIZE A</b>		<b>5962- 97619</b>
		REVISION LEVEL	SHEET <b>6</b>

DSCC FORM 2234  
APR 97

9004708 0033724 898

TABLE I. Electrical performance characteristics - Continued.

Test and MIL-STD-883 test method <u>1/</u>	Symbol	Test conditions <u>2/</u> -55°C ≤ T <sub>C</sub> ≤ +125°C +2.0 V ≤ V <sub>CC</sub> ≤ +3.6 V unless otherwise specified	Device type	V <sub>CC</sub>	Group A subgroups	Limits <u>3/</u>		Unit
						Min	Max	
Input capacitance 3012	C <sub>IN</sub>	T <sub>C</sub> = +25°C V <sub>IN</sub> = V <sub>CC</sub> or GND See 4.4.1c	All	3.3 V	4		10.0	pF
Power dissipation capacitance	C <sub>PD</sub> <u>4/</u>	C <sub>L</sub> = 50 pF minimum f = 10 MHz See 4.4.1c	All	3.3 V	4		10.0	pF
Low level ground bounce noise	V <sub>OLP</sub> <u>5/</u>	V <sub>IH</sub> = 2.7 V, V <sub>IL</sub> = 0.0 V T <sub>A</sub> = +25° C See figure 4 See 4.4.1d	All	3.3 V	4		1500	mV
Low level ground bounce noise	V <sub>OLV</sub> <u>5/</u>		All	3.3 V	4		-1500	
High level V <sub>CC</sub> bounce noise	V <sub>OHP</sub> <u>5/</u>		All	3.3 V	4		750	
High level V <sub>CC</sub> bounce noise	V <sub>OHV</sub> <u>5/</u>		All	3.3 V	4		-750	
Functional test 3014	<u>6/</u>	V <sub>IN</sub> = V <sub>IL</sub> or V <sub>IH</sub> Verify output V <sub>O</sub> See 4.4.1b	All	1.5 V 2.0 V 2.7 V 3.6 V	7,8	L	H	
Propagation delay time, mA or mB to mY 3003	t <sub>PLH</sub> t <sub>PHL</sub> <u>7/</u>	C <sub>L</sub> = 50 pF minimum See Figure 5	All	2.7 V	9,10,11		5.6	ns
				3.0 V and 3.6 V		1.0	4.6	
Output skew	t <sub>sk(o)</sub> <u>8/</u>	C <sub>L</sub> = 50 pF minimum	All	3.0 V and 3.6 V	9		1.0	ns

See footnotes on next sheet.

<b>STANDARD MICROCIRCUIT DRAWING</b>  <b>DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000</b>	<b>SIZE A</b>		<b>5962- 97619</b>
		REVISION LEVEL	SHEET <b>7</b>

DSCC FORM 2234  
APR 97

9004708 0033725 724

TABLE I. Electrical performance characteristics - Continued

- 1/ For tests not listed in the referenced MIL-STD-883 (e.g.  $\Delta I_{CC}$ ), utilize the general test procedure of 883 under the conditions listed herein.
- 2/ Each input/output, as applicable, shall be tested at the specified temperature, for the specified limits, to the tests in table I herein. Output terminals not designated shall be high level logic, low level logic, or open, except for all  $I_{CC}$  and  $\Delta I_{CC}$  tests, where the output terminals shall be open. When performing these tests, the current meter shall be placed in the circuit such that all current flows through the meter. For input terminals not designated,  $V_{IN} = 3.0 \text{ V}$  or  $V_{IN} = \text{GND}$ .
- 3/ For negative and positive voltage and current values, the sign designates the potential difference in reference to GND and the direction of current flow, respectively; and the absolute value of the magnitude, not the sign, is relative to the minimum and maximum limits, as applicable, listed herein.
- 4/ Power dissipation capacitance ( $C_{PD}$ ) determines both the power consumption ( $P_D$ ) and current consumption ( $I_S$ ). Where:  

$$P_D = (C_{PD} + C_L) (V_{CC} \times V_{CC})f + (I_{CC} \times V_{CC})$$

$$I_S = (C_{PD} + C_L) V_{CC}f + I_{CC}$$
 $f$  is the frequency of the input signal; and  $C_L$  is the external output load capacitance.
- 5/ This test is for qualification only. Ground and  $V_{CC}$  bounce tests are performed on a non-switching (quiescent) output and are used to measure the magnitude of induced noise caused by other simultaneously switching outputs. The test is performed on a low noise bench test fixture. For the device under test, all outputs shall be loaded with  $500\Omega$  of load resistance and a minimum of  $50 \text{ pF}$  of load capacitance (see figure 4). Only chip capacitors and resistors shall be used. The output load components shall be located as close as possible to the device outputs. It is suggested, that whenever possible, this distance be kept to less than 0.25 inches. Decoupling capacitors shall be placed in parallel from  $V_{CC}$  to ground. The values of these decoupling capacitors shall be determined by the device manufacturer. The low and high level ground and  $V_{CC}$  bounce noise is measured at the quiet output using a 1 GHz minimum bandwidth oscilloscope with a  $50\Omega$  input impedance.  
  
 The device inputs shall be conditioned such that all outputs are at a high nominal  $V_{OH}$  level. The device inputs shall then be conditioned such that they switch simultaneously and the output under test remains at  $V_{OH}$  as all other outputs possible are switched from  $V_{OH}$  to  $V_{OL}$ .  $V_{OHV}$  and  $V_{OHP}$  are then measured from the nominal  $V_{OH}$  level to the largest negative and positive peaks, respectively (see figure 4). This is then repeated with the same outputs not under test switching from  $V_{OL}$  to  $V_{OH}$ .  
  
 The device inputs shall be conditioned such that all outputs are at a low nominal  $V_{OL}$  level. The device inputs shall then be conditioned such that they switch simultaneously and the output under test remains at  $V_{OL}$  as all other outputs possible are switched from  $V_{OL}$  to  $V_{OH}$ .  $V_{OLP}$  and  $V_{OLV}$  are then measured from the nominal  $V_{OL}$  level to the largest positive and negative peaks, respectively (see figure 4). This is then repeated with the same outputs not under test switching from  $V_{OH}$  to  $V_{OL}$ .
- 6/ Tests shall be performed in sequence, attributes data only. Functional tests shall include the truth table and other logic patterns used for fault detection. The test vectors used to verify the truth table shall, at a minimum, test all functions of each input and output. All possible input to output logic patterns per function shall be guaranteed, if not tested, to the truth table in figure 2 herein. Functional tests shall be performed in sequence as approved by the qualifying activity on qualified devices. Allowable tolerances per MIL-STD-883 may be incorporated. For outputs,  $L \leq 0.8 \text{ V}$ ,  $H \geq 2.0 \text{ V}$ .
- 7/ For propagation delay tests, all paths must be tested.
- 8/ Skew between any two outputs of the same package switching in the same direction. This parameter is warranted, but not production tested.

<b>STANDARD MICROCIRCUIT DRAWING</b>  <b>DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000</b>	<b>SIZE A</b>		<b>5962- 97619</b>
		<b>REVISION LEVEL</b>	<b>SHEET 8</b>

DSCC FORM 2234  
APR 97

9004708 0033726 660

Device type	All	
Case outlines	C, D	2
Terminal number	Terminal symbol	Terminal symbol
1	1A	NC
2	1B	1A
3	1Y	1B
4	2A	1Y
5	2B	NC
6	2Y	2A
7	GND	NC
8	3Y	2B
9	3A	2Y
10	3B	GND
11	4Y	NC
12	4A	3Y
13	4B	3A
14	V <sub>cc</sub>	3B
15	---	NC
16	---	4Y
17	---	NC
18	---	4A
19	---	4B
20	---	V <sub>cc</sub>

NC = No connection

FIGURE 1. Terminal connections.

<b>STANDARD MICROCIRCUIT DRAWING</b>  <b>DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000</b>	<b>SIZE A</b>		<b>5962- 97619</b>
		<b>REVISION LEVEL</b>	<b>SHEET 9</b>

DSCC FORM 2234  
APR 97

■ 9004708 0033727 5T7 ■

Inputs (each gate)		Outputs (each gate)
mA	mB	mY
L	L	L
L	H	H
H	L	H
H	H	L

H = High voltage level  
L = Low voltage level

FIGURE 2. Truth table.

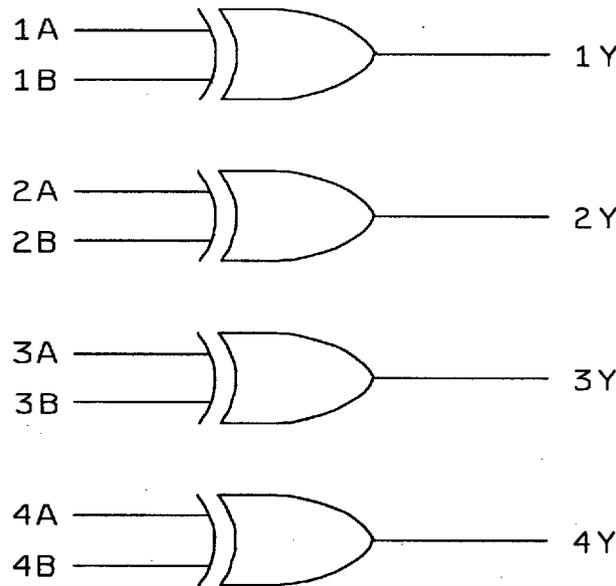
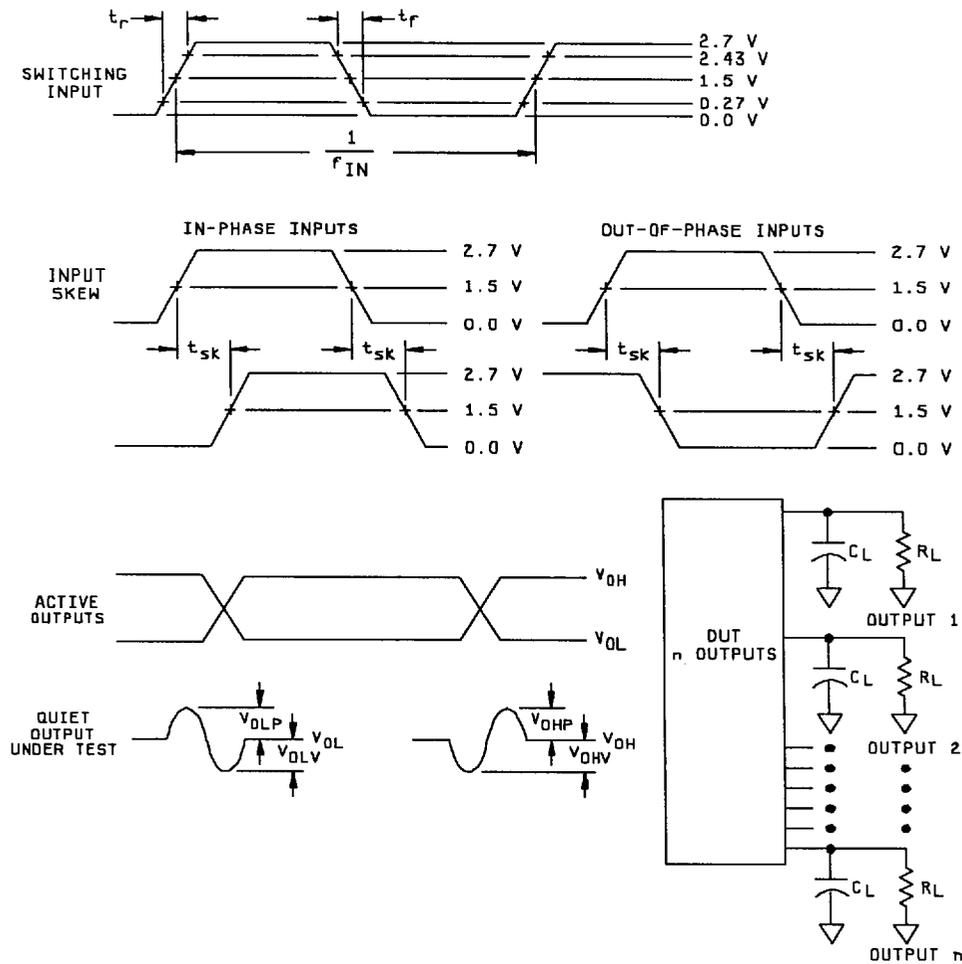


FIGURE 3. Logic diagram.

<b>STANDARD MICROCIRCUIT DRAWING</b>  <b>DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000</b>	<b>SIZE A</b>		<b>5962- 97619</b>
		<b>REVISION LEVEL</b>	<b>SHEET 10</b>

DSCC FORM 2234  
APR 97

■ 9004708 0033728 433 ■

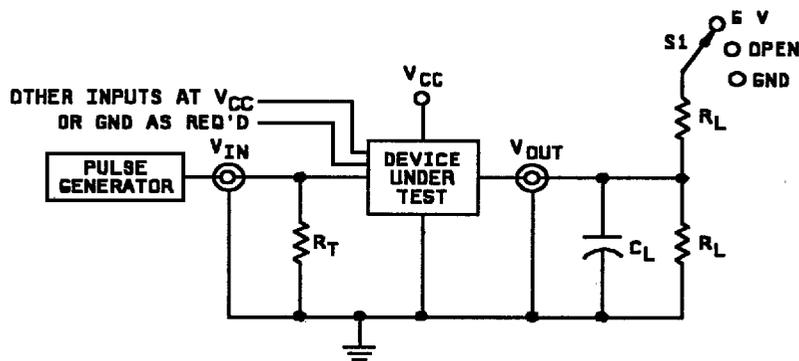
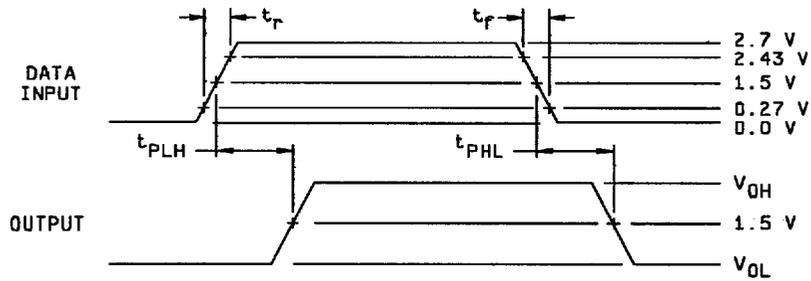


**NOTES:**

1.  $C_L$  includes a 47 pF chip capacitor (-0 percent, +20 percent) and at least 3 pF of equivalent capacitance from the test jig and probe.
2.  $R_L = 450\Omega \pm 1$  percent, chip resistor in series with a  $50\Omega$  termination. For monitored outputs, the  $50\Omega$  termination shall be the  $50\Omega$  characteristic impedance of the coaxial connector to the oscilloscope.
3. Input signal to the device under test:
  - a.  $V_{IN} = 0.0$  V to 2.7 V; duty cycle = 50 percent;  $f_{IN} \geq 1$  MHz.
  - b.  $t_r, t_f = 3.0$  ns  $\pm 1.0$  ns. For input signal generators incapable of maintaining these values of  $t_r$  and  $t_f$ , the 3.0 ns limit may be increased up to 10 ns, as needed, maintaining the  $\pm 1.0$  ns tolerance and guaranteeing the results at 3.0 ns  $\pm 1.0$  ns; skew between any two switching inputs signals ( $t_{sk}$ ):  $\leq 250$  ps.

FIGURE 4. Ground bounce test circuit and waveforms.

<b>STANDARD MICROCIRCUIT DRAWING</b>  <b>DEFENSE SUPPLY CENTER COLUMBUS</b> <b>COLUMBUS, OHIO 43216-5000</b>	<b>SIZE A</b>		<b>5962- 97619</b>
		REVISION LEVEL	SHEET <b>11</b>



**NOTES:**

1. When measuring  $t_{PLH}$  and  $t_{PHL}$ , S1= open.
2.  $C_L = 50$  pF (includes test jig and probe capacitance).
3.  $R_L = 500\Omega$ ,  $R_T = 50\Omega$  or equivalent.
4. Input signal from pulse generator:  $V_{IN} = 0.0$  V to 2.7 V;  $PRR \leq 10$  MHz;  $t_r = 2.5$  ns;  $t_f = 2.5$  ns;  $t_r$  and  $t_f$  shall be measured from 0.27 V to 2.43V and from 2.43 V to 0.27 V, respectively; duty cycle = 50 percent.
5. Timing parameters shall be tested at a minimum input frequency of 1 MHz.
6. The outputs are measured one at a time with one transition per measurement

FIGURE 5. Switching waveforms and test circuit.

<b>STANDARD MICROCIRCUIT DRAWING</b>  <b>DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000</b>	<b>SIZE A</b>		<b>5962- 97619</b>
		<b>REVISION LEVEL</b>	<b>SHEET 12</b>

4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

- a. Burn-in test, method 1015 of MIL-STD-883.
  - (1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.
  - (2)  $T_A = +125^\circ\text{C}$ , minimum.
- b. Interim and final electrical test parameters shall be as specified in table II herein.

4.2.2 Additional criteria for device classes Q and V.

- a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.
- b. Interim and final electrical test parameters shall be as specified in table II herein.
- c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-PRF-38535 permits alternate in-line control testing. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

<b>STANDARD MICROCIRCUIT DRAWING</b>  <b>DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000</b>	<b>SIZE A</b>		<b>5962- 97619</b>
		REVISION LEVEL	SHEET 13

- a. Tests shall be as specified in table II herein.
- b. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the truth table in figure 2 herein. The test vectors used to verify the truth table shall, at a minimum, test all functions of each input and output. All possible input to output logic patterns per function shall be guaranteed, if not tested, to the truth table in figure 2, herein. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device; these tests shall have been fault graded in accordance with MIL-STD-883, test method 5012 (see 1.5 herein).
- c.  $C_{IN}$  and  $C_{PD}$  shall be measured only for initial qualification and after process or design changes which may affect capacitance.  $C_{IN}$  shall be measured between the designated terminal and GND at a frequency of 1 MHz. This test may be performed at 10 MHz and guaranteed, if not tested, at 1 MHz.  $C_{PD}$  shall be tested in accordance with the latest revision of JEDEC Standard No. 20 and table I herein. The DC bias for the pin under test ( $V_{BIAS}$ ) = 2.5 V or 3.0 V. For  $C_{IN}$ , and  $C_{PD}$ , test all applicable pins on five devices with zero failures.

For  $C_{IN}$ , a device manufacturer may qualify devices by functional groups. A specific functional group shall be composed of function types, that by design, will yield the same capacitance values when tested in accordance with table I, herein. The device manufacturer shall set a function group limit for the  $C_{IN}$  test. The device manufacturer may then test one device functional group, to the limits and conditions specified herein. All other device functions in that particular functional group shall be guaranteed, if not tested, to the limits and test conditions specified in table I, herein. The device manufacturers shall submit to DSCC-VA the device functions listed in each functional group and the test results for each device tested.

- d. Ground and  $V_{CC}$  bounce tests are required for all device classes. These tests shall be performed only for initial qualification, after process or design changes which may affect the performance of the device, and any changes to the test fixture.  $V_{OLP}$ ,  $V_{OLV}$ ,  $V_{OHP}$ , and  $V_{OHV}$  shall be measured for the worst case outputs of the device. All other outputs shall be guaranteed, if not tested, to the limits established for the worst case outputs. The worst case outputs tested are to be determined by the manufacturer. Test 5 devices assembled in the worst case package type supplied to this document. All other package types shall be guaranteed, if not tested, to the limits established for the worst case package. The 5 devices to be tested shall be the worst case device type supplied to this drawing. All other device types shall be guaranteed, if not tested, to the limits established for the worst case device type. The package type and device type to be tested shall be determined by the manufacturer. The device manufacturer will submit to DSCC-VA data that shall include all measured peak values for each device tested and detailed oscilloscope plots for each  $V_{OLP}$ ,  $V_{OLV}$ ,  $V_{OHP}$ , and  $V_{OHV}$  from one sample part per function. The plot shall contain the waveforms of both a switching output and the output under test.

Each device manufacturer shall test product on the fixtures they currently use. When a new fixture is used, the device manufacturer shall inform DSCC-VA of this change and test the 5 devices on both the new and old test fixtures. The device manufacturer shall then submit to DSCC-VA data from testing on both fixtures, that shall include all measured peak values for each device tested and detailed oscilloscope plots for each  $V_{OLP}$ ,  $V_{OLV}$ ,  $V_{OHP}$ , and  $V_{OHV}$  from one sample part per function. The plot shall contain the waveforms of both a switching output and the output under test.

For  $V_{OHP}$ ,  $V_{OHV}$ ,  $V_{OLP}$ , and  $V_{OLV}$ , a device manufacturer may qualify devices by functional groups. A specific functional group shall be composed of function types, that by design, will yield the same test values when tested in accordance with table I, herein. The device manufacturer shall set a functional group limit for the  $V_{OHP}$ ,  $V_{OHV}$ ,  $V_{OLP}$ , and  $V_{OLV}$  tests. The device manufacturer may then test one device function from a functional group, to the limits and conditions specified herein. All other device functions in that particular functional group shall be guaranteed, if not tested, to the limits and conditions specified in table I, herein. The device manufacturers shall submit to DSCC-VA the device functions listed in each functional group and test results, along with the oscilloscope plots, for each device tested.

<b>STANDARD MICROCIRCUIT DRAWING</b>  <b>DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000</b>	<b>SIZE A</b>		<b>5962- 97619</b>
		<b>REVISION LEVEL</b>	<b>SHEET 14</b>

DSCC FORM 2234  
 APR 97

■ 9004708 0033732 964 ■

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

- b.  $T_A = +125^\circ\text{C}$ , minimum.
- c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.

4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

- a. End-point electrical parameters shall be as specified in table II herein.
- b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at  $T_A = +25^\circ\text{C} \pm 5^\circ\text{C}$ , after exposure, to the subgroups specified in table II herein.
- c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

4.5 Methods of inspection. Methods of inspection shall be specified as follows:

4.5.1 Voltage and current. Unless otherwise specified, all voltages given are referenced to the microcircuit GND terminal. Currents given are conventional current and positive when flowing into the referenced terminal.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.

<b>STANDARD MICROCIRCUIT DRAWING</b>  <b>DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000</b>	<b>SIZE A</b>		<b>5962- 97619</b>
		<b>REVISION LEVEL</b>	<b>SHEET 15</b>

TABLE II. Electrical test requirements.

Test requirements	Subgroups (in accordance with MIL-STD-883, method 5005, table I)	Subgroups (in accordance with MIL-PRF-38535, table III)	
	Device class M	Device class Q	Device class V
Interim electrical parameters (see 4.2)	---	---	1
Final electrical parameters (see 4.2)	1/ 1, 2, 3, 7, 8, 9, 10, 11	1/ 1, 2, 3, 7, 8, 9, 10, 11	2/ 1, 2, 3, 7, 8, 9, 10, 11
Group A test requirements (see 4.4)	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11	1, 2, 3, 4, 7, 8, 9, 10, 11
Group C end-point electrical parameters (see 4.4)	1, 2, 3	1, 2, 3	1, 2, 3, 7, 8, 9, 10, 11
Group D end-point electrical parameters (see 4.4)	1, 2, 3	1, 2, 3	1, 2, 3
Group E end-point electrical parameters (see 4.4)	1, 7, 9	1, 7, 9	1, 7, 9

1/ PDA applies to subgroup 1.  
2/ PDA applies to subgroups 1 and 7.

6.3 Record of users. Military and industrial users should inform Defense Supply Center Columbus when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0525.

6.4 Comments. Comments on this drawing should be directed to DSCC-VA, Columbus, Ohio 43216-5000; or telephone (614) 692-0674.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DSCC-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.

<b>STANDARD MICROCIRCUIT DRAWING</b>  <b>DEFENSE SUPPLY CENTER COLUMBUS COLUMBUS, OHIO 43216-5000</b>	<b>SIZE A</b>		<b>5962- 97619</b>
		<b>REVISION LEVEL</b>	<b>SHEET 16</b>

DSCC FORM 2234  
APR 97

9004708 0033734 737

DATE: 97-11-25

Approved sources of supply for SMD 5962-97619 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535.

Standard microcircuit drawing PIN <u>1/</u>	Vendor CAGE number	Vendor similar PIN <u>2/</u>
5962-9761901QCA	01295	SNJ54LVC86AJ
5962-9761901QDA	01295	SNJ54LVC86AW
5962-9761901Q2A	01295	SNJ54LVC86AFK

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. If the desired lead finish is not listed, contact the Vendor to determine its availability

2/ **Caution.** Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

Vendor CAGE number

01295

Vendor name and address

Texas Instruments Incorporated  
13500 N. Central Expressway  
P.O. Box 655303  
Dallas, TX 75265  
Point of contact: I-20 at FM 1788  
Midland, TX 79711-0448

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.

9004708 0033735 673