

SLPS201A -AUGUST 2009-REVISED SEPTEMBER 2010

# N-Channel NexFET™ Power MOSFETs

Check for Samples: CSD16403Q5A

### **FEATURES**

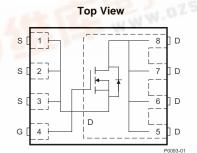
- Ultra Low Q<sub>q</sub> and Q<sub>qd</sub>
- **Low Thermal Resistance**
- **Avalanche Rated**
- **Pb Free Terminal Plating**
- **RoHS Compliant**
- **Halogen Free**
- SON 5mm x 6mm Plastic Package

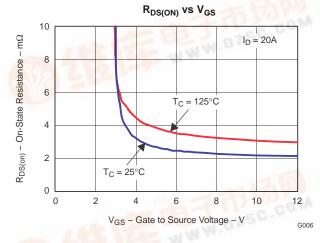
# **APPLICATIONS**

- Point-of-Load Synchronous Buck Converter for Applications in Networking, Telecom and Computing Systems
- **Optimized for Control FET Applications**

### DESCRIPTION

The NexFET™ power MOSFET has been designed to minimize losses in power conversion applications.





### PRODUCT SUMMARY

V <sub>DS</sub>	Drain to Source Voltage	25	V	
$Q_g$	Gate Charge Total (4.5V) 13.3			nC
$Q_{gd}$	Gate Charge Gate to Drain	e Gate to Drain 3.5		nC
<b>D</b>	Design to Course On Design	V <sub>GS</sub> = 4.5V	2.9	mΩ
R <sub>DS(on)</sub>	Drain to Source On Resistance	V <sub>GS</sub> = 10V	2.2	mΩ
V <sub>GS(th)</sub>	Threshold Voltage	1.6	V	

#### ORDERING INFORMATION

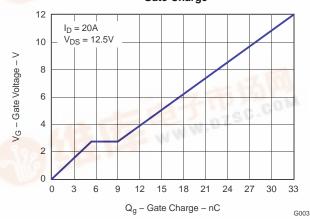
Device	Package	Media	Qty	Ship
CSD16403Q5A	SON 5X6 Plastic Package	13-inch reel	2500	Tape and Reel

### **ABSOLUTE MAXIMUM RATINGS**

$T_A = 2$	5°C unless otherwise stated	VALUE	UNIT
$V_{DS}$	Drain to Source Voltage	25	V
V <sub>GS</sub>	Gate to Source Voltage	+16 / -12	V
W	Continuous Drain Current, T <sub>C</sub> = 25°C	100	Α
ID	Continuous Drain Current <sup>(1)</sup>	28	Α
$I_{DM}$	Pulsed Drain Current, T <sub>A</sub> = 25°C <sup>(2)</sup>	184	Α
$P_D$	Power Dissipation <sup>(1)</sup>	3.1	W
$T_J$ , $T_{STG}$	Operating Junction and Storage Temperature Range	-55 to 150	°C
E <sub>AS</sub>	Avalanche Energy, single pulse $I_D = 67A$ , $L = 0.1 mH$ , $R_G = 25\Omega$	224	mJ
. ,	θJA = 41°C/W on 1in² Cu FR4 PCB.	SC.CO.	

- (1)  $R_{\theta JA} = 41^{\circ}\text{C/W on } 1\text{in}^2\text{ Cu FR4 PCB}.$
- (2) Pulse width ≤300μs, duty cycle ≤2%

### **Gate Charge**



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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

# **ELECTRICAL CHARACTERISTICS**

 $(T_A = 25^{\circ}C \text{ unless otherwise stated})$ 

$(1_A = 25)$	°C unless otherwise stated)					
	PARAMETER	TEST CONDITIONS	MIN	TYP	MAX	UNIT
Static C	haracteristics					
BV <sub>DSS</sub>	Drain to Source Voltage	$V_{GS} = 0V, I_D = 250\mu A$	25			V
$I_{DSS}$	Drain to Source Leakage Current	$V_{GS} = 0V$ , $V_{DS} = 20V$			1	μΑ
$I_{GSS}$	Gate to Source Leakage Current	$V_{DS} = 0V, V_{GS} = +16/-12V$			100	nA
$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\mu A$	1.2	1.6	1.9	V
D	Drain to Source On Resistance	$V_{GS} = 4.5V, I_D = 20A$		2.9	3.7	$m\Omega$
R <sub>DS(on)</sub>	Drain to Source On Resistance	$V_{GS} = 10V, I_D = 20A$		2.2	2.8	mΩ
9 <sub>fs</sub>	Transconductance	$V_{DS} = 15V, I_D = 20A$		91		S
Dynamic	c Characteristics					
C <sub>ISS</sub>	Input Capacitance			2040	2660	pF
Coss	Output Capacitance	$V_{GS} = 0V, V_{DS} = 12.5V, f = 1MHz$		1600	2080	pF
C <sub>RSS</sub>	Reverse Transfer Capacitance			115	160	pF
R <sub>g</sub>	Series Gate Resistance			1.2	2.4	Ω
Qg	Gate Charge Total (4.5V)			13.3	18	nC
Q <sub>gd</sub>	Gate Charge Gate to Drain	V 40 5V 1 20A		3.5		nC
$Q_{gs}$	Gate Charge Gate to Source	$V_{DS} = 12.5V, I_D = 20A$		5.5		nC
Qg(th)	Gate Charge at Vth			3.1		nC
Q <sub>OSS</sub>	Output Charge	$V_{DS} = 13.5V, V_{GS} = 0V$		33		nC
t <sub>d(on)</sub>	Turn On Delay Time			11.8		ns
t <sub>r</sub>	Rise Time	$V_{DS} = 12.5V, V_{GS} = 4.5V, I_{D} = 20A,$		18.3		ns
t <sub>d(off)</sub>	Turn Off Delay Time	$R_G = 2\Omega$		15.2		ns
t <sub>f</sub>	Fall Time			9.2		ns
Diode C	haracteristics		<b>"</b>		l	
V <sub>SD</sub>	Diode Forward Voltage	$I_{S} = 20A, V_{GS} = 0V$		0.8	1.0	V
Q <sub>rr</sub>	Reverse Recovery Charge	$V_{DD} = 13.5V$ , $I_F = 20A$ , $di/dt = 300A/\mu s$		47		nC
t <sub>rr</sub>	Reverse Recovery Time	$V_{DD} = 13.5V$ , $I_F = 20A$ , $di/dt = 300A/\mu s$		35		ns

### THERMAL CHARACTERISTICS

 $(T_A = 25^{\circ}C \text{ unless otherwise stated})$ 

	PARAMETER	MIN	TYP	MAX	UNIT
R $_{\theta JC}$	Thermal Resistance Junction to Case <sup>(1)</sup>			1.8	°C/W
R $_{\theta JA}$	Thermal Resistance Junction to Ambient <sup>(1)</sup> (2)			51	°C/W

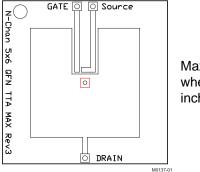
<sup>(1)</sup>  $R_{\theta JC}$  is determined with the device mounted on a 1 inch square 2 oz. Cu pad on a 1.5 x 1.5 in 0.060 inch thick FR4 board.  $R_{\theta JC}$  is specified by design while  $R_{\theta JA}$  is determined by the user's board design.

(2) Device mounted on FR4 Material with 1 inch<sup>2</sup> of 2 oz. Cu.

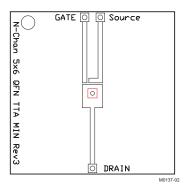
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Max  $R_{\theta JA} = 51$ °C/W when mounted on 1 inch<sup>2</sup> of 2 oz. Cu.



Max  $R_{\theta JA} = 118^{\circ} C/W$  when mounted on minimum pad area of 2 oz. Cu.

### TYPICAL MOSFET CHARACTERISTICS

 $(T_A = 25^{\circ}C \text{ unless otherwise stated})$ 

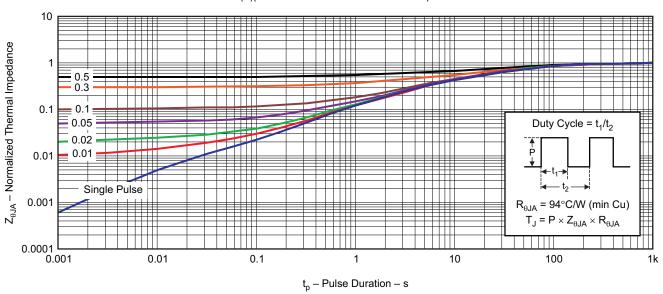


Figure 1. Transient Thermal Impedance

G012



# TYPICAL MOSFET CHARACTERISTICS (continued)

 $(T_A = 25^{\circ}C \text{ unless otherwise stated})$ 

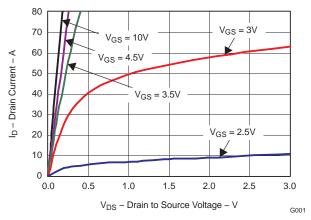


Figure 2. Saturation Characteristics

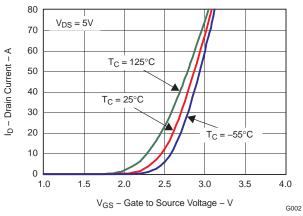


Figure 3. Transfer Characteristics

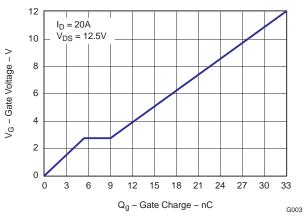


Figure 4. Gate Charge

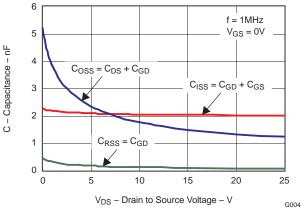


Figure 5. Capacitance

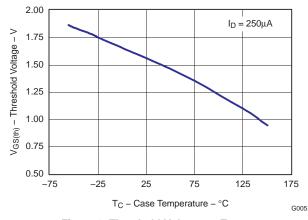


Figure 6. Threshold Voltage vs Temperature

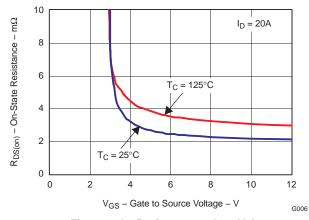


Figure 7. On Resistance vs Gate Voltage

# TYPICAL MOSFET CHARACTERISTICS (continued)

 $(T_A = 25^{\circ}C \text{ unless otherwise stated})$ 

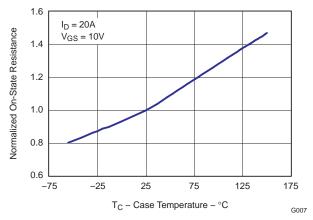


Figure 8. On Resistance vs Temperature

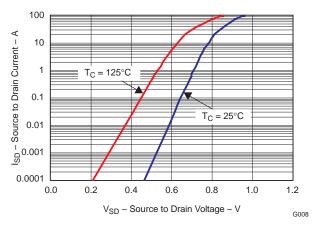


Figure 9. Typical Diode Forward Voltage

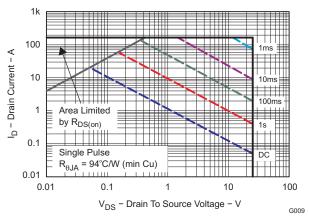


Figure 10. Maximum Safe Operating Area

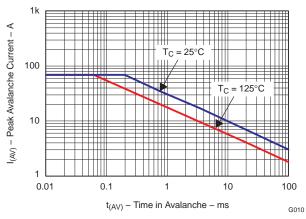


Figure 11. Single Pulse Unclamped Inductive Switching

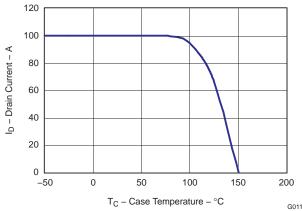
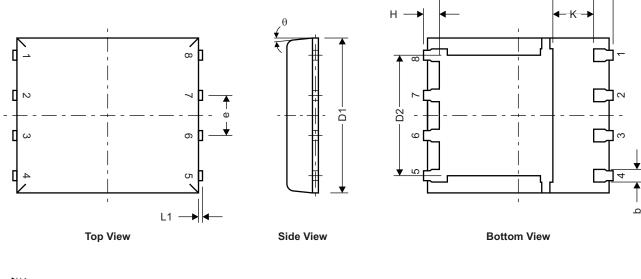


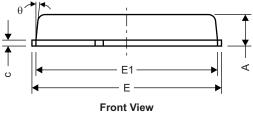
Figure 12. Maximum Drain Current vs Temperature



# **MECHANICAL DATA**

# **Q5A Package Dimensions**





M0135-01

DIM		MILLIMETERS	
	MIN	NOM	MAX
А	0.90	1.00	1.10
b	0.33	0.41	0.51
С	0.20	0.25	0.30
D1	4.80	4.90	5.00
D2	3.61	3.81	3.96
Е	5.90	6.00	6.10
E1	5.70	5.75	5.80
E2	3.38	3.58	3.78
е		1.27 BSC	
Н	0.41	0.51	0.61
K	1.10		
L	0.51	0.61	0.71
L1	0.06	0.13	0.20
θ	0°		12°

For recommended circuit layout for PCB designs, see application note SLPA005 – Reducing Ringing Through PCB Layout Techniques.

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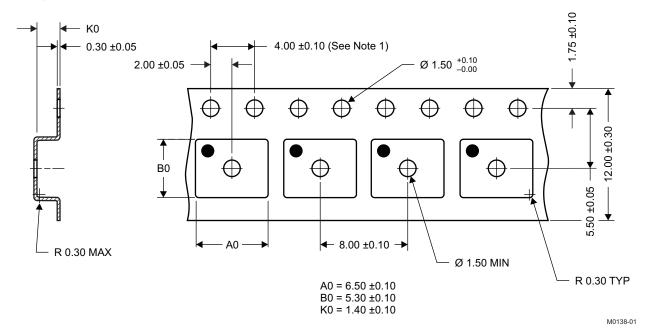
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Recommen	ded PCB Pattern
F6 -	F7
₩ F10	M0139-01

DIM	MILLIN	IETERS	INC	HES
DIN	MIN	MAX	MIN	MAX
F1	6.205	6.305	0.244	0.248
F2	4.46	4.56	0.176	0.18
F3	4.46	4.56	0.176	0.18
F4	0.65	0.7	0.026	0.028
F5	0.62	0.67	0.024	0.026
F6	0.63	0.68	0.025	0.027
F7	0.7	0.8	0.028	0.031
F8	0.65	0.7	0.026	0.028
F9	0.62	0.67	0.024	0.026
F10	4.9	5	0.193	0.197
F11	4.46	4.56	0.176	0.18

# **Q5A Tape and Reel Information**



#### Notes:

- 1. 10 sprocket hole pitch cumulative tolerance ±0.2
- 2. Camber not to exceed 1mm IN 100mm, noncumulative over 250mm
- 3. Material:black static dissipative polystyrene
- 4. All dimensions are in mm (unless otherwise specified)
- 5. A0 and B0 measured on a plane 0.3mm above the bottom of the pocket
- 6. MSL1 260°C (IR and Convection) PbF Reflow Compatible

### **REVISION HISTORY**

### Changes from Original (August 2009) to Revision A

Page



## PACKA

### PACKAGING INFORMATION

Orderable Device	Status <sup>(1)</sup>	Package Type	Package Drawing	Pins	Package Qty	Eco Plan <sup>(2)</sup>	Lead/ Ball Finish	MSL Pea
CSD16403Q5A	ACTIVE	SON	DQJ	8	2500	Pb-Free (RoHS Exempt)	CU SN	Level-1-2600

(1) The marketing status values are defined as follows:

ACTIVE: Product device recommended for new designs.

LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.

NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new

PREVIEW: Device has been announced but is not in production. Samples may or may not be available.

**OBSOLETE:** TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.information and additional product content details.

**TBD:** The Pb-Free/Green conversion plan has not been defined.

**Pb-Free** (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for **Pb-Free** (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.

Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retard in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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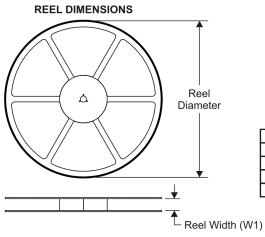
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# TAPE AND REEL INFORMATION





A0	Dimension designed to accommodate the component width
B0	Dimension designed to accommodate the component length
K0	Dimension designed to accommodate the component thickness
W	Overall width of the carrier tape
P1	Pitch between successive cavity centers

# QUADRANT ASSIGNMENTS FOR PIN 1 ORIENTATION IN TAPE

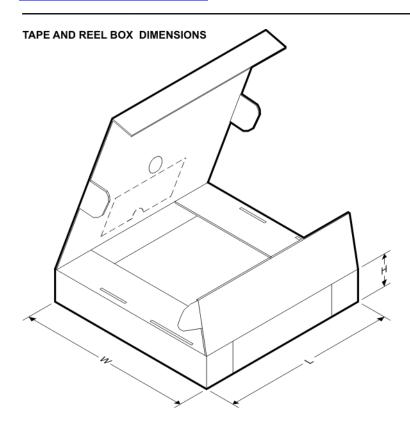


### \*All dimensions are nominal

Device	Package Type	Package Drawing			Reel Diameter (mm)	Reel Width W1 (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
CSD16403Q5A	SON	DQJ	8	2500	330.2	12.4	6.5	5.3	1.4	8.0	12.0	Q1

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12-Aug-2010



### \*All dimensions are nominal

Device	Package Type	Package Drawing	Pins	SPQ	Length (mm)	Width (mm)	Height (mm)
CSD16403Q5A	SON	DQJ	8	2500	347.0	342.0	55.0

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