**FAIRCHILD**
SEMICONDUCTOR™

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# 74ACT825
# 8-Bit D-Type Flip-Flop

## General Description

The ACT825 is an 8-bit buffered register. They have Clock Enable and Clear features which are ideal for parity bus interfacing in high performance microprogramming systems. Also included are multiple enables that allow multiuse control of the interface. The ACT825 has noninverting outputs.

## Features

■ Outputs source/sink 24 mA
■ Inputs and outputs are on opposite sides
■ TTL compatible inputs

## Ordering Code:

| Order Number | Package Number | Package Description |
|---|---|---|
| 74ACT825SC | M24B | 24-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide |
| 74ACT825MTC | MTC24 | 24-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide |
| 74ACT825SPC | N24C | 24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide |

Device also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

## Logic Symbols



**IEEE/IEC**
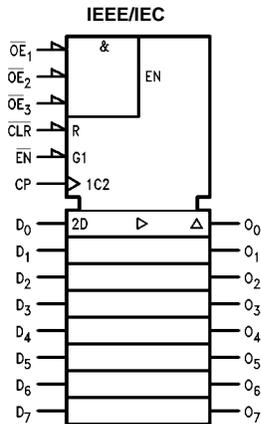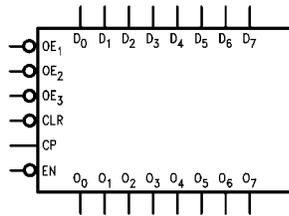


## Connection Diagram
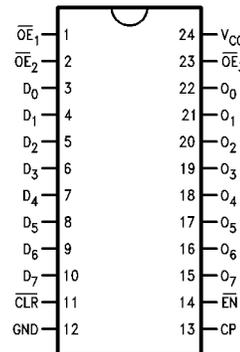


## Pin Descriptions

| Pin Names | Description |
|---|---|
| $D_0$–$D_7$ | Data Inputs |
| $O_0$–$O_7$ | Data Outputs |
| $\overline{OE}_1$, $\overline{OE}_2$, $\overline{OE}_3$ | Output Enables |
| $\overline{EN}$ | Clock Enable |
| $\overline{CLR}$ | Clear |
| CP | Clock Input |

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## Functional Description

The ACT825 consists of eight D-type edge-triggered flip-flops. These devices have 3-STATE outputs for bus systems, organized in a broadside pinning. In addition to the clock and output enable pins, the buffered clock (CP) and buffered Output Enable ($\overline{OE}$) are common to all flip-flops. The flip-flops will store the state of their individual D inputs that meet the setup and hold time requirements on the LOW-to-HIGH CP transition. With $\overline{OE}_1$, $\overline{OE}_2$ and $\overline{OE}_3$ LOW, the contents of the flip-flops are available at the outputs. When one of $\overline{OE}_1$, $\overline{OE}_2$ or $\overline{OE}_3$ is HIGH, the outputs go to the high impedance state.

Operation of the $\overline{OE}$ input does not affect the state of the flip-flops. The ACT825 has Clear ($\overline{CLR}$) and Clock Enable ($\overline{EN}$) pins. These pins are ideal for parity bus interfacing in high performance systems.

When $\overline{CLR}$ is LOW and $\overline{OE}$ is LOW, the outputs are LOW. When $\overline{CLR}$ is HIGH, data can be entered into the flip-flops. When $\overline{EN}$ is LOW, data on the inputs is transferred to the outputs on the LOW-to-HIGH clock transition. When $\overline{EN}$ is HIGH, the outputs do not change state, regardless of the data or clock input transitions.

## Function Table

| Inputs | | | | | Internal | Output | Function |
|---|---|---|---|---|---|---|---|
| $\overline{OE}$ | $\overline{CLR}$ | $\overline{EN}$ | CP | $D_n$ | Q | O | |
| H | X | L | ⟋ | L | L | Z | High-Z |
| H | X | L | ⟋ | H | H | Z | High-Z |
| H | L | X | X | X | L | Z | Clear |
| L | L | X | X | X | L | L | Clear |
| H | H | H | X | X | NC | Z | Hold |
| L | H | H | X | X | NC | NC | Hold |
| H | H | L | ⟋ | L | L | Z | Load |
| H | H | L | ⟋ | H | H | Z | Load |
| L | H | L | ⟋ | L | L | L | Load |
| L | H | L | ⟋ | H | H | H | Load |

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance
⟋ = LOW-to-HIGH Transition
NC = No Change

## Logic Diagram
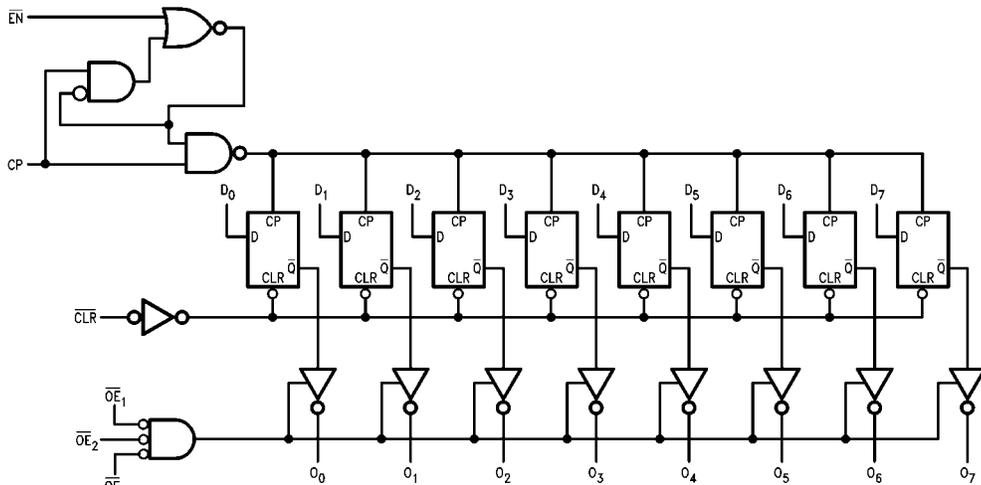


Please note that this diagram is provided only for the understanding of logic operations and should not be used to estimate propagation delays.

## Absolute Maximum Ratings(Note 1)

| | |
|---|---|
| Supply Voltage ($V_{CC}$) | −0.5V to 7.0V |
| DC Input Diode Current ($I_{IK}$) | |
| $V_I = -0.5V$ | −20 mA |
| $V_I = V_{CC} +0.5V$ | +20 mA |
| DC Input Voltage ($V_I$) | −0.5V to $V_{CC}$ +0.5V |
| DC Output Diode Current ($I_{OK}$) | |
| $V_O = -0.5V$ | −20 mA |
| $V_O = V_{CC} +0.5V$ | +20 mA |
| DC Output Voltage ($V_O$) | +0.5V |
| DC Output Source or Sink Current ($I_O$) | ± 50 mA |
| DC $V_{CC}$ or Ground Current | |
| Per Output Pin ($I_{CC}$ or $I_{GND}$) | ± 50 mA |
| Storage Temperature ($T_{STG}$) | −65°C to +150°C |
| Junction Temperature ($T_J$) | |
| PDIP | 140°C |

## Recommended Operating Conditions

| | |
|---|---|
| Supply Voltage ($V_{CC}$) | 4.5V to 5.5V |
| Input Voltage ($V_I$) | 0V to $V_{CC}$ |
| Output Voltage ($V_O$) | 0V to $V_{CC}$ |
| Operating Temperature ($T_A$) | −40°C to +85°C |
| Minimum Input Edge Rate (ΔV/Δt) | 125 mV/ns |
| $V_{IN}$ from 0.8V to 2.0V | |
| $V_{CC}$ @ 4.5V, 5.5V | |

**Note 1:** Absolute maximum ratings are those values beyond which damage to the device may occur. The databook specifications should be met, without exception, to ensure that the system design is reliable over its power supply, temperature, and output/input loading variables. Fairchild does not recommend operation of FACT™ circuits outside databook specifications.

## DC Electrical Characteristics

| Symbol | Parameter | $V_{CC}$ (V) | $T_A = 25°C$ Typ | $T_A = 25°C$ Guaranteed Limits | $T_A = -40°C$ to $+85°C$ | Units | Conditions |
|---|---|---|---|---|---|---|---|
| $V_{IH}$ | Minimum HIGH Level | 4.5 | 1.5 | 2.0 | 2.0 | V | $V_{OUT} = 0.1V$ |
| | Input Voltage | 5.5 | 1.5 | 2.0 | 2.0 | | or $V_{CC}$ −0.1V |
| $V_{IL}$ | Maximum LOW Level | 4.5 | 1.5 | 0.8 | 0.8 | V | $V_{OUT} = 0.1V$ |
| | Input Voltage | 5.5 | 1.5 | 0.8 | 0.8 | | or $V_{CC}$ −0.1V |
| $V_{OH}$ | Minimum HIGH Level | 4.5 | 4.49 | 4.4 | 4.4 | V | $I_{OUT} = -50$ μA |
| | Output Voltage | 5.5 | 5.49 | 5.4 | 5.4 | | |
| | | 4.5 | | 3.86 | 3.76 | V | $V_{IN} = V_{IL}$ or $V_{IH}$ $I_{OH} = -24$ mA |
| | | 5.5 | | 4.86 | 4.76 | | $I_{OH} = -24$ mA (Note 2) |
| $V_{OL}$ | Maximum LOW Level | 4.5 | 0.001 | 0.1 | 0.1 | V | $I_{OUT} = 50$ μA |
| | Output Voltage | 5.5 | 0.001 | 0.1 | 0.1 | | |
| | | 4.5 | | 0.36 | 0.44 | V | $V_{IN} = V_{IL}$ or $V_{IH}$ $I_{OL} = 24$ mA |
| | | 5.5 | | 0.36 | 0.44 | | $I_{OL} = 24$ mA (Note 2) |
| $I_{IN}$ | Maximum Input Leakage Current | 5.5 | | ± 0.1 | ± 1.0 | μA | $V_I = V_{CC}$, GND |
| $I_{OZ}$ | Maximum 3-STATE Current | 5.5 | | ±0.5 | ±5.0 | μA | $V_I = V_{IL}$, $V_{IH}$ $V_O = V_{CC}$, GND |
| $I_{CCT}$ | Maximum $I_{CC}$/Input | 5.5 | 0.6 | | 1.5 | mA | $V_I = V_{CC}$ −2.1V |
| $I_{OLD}$ | Minimum Dynamic | 5.5 | | | 75 | mA | $V_{OLD} = 1.65V$ Max |
| $I_{OHD}$ | Output Current (Note 3) | 5.5 | | | −75 | mA | $V_{OHD} = 3.85V$ Min |
| $I_{CC}$ | Maximum Quiescent Supply Current | 5.5 | | 8.0 | 80 | μA | $V_{IN} = V_{CC}$ or GND |

**Note 2:** All outputs loaded; thresholds on input associated with output under test.

**Note 3:** Maximum test duration 2.0 ms, one output loaded at a time.

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## AC Electrical Characteristics

| Symbol | Parameter | $V_{CC}$ (V) (Note 4) | $T_A = +25°C$ $C_L = 50$ pF Min | Typ | Max | $T_A = -40°C$ to $+85°C$ $C_L = 50$ pF Min | Max | Units |
|---|---|---|---|---|---|---|---|---|
| $f_{MAX}$ | Maximum Clock Frequency | 5.0 | 120 | 158 | | 109 | | MHz |
| $t_{PLH}$ | Propagation Delay CP to $O_n$ | 5.0 | 1.5 | 5.5 | 9.5 | 1.5 | 10.5 | ns |
| $t_{PHL}$ | Propagation Delay CP to $O_n$ | 5.0 | 2.0 | 5.5 | 9.5 | 1.5 | 10.5 | ns |
| $t_{PHL}$ | Propagation Delay $\overline{CLR}$ to $O_n$ | 5.0 | 2.5 | 8.0 | 13.5 | 2.0 | 15.5 | ns |
| $t_{PZH}$ | Output Enable Time $\overline{OE}$ to $O_n$ | 5.0 | 1.5 | 6.0 | 10.5 | 1.5 | 11.5 | ns |
| $t_{PZL}$ | Output Enable Time $\overline{OE}$ to $O_n$ | 5.0 | 2.0 | 6.5 | 11.0 | 1.5 | 12.0 | ns |
| $t_{PHZ}$ | Output Disable Time $\overline{OE}$ to $O_n$ | 5.0 | 1.5 | 6.5 | 11.0 | 1.5 | 12.0 | ns |
| $t_{PLZ}$ | Output Disable Time $\overline{OE}$ to $O_n$ | 5.0 | 1.5 | 6.0 | 10.5 | 1.5 | 11.5 | ns |

**Note 4:** Voltage Range 5.0 is 5.0V ± 0.5V

## AC Operating Requirements

| Symbol | Parameter | $V_{CC}$ (V) (Note 5) | $T_A = +25°C$ $C_L = 50$ pF Typ | $T_A = -40°C$ to $+85°C$ $C_L = 50$ pF Guaranteed Minimum | | Units |
|---|---|---|---|---|---|---|
| $t_S$ | Setup Time, HIGH or LOW $D_n$ to CP | 5.0 | 0.5 | 2.5 | 2.5 | ns |
| $t_H$ | Hold Time, HIGH or LOW $D_n$ to CP | 5.0 | 0 | 2.5 | 2.5 | ns |
| $t_S$ | Setup Time, HIGH or LOW $\overline{EN}$ to CP | 5.0 | 0 | 2.0 | 2.5 | ns |
| $t_H$ | Hold Time, HIGH or LOW $\overline{EN}$ to CP | 5.0 | 0 | 1.0 | 1.0 | ns |
| $t_W$ | CP Pulse Width HIGH or LOW | 5.0 | 2.5 | 4.5 | 5.5 | ns |
| $t_W$ | $\overline{CLR}$ Pulse Width, LOW | 5.0 | 3.0 | 5.5 | 5.5 | ns |
| $t_{REC}$ | $\overline{CLR}$ to CP Recovery Time | 5.0 | 1.5 | 3.5 | 4.0 | ns |

**Note 5:** Voltage Range 5.0 is 5.0V ± 0.5V

## Capacitance

| Symbol | Parameter | Typ | Units | Conditions |
|---|---|---|---|---|
| $C_{IN}$ | Input Capacitance | 4.5 | pF | $V_{CC}$ = OPEN |
| $C_{PD}$ | Power Dissipation Capacitance | 44 | pF | $V_{CC}$ = 5.0V |

## Physical Dimensions inches (millimeters) unless otherwise noted



**24-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300 Wide**
**Package Number M24B**

**74ACT825**

## Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

7.72

4.16

(1.78 TYP)

0.42 TYP

0.65 TYP

LAND PATTERN RECOMMENDATION

7.8 ± 0.1

-A-

24

13

6.4

4.4 ± 0.1

-B-

3.2

GAGE PLANE

0.25

SEATING PLANE

0°-8°

0.6 ± 0.1

DETAIL A
TYPICAL

1

12

⌒ 0.2 C B A
ALL LEAD TIPS

SEE DETAIL D

⌒ 0.1 C
ALL LEAD TIPS

(0.90)

1.1 MAX

-C-

0.65 TYP

0.10 ± 0.05 TYP

0.09-0.20 TYP

0.19 - 0.30 TYP

⊕ 0.13 (M) A B (S) C (S)

MTC24 (REV B)

**24-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide**
**Package Number MTC24**

74ACT825 8-Bit D-Type Flip-Flop

**Physical Dimensions** inches (millimeters) unless otherwise noted (Continued)



1.243 – 1.270
(31.57 – 32.26)
MAX

0.092
(2.337)
(2 PLS)

PIN NO. 1
IDENT

0.032
(0.813)
RAD
OPTION 2

OPTION 2

0.062
(1.575)
RAD

EJECTOR PINS
OPTIONAL

0.260 ± 0.005
(6.604 ± 0.127)

0.300 – 0.320
(7.62 – 8.128)

0.009 – 0.015
(0.229 – 0.381)

95° ± 5°

0.280
(7.112)
MIN

0.325 +0.040 −0.015
(8.255 +1.016 −0.381)

0.065
(1.651)

0.075 ± 0.015
(1.905 ± 0.381)

0.100 ± 0.010
(2.54 ± 0.254)
TYP

0.040
(1.016)
TYP

0.130 ± 0.005
(3.302 ± 0.127)

0.020
(0.508)
MIN

0.145 – 0.200
(3.683 – 5.080)

0.018 ± 0.003
(0.457 ± 0.076)
TYP

0.125 – 0.145
(3.175 – 3.556)
MIN

90° ± 4° TYP

N24C (REV F)

**24-Lead Plastic Dual-In-Line Package (PDIP), JEDEC MS-001, 0.300 Wide**
**Package Number N24C**

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