

Micropower 150 mA LDO Linear Regulators with DELAY, Adjustable RESET, and Monitor FLAG

The NCV8502 is a family of precision micropower voltage regulators. Their output current capability is 150 mA. The family has output voltage options for adjustable, 2.5 V, 3.3 V, 5.0 V, 8.0 V, and 10 V.

The output voltage is accurate within $\pm 2.0\%$ with a maximum dropout voltage of 0.6 V at 150 mA. Low quiescent current is a feature drawing only 90 μA with a 100 μA load. This part is ideal for any and all battery operated microprocessor equipment.

Microprocessor control logic includes an active $\overline{\text{RESET}}$ (with DELAY), and a FLAG monitor which can be used to provide an early warning signal to the microprocessor of a potential impending $\overline{\text{RESET}}$ signal. The use of the FLAG monitor allows the microprocessor to finish any signal processing before the $\overline{\text{RESET}}$ shuts the microprocessor down.

The active $\overline{\text{RESET}}$ circuit operates correctly at an output voltage as low as 1.0 V. The $\overline{\text{RESET}}$ function is activated during the power up sequence or during normal operation if the output voltage drops outside the regulation limits.

The reset threshold voltage can be decreased by the connection of external resistor divider to R_{ADJ} lead.

The regulator is protected against reverse battery, short circuit, and thermal overload conditions. The device can withstand load dump transients making it suitable for use in automotive environments. The device has also been optimized for EMC conditions.

Features

- Output Voltage Options: Adjustable, 2.5 V, 3.3 V, 5.0 V, 8.0 V, 10 V
- $\pm 2.0\%$ Output
- Low 90 μA Quiescent Current
- Fixed or Adjustable Output Voltage
- Active $\overline{\text{RESET}}$
- Adjustable Reset
- 150 mA Output Current Capability
- Fault Protection
 - ◆ +60 V Peak Transient Voltage
 - ◆ -15 V Reverse Voltage
 - ◆ Short Circuit
 - ◆ Thermal Overload
- Early Warning through $\overline{\text{FLAG/MON}}$ Leads
- NCV Prefix for Automotive and Other Applications Requiring Site and Change Control
- Pb-Free Packages are Available

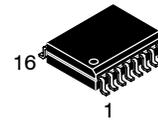


ON Semiconductor®

<http://onsemi.com>

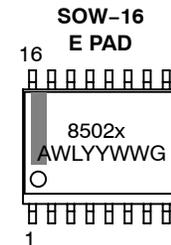
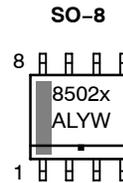


**SO-8
D SUFFIX
CASE 751**



**SOIC 16 LEAD
WIDE BODY
EXPOSED PAD
PDW SUFFIX
CASE 751AG**

MARKING DIAGRAMS



- x = Voltage Ratings as Indicated Below:
- A = Adjustable
 - 2 = 2.5 V
 - 3 = 3.3 V
 - 5 = 5.0 V
 - 8 = 8.0 V
 - 0 = 10 V
- A = Assembly Location
 WL, L = Wafer Lot
 YY, Y = Year
 WW, W = Work Week
 G or ■ = Pb-Free Device

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 12 of this data sheet.

NCV8502 Series

查询"NCV8502DADJG"供应商 PIN CONNECTIONS, ADJUSTABLE OUTPUT



PIN CONNECTIONS, FIXED OUTPUT

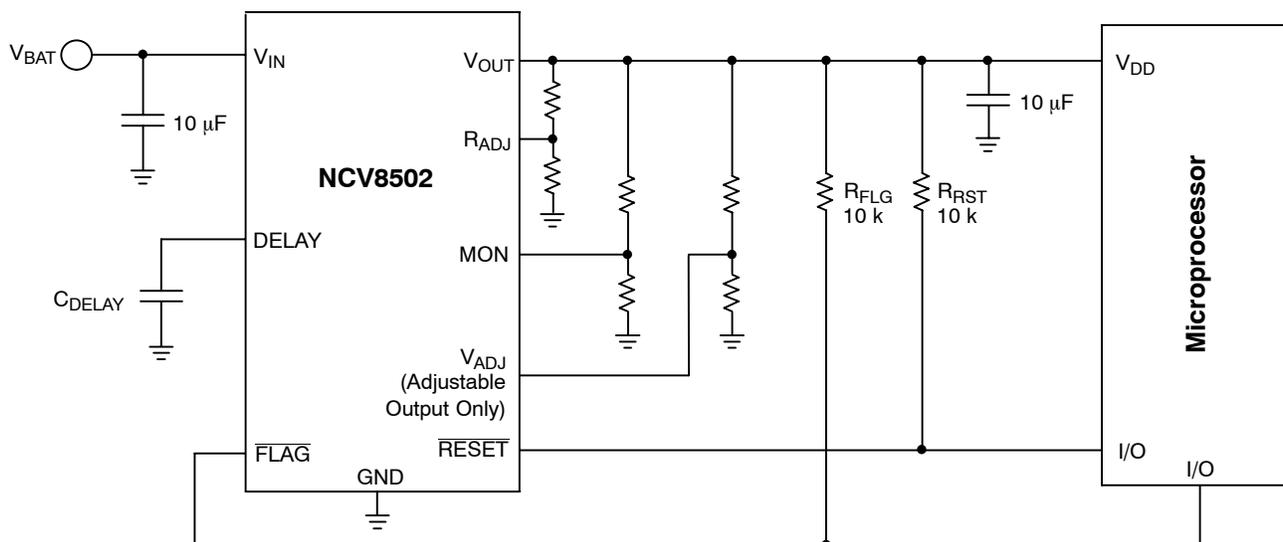


Figure 1. Application Diagram

MAXIMUM RATINGS*

Rating	Value	Unit
V_{IN} (dc)	-15 to 45	V
Peak Transient Voltage (46 V Load Dump @ $V_{IN} = 14\ \text{V}$)	60	V
Operating Voltage	45	V
V_{OUT} (dc)	-0.3 to 16	V
Voltage Range (RESET, FLAG)	-0.3 to 10	V

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

*During the voltage range which exceeds the maximum tested voltage of V_{IN} , operation is assured, but not specified. Wider limits may apply. Thermal dissipation must be observed closely.

NCV8502 Series

MAXIMUM RATINGS* (continued)

Rating	Value	Unit
Input Voltage Range (MON, V _{ADJ} , R _{ADJ})	-0.3 to 10	V
ESD Susceptibility (Human Body Model)	2.0	kV
Junction Temperature, T _J	-40 to +150	°C
Storage Temperature, T _S	-55 to 150	°C
Package Thermal Resistance, SO-8: Junction-to-Case, R _{θJC} Junction-to-Ambient, R _{θJA}	45 165	°C/W °C/W
Package Thermal Resistance, SOW-16 E PAD: Junction-to-Case, R _{θJC} Junction-to-Ambient, R _{θJA} Junction-to-Pin, R _{θJP} (Note 1)	15 56 35	°C/W °C/W °C/W
Lead Temperature Soldering: Reflow: (SMD styles only) (Note 2)	240 peak (Note 3)	°C

1. Measured to pin 16.
2. 60 second maximum above 183°C.
3. -5°C / +0°C allowable conditions.

*During the voltage range which exceeds the maximum tested voltage of V_{IN}, operation is assured, but not specified. Wider limits may apply. Thermal dissipation must be observed closely.

ELECTRICAL CHARACTERISTICS (I_{OUT} = 1.0 mA, -40°C ≤ T_J ≤ 150°C; V_{IN} = dependent on voltage option (Note 4); unless otherwise specified.)

Characteristic	Test Conditions	Min	Typ	Max	Unit
Output Stage					
Output Voltage for 2.5 V Option	6.5 V < V _{IN} < 16 V, 100 μA ≤ I _{OUT} ≤ 150 mA 5.5 V < V_{IN} < 26 V, 100 μA ≤ I_{OUT} ≤ 150 mA	2.450 2.425	2.5 2.5	2.550 2.575	V V
Output Voltage for 3.3 V Option	7.3 V < V _{IN} < 16 V, 100 μA ≤ I _{OUT} ≤ 150 mA 5.5 V < V_{IN} < 26 V, 100 μA ≤ I_{OUT} ≤ 150 mA	3.234 3.201	3.3 3.3	3.366 3.399	V V
Output Voltage for 5.0 V Option	9.0 V < V _{IN} < 16 V, 100 μA ≤ I _{OUT} ≤ 150 mA 6.0 V < V_{IN} < 26 V, 100 μA ≤ I_{OUT} ≤ 150 mA	4.90 4.85	5.0 5.0	5.10 5.15	V V
Output Voltage for 8.0 V Option	9.0 V < V_{IN} < 26 V, 100 μA ≤ I_{OUT} ≤ 150 mA	7.76	8.0	8.24	V
Output Voltage for 10 V Option	11 V < V_{IN} < 26 V, 100 μA ≤ I_{OUT} ≤ 150 mA	9.7	10	10.3	V V
Output Voltage for Adjustable Option	V _{OUT} = V _{ADJ} (Unity Gain) 6.5 V < V _{IN} < 16 V, 100 μA < I _{OUT} < 150 mA 5.5 V < V _{IN} < 26 V, 100 μA < I _{OUT} < 150 mA	1.254 1.242	1.280 1.280	1.306 1.318	V V
Dropout Voltage (V _{IN} - V _{OUT}) (5.0 V, 8.0 V, 10 V and Adj. > 5.0 V Options Only)	I _{OUT} = 150 mA I _{OUT} = 1.0 mA	- -	400 100	600 150	mV mV
Load Regulation	V _{IN} = 14 V, 5.0 mA ≤ I _{OUT} ≤ 150 mA	-30	5.0	30	mV
Line Regulation	[V _{OUT} (Typ) + 1.0] < V _{IN} < 26 V, I _{OUT} = 1.0 mA	-	15	60	mV
Quiescent Current, Low Load 2.5 V Option 3.3 V Option 5.0 V Option 8.0 V Option 10 V Option Adjustable Option	I _{OUT} = 100 μA, V _{IN} = 12 V, MON = V _{OUT}	- - - - - -	90 90 90 100 100 50	125 125 125 150 150 75	μA μA μA μA μA μA
Quiescent Current, Medium Load All Options	I _{OUT} = 75 mA, V _{IN} = 14 V, MON = V _{OUT}	-	4.0	6.0	mA
Quiescent Current, High Load All Options	I _{OUT} = 150 mA, V _{IN} = 14 V, MON = V _{OUT}	-	12	19	mA
Current Limit	-	151	300	-	mA

4. Voltage range specified in Output Stage of the Electrical Characteristics in boldface type.

NCV8502 Series

ELECTRICAL CHARACTERISTICS (continued) ($I_{OUT} = 1.0 \text{ mA}$; $-40^{\circ}\text{C} \leq T_J \leq 150^{\circ}\text{C}$; V_{IN} = dependent on voltage option (Note 5); unless otherwise specified)

Characteristic	Test Conditions	Min	Typ	Max	Unit
----------------	-----------------	-----	-----	-----	------

Output Stage

Short Circuit Output Current	$V_{OUT} = 0 \text{ V}$	40	190	–	mA
Thermal Shutdown	(Guaranteed by Design)	150	180	–	$^{\circ}\text{C}$

Reset Function (RESET)

RESET Threshold for 2.5 V Option HIGH (V_{RH}) LOW (V_{RL})	5.5 V \leq $V_{IN} \leq$ 26 V (Note 6) V_{OUT} Increasing V_{OUT} Decreasing	2.28	2.350	$0.98 \times V_{OUT}$	V
		2.25	2.300	$0.97 \times V_{OUT}$	V
RESET Threshold for 3.3 V Option HIGH (V_{RH}) LOW (V_{RL})	5.5 V \leq $V_{IN} \leq$ 26 V (Note 6) V_{OUT} Increasing V_{OUT} Decreasing	3.00	3.102	$0.98 \times V_{OUT}$	V
		2.97	3.036	$0.97 \times V_{OUT}$	V
RESET Threshold for 5.0 V Option HIGH (V_{RH}) LOW (V_{RL})	V_{OUT} Increasing V_{OUT} Decreasing	4.55	4.70	$0.98 \times V_{OUT}$	V
		4.50	4.60	$0.97 \times V_{OUT}$	V
RESET Threshold for 8.0 V Option HIGH (V_{RH}) LOW (V_{RL})	V_{OUT} Increasing V_{OUT} Decreasing	7.05	7.52	$0.98 \times V_{OUT}$	V
		7.00	7.36	$0.97 \times V_{OUT}$	V
RESET Threshold for 10 V Option HIGH (V_{RH}) LOW (V_{RL})	V_{OUT} Increasing V_{OUT} Decreasing	8.60	9.40	$0.98 \times V_{OUT}$	V
		8.50	9.20	$0.97 \times V_{OUT}$	V
Output Voltage Low (V_{RLO})	$1.0 \text{ V} \leq V_{OUT} \leq V_{RL}$, $R_{RESET} = 10 \text{ k}$	–	0.1	0.4	V
DELAY Switching Threshold (V_{DT})	–	1.4	1.8	2.2	V
DELAY Low Voltage	$V_{OUT} < \overline{\text{RESET}}$ Threshold Low(min)	–	–	0.1	V
DELAY Charge Current	DELAY = 1.0 V, $V_{OUT} > V_{RH}$	1.5	2.5	3.5	μA
DELAY Discharge Current	DELAY = 1.0 V, $V_{OUT} = 1.5 \text{ V}$	5.0	–	–	mA
Reset Adjust Switching Voltage ($V_{R(ADJ)}$)	–	1.23	1.31	1.39	V

FLAG/Monitor

Monitor Threshold	Increasing and Decreasing	1.10	1.20	1.31	V
Hysteresis	–	20	50	100	mV
Input Current	MON = 2.0 V	–0.5	0.1	0.5	μA
Output Saturation Voltage	MON = 0 V, $I_{FLAG} = 1.0 \text{ mA}$	–	0.1	0.4	V

Voltage Adjust (Adjustable Output only)

Input Current	$V_{ADJ} = 1.28 \text{ V}$	–0.5	–	0.5	μA
---------------	----------------------------	------	---	-----	---------------

5. Voltage range specified in Output Stage of the Electrical Characteristics in boldface type.

6. For $V_{IN} \leq 5.5 \text{ V}$, a RESET = Low may occur with the output in regulation.

NCV8502 Series

PACKAGE PIN DESCRIPTION, ADJUSTABLE OUTPUT

Package Pin Number		Pin Symbol	Function
SO-8	SOW-16 E PAD		
1	7	V_{IN}	Input Voltage.
2	8	MON	Monitor. Input for early warning comparator. If not needed connect to V_{OUT} .
3, 4	3-6, 9-12, 14, 15	NC	No connection.
5	13	GND	Ground. All GND leads must be connected to Ground.
6	16	\overline{FLAG}	Open collector output from early warning comparator.
7	1	V_{ADJ}	Voltage Adjust. A resistor divider from V_{OUT} to this lead sets the output voltage.
8	2	V_{OUT}	$\pm 2.0\%$, 150 mA output.

PACKAGE PIN DESCRIPTION, FIXED OUTPUT

Package Pin Number		Pin Symbol	Function
SO-8	SOW-16 E PAD		
1	7	V_{IN}	Input Voltage.
2	8	MON	Monitor. Input for early warning comparator. If not needed connect to V_{OUT} .
3	9	R_{ADJ}	Reset Adjust. If not needed connect to ground.
4	10	DELAY	Timing capacitor for \overline{RESET} function.
5	13	GND	Ground. All GND leads must be connected to Ground.
6	16	\overline{RESET}	Active reset (accurate to $V_{OUT} \geq 1.0$ V)
7	1	\overline{FLAG}	Open collector output from early warning comparator.
8	2	V_{OUT}	$\pm 2.0\%$, 150 mA output.
-	3-6, 11, 12, 14, 15	NC	No connection.

TYPICAL PERFORMANCE CHARACTERISTICS

[查询"NCV8502DADJG"供应商](#)

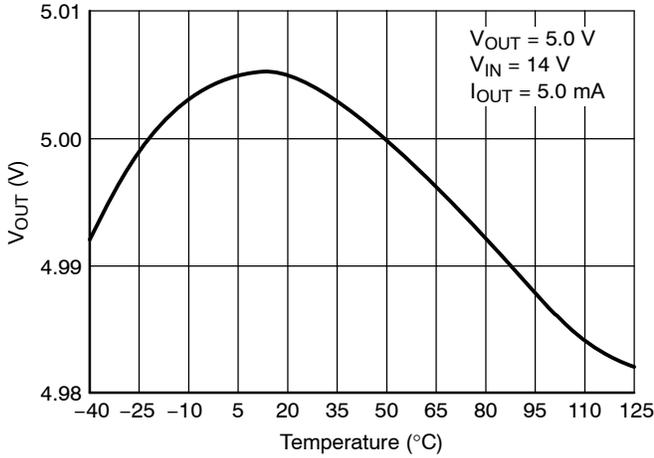


Figure 2. Output Voltage vs. Temperature

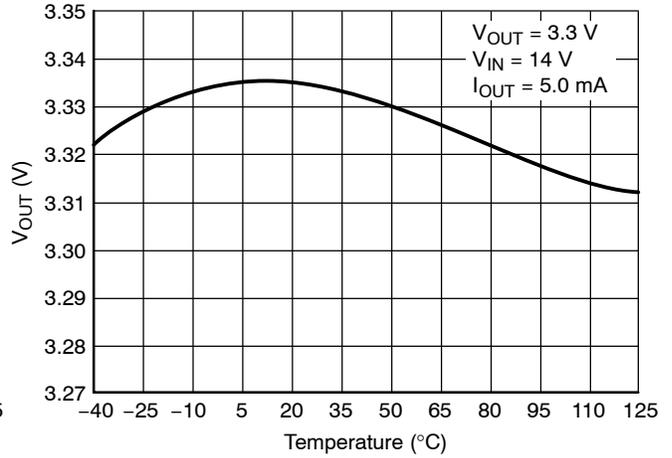


Figure 3. Output Voltage vs. Temperature

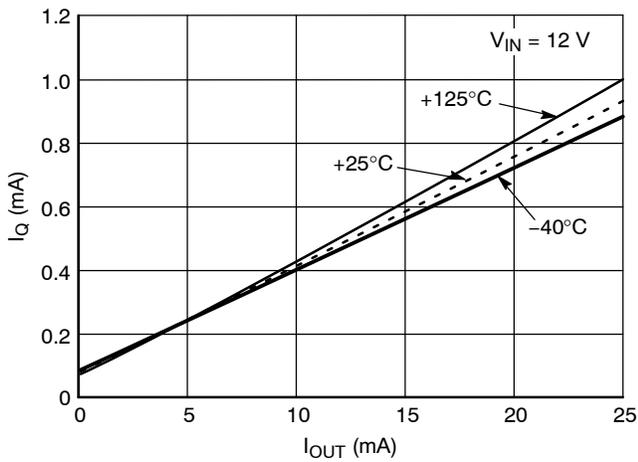


Figure 4. Quiescent Current vs. Output Current

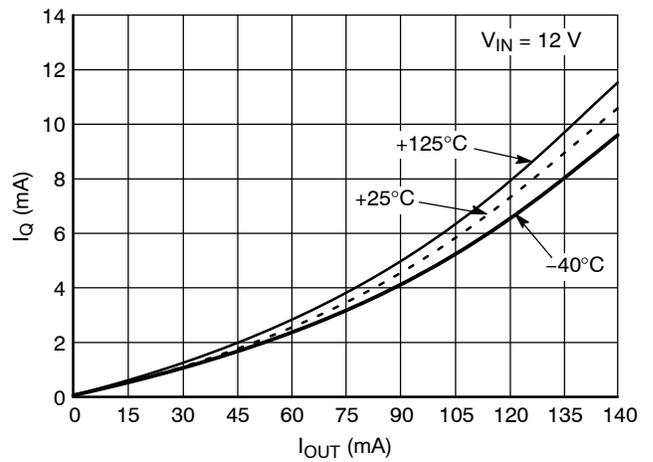


Figure 5. Quiescent Current vs. Output Current

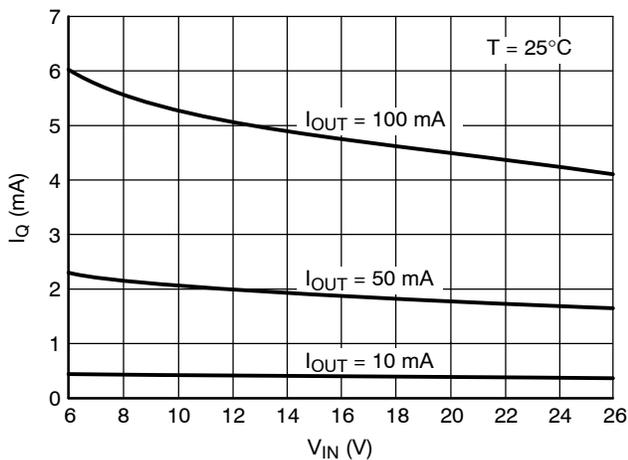


Figure 6. Quiescent Current vs. Input Voltage

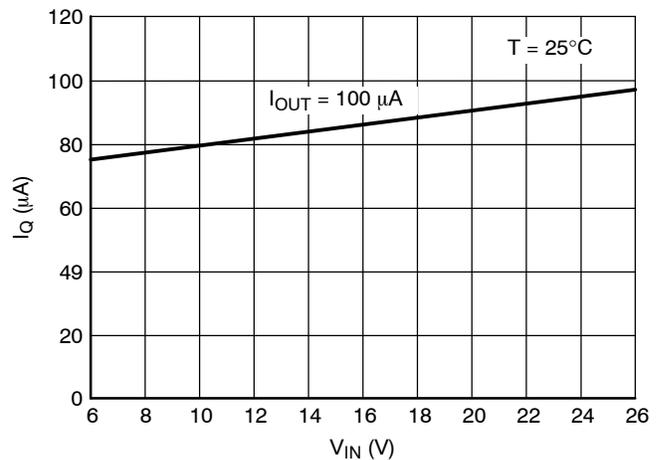


Figure 7. Quiescent Current vs. Input Voltage

TYPICAL PERFORMANCE CHARACTERISTICS

[查询"NCV8502DADJG"供应商](#)

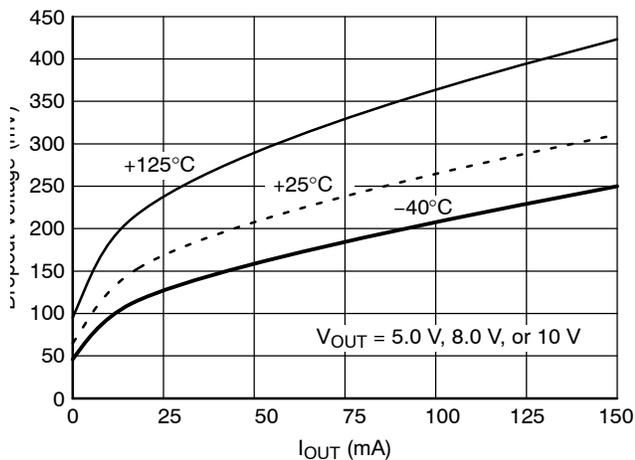


Figure 8. Dropout Voltage vs. Output Current

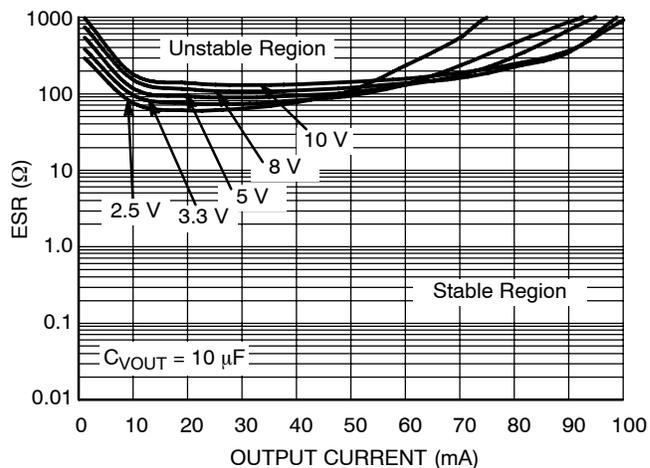


Figure 9. Output Stability with Output Voltage Change

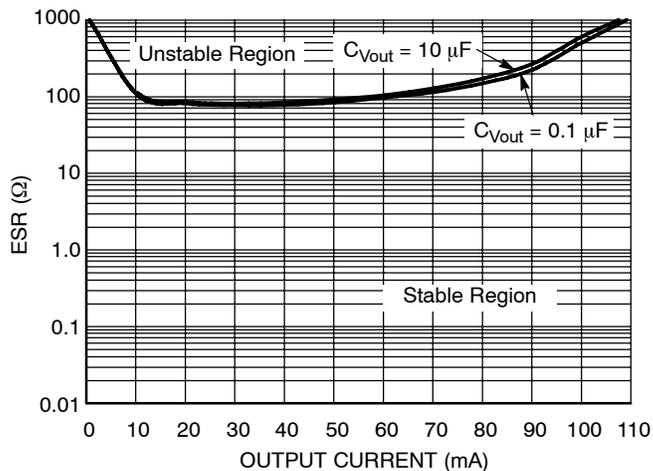


Figure 10. Output Stability with Output Capacitor Change

NCV8502 Series

[查询"NCV8502DADJG"供应商](#)

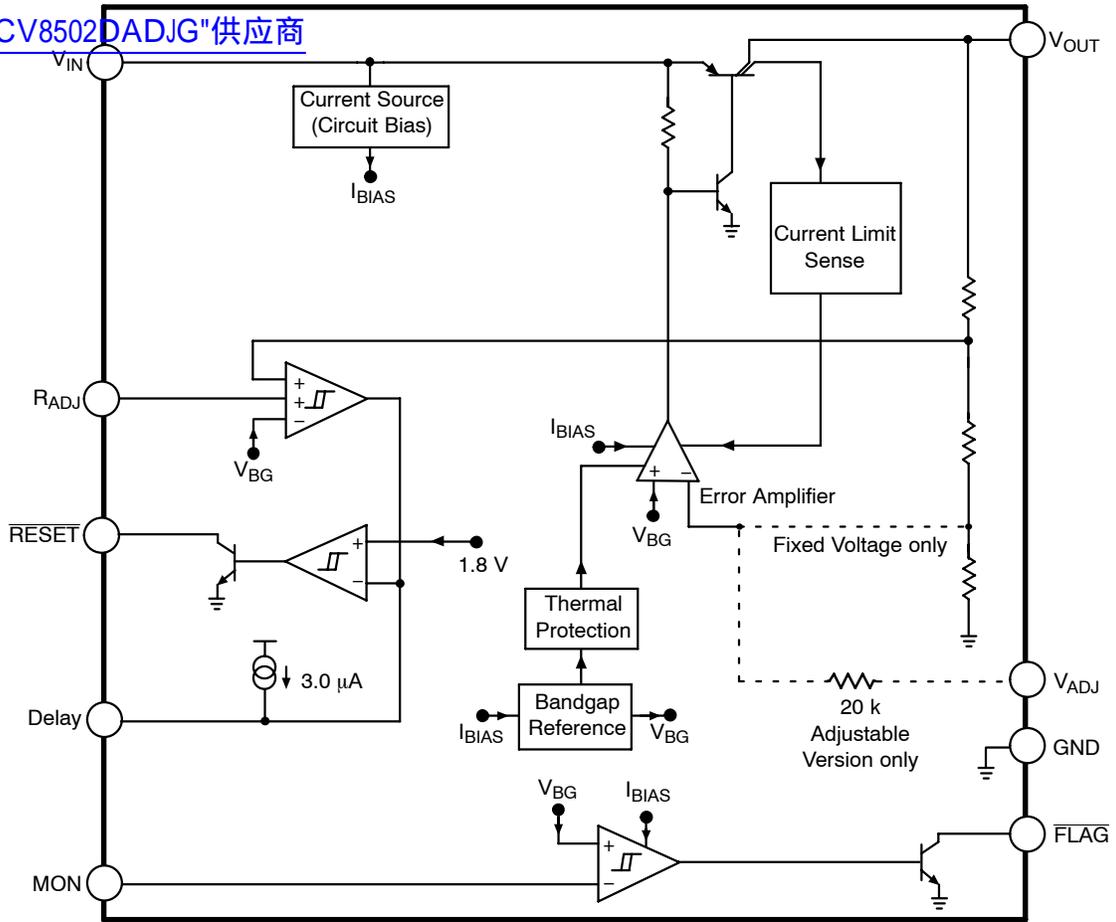


Figure 11. Block Diagram

CIRCUIT DESCRIPTION

[查询"NCV8502DADJG"供应商](#)

REGULATOR CONTROL FUNCTIONS

The NCV8502 contains the microprocessor compatible control function $\overline{\text{RESET}}$ (Figure 12).

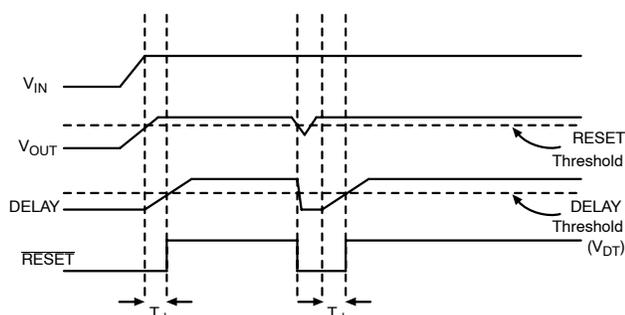


Figure 12. Reset and Delay Circuit Wave Forms

$\overline{\text{RESET}}$ Function

A $\overline{\text{RESET}}$ signal (low voltage) is generated as the IC powers up until V_{OUT} is within 6.0% of the regulated output voltage, or when V_{OUT} drops out of regulation, and is lower than 8.0% below the regulated output voltage. Hysteresis is included in the function to minimize oscillations.

The $\overline{\text{RESET}}$ output is an open collector NPN transistor, controlled by a low voltage detection circuit. The circuit is functionally independent of the rest of the IC thereby guaranteeing that the $\overline{\text{RESET}}$ signal is valid for V_{OUT} as low as 1.0 V.

Adjustable Reset Function

The reset threshold can be made lower by connecting an external resistor divider to the R_{ADJ} lead from the V_{OUT} lead, as displayed in Figure 13. This lead is grounded to select the default value of 4.6 V.

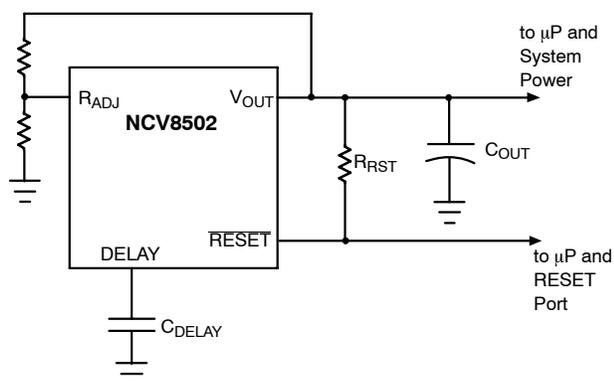


Figure 13. Adjustable $\overline{\text{RESET}}$

DELAY Function

The reset delay circuit provides a programmable (by external capacitor) delay on the $\overline{\text{RESET}}$ output lead.

The DELAY lead provides source current (typically 2.5 μA) to the external DELAY capacitor during the following proceedings:

1. During Power Up (once the regulation threshold has been verified).
2. After a reset event has occurred and the device is back in regulation. The DELAY capacitor is discharged when the regulation ($\overline{\text{RESET}}$ threshold) has been violated. This is a latched incident. The capacitor will fully discharge and wait for the device to regulate before going through the delay time event again.

FLAG/Monitor Function

An on-chip comparator is provided to perform an early warning to the microprocessor of a possible reset signal. The reset signal typically turns the microprocessor off instantaneously. This can cause unpredictable results with the microprocessor. The signal received from the $\overline{\text{FLAG}}$ pin will allow the microprocessor time to complete its present task before shutting down. This function is performed by a comparator referenced to the bandgap reference. The actual trip point can be programmed externally using a resistor divider to the input monitor (MON) (Figure 14). The typical threshold is 1.20 V on the MON pin.

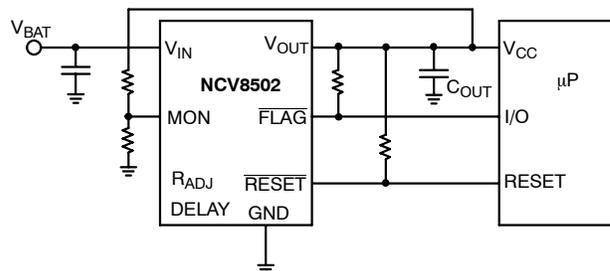


Figure 14. $\overline{\text{FLAG}}$ /Monitor Function

Voltage Adjust

Figure 15 shows the device setup for a user configurable output voltage. The feedback to the V_{ADJ} pin is taken from a voltage divider referenced to the output voltage. The loop is balanced around the Unity Gain threshold (1.28 V typical).

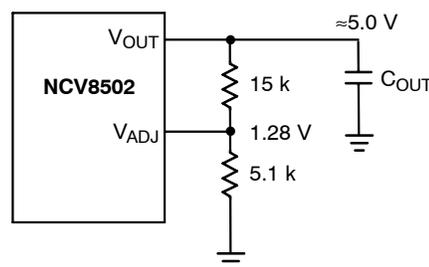


Figure 15. Adjustable Output Voltage

[查询"NCV8502DADJG"供应商](#)

APPLICATION NOTES

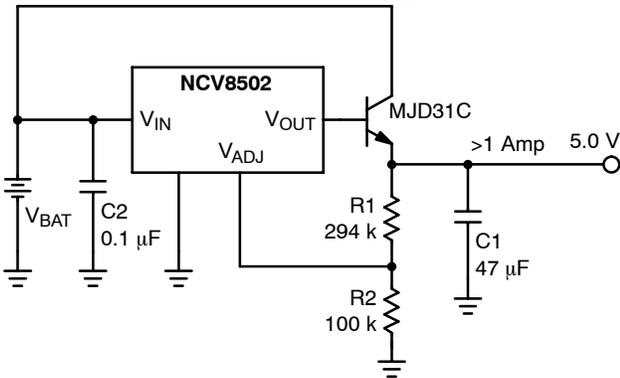


Figure 16. Additional Output Current

Adding Capability

Figure 16 shows how the adjustable version of parts can be used with an external pass transistor for additional current capability. The setup as shown will provide greater than 1 Amp of output current.

FLAG MONITOR

Figure 17 shows the FLAG Monitor waveforms as a result of the circuit depicted in Figure 14. As the output voltage falls (V_{OUT}), the Monitor threshold is crossed. This causes the voltage on the \overline{FLAG} output to go low sending a warning signal to the microprocessor that a \overline{RESET} signal may occur in a short period of time. $T_{WARNING}$ is the time the microprocessor has to complete the function it is currently working on and get ready for the \overline{RESET} shutdown signal.

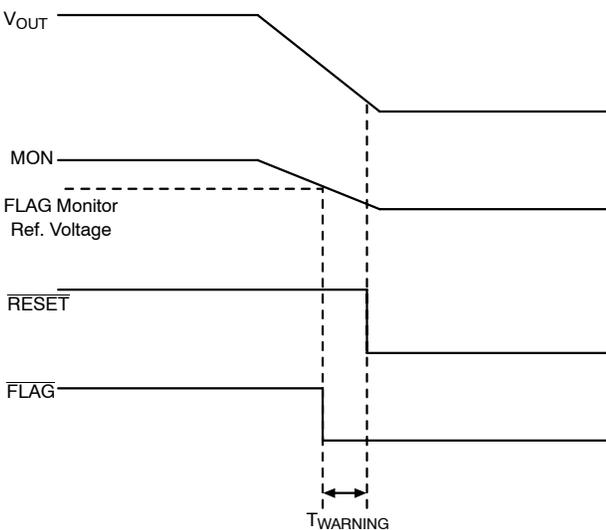
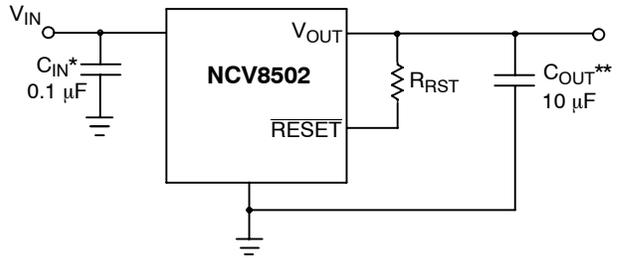


Figure 17. FLAG Monitor Circuit Waveform



* C_{IN} required if regulator is located far from the power supply filter
 ** C_{OUT} required for stability. Capacitor must operate at minimum temperature expected

Figure 18. Test and Application Circuit Showing Output Compensation

SETTING THE DELAY TIME

The delay time is controlled by the Reset Delay Low Voltage, Delay Switching Threshold, and the Delay Charge Current. The delay follows the equation:

$$t_{DELAY} = \frac{[C_{DELAY}(V_{dt} - \text{Reset Delay Low Voltage})]}{\text{Delay Charge Current}}$$

Example:

Using $C_{DELAY} = 33 \text{ nF}$.

Assume reset Delay Low Voltage = 0.

Use the typical value for $V_{dt} = 1.8 \text{ V}$.

Use the typical value for Delay Charge Current = $2.5 \mu\text{A}$.

$$t_{DELAY} = \frac{[33 \text{ nF}(1.8 - 0)]}{2.5 \mu\text{A}} = 23.8 \text{ ms}$$

STABILITY CONSIDERATIONS

The output or compensation capacitor helps determine three main characteristics of a linear regulator: start-up delay, load transient response and loop stability.

The capacitor value and type should be based on cost, availability, size and temperature constraints.

The value for the output capacitor C_{OUT} shown in Figure 18 should work for most applications, however it is not necessarily the optimized solution.

查询 NCV8502PADJG 供应商
CALCULATING POWER DISSIPATION IN A SINGLE OUTPUT LINEAR REGULATOR

The maximum power dissipation for a single output regulator (Figure 19) is:

$$P_{D(max)} = [V_{IN(max)} - V_{OUT(min)}]I_{OUT(max)} + V_{IN(max)}I_Q \quad (eq. 1)$$

where:

- $V_{IN(max)}$ is the maximum input voltage,
- $V_{OUT(min)}$ is the minimum output voltage,
- $I_{OUT(max)}$ is the maximum output current for the application, and
- I_Q is the quiescent current the regulator consumes at $I_{OUT(max)}$.

Once the value of $P_{D(max)}$ is known, the maximum permissible value of $R_{\theta JA}$ can be calculated:

$$R_{\theta JA} = \frac{150^{\circ}\text{C} - T_A}{P_D} \quad (eq. 2)$$

The value of $R_{\theta JA}$ can then be compared with those in the package section of the data sheet. Those packages with $R_{\theta JA}$'s less than the calculated value in equation 2 will keep the die temperature below 150°C .

In some cases, none of the packages will be sufficient to dissipate the heat generated by the IC, and an external heatsink will be required.

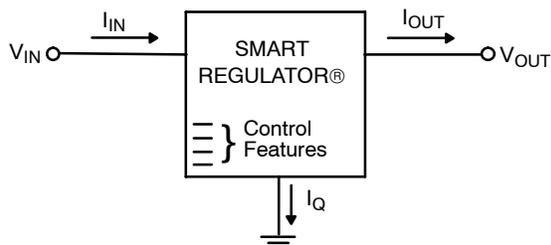


Figure 19. Single Output Regulator with Key Performance Parameters Labeled

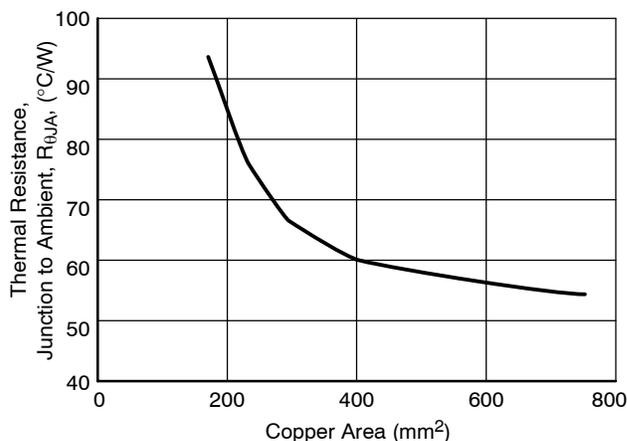


Figure 20. 16 Lead SOW (Exposed Pad), θ_{JA} as a Function of the Pad Copper Area (2 oz. Cu Thickness), Board Material = 0.0625" G-10/R-4

HEAT SINKS

A heat sink effectively increases the surface area of the package to improve the flow of heat away from the IC and into the surrounding air.

Each material in the heat flow path between the IC and the outside environment will have a thermal resistance. Like series electrical resistances, these resistances are summed to determine the value of $R_{\theta JA}$:

$$R_{\theta JA} = R_{\theta JC} + R_{\theta CS} + R_{\theta SA} \quad (eq. 3)$$

where:

- $R_{\theta JC}$ = the junction-to-case thermal resistance,
- $R_{\theta CS}$ = the case-to-heatsink thermal resistance, and
- $R_{\theta SA}$ = the heatsink-to-ambient thermal resistance.

$R_{\theta JC}$ appears in the package section of the data sheet. Like $R_{\theta JA}$, it too is a function of package type. $R_{\theta CS}$ and $R_{\theta SA}$ are functions of the package type, heatsink and the interface between them. These values appear in heat sink data sheets of heat sink manufacturers.

NCV8502 Series

ORDERING INFORMATION 供应商
[查询 NCV8502DADJG](#)

Device	Output Voltage	Package	Shipping†
NCV8502DADJ	Adjustable	SO-8	98 Units/Rail
NCV8502DADJG		SO-8 (Pb-Free)	98 Units/Rail
NCV8502DADJR2		SO-8	2500 Tape & Reel
NCV8502DADJR2G		SO-8 (Pb-Free)	2500 Tape & Reel
NCV8502PDWADJ		SOW-16 Exposed Pad	47 Units/Rail
NCV8502PDWADJG		SOW-16 Exposed Pad (Pb-Free)	47 Units/Rail
NCV8502PDWADJR2		SOW-16 Exposed Pad	1000 Tape & Reel
NCV8502PDWADJR2G		SOW-16 Exposed Pad (Pb-Free)	1000 Tape & Reel
NCV8502D25	2.5 V	SO-8	98 Units/Rail
NCV8502D25G		SO-8 (Pb-Free)	98 Units/Rail
NCV8502D25R2		SO-8	2500 Tape & Reel
NCV8502D25R2G		SO-8 (Pb-Free)	2500 Tape & Reel
NCV8502PDW25		SOW-16 Exposed Pad	47 Units/Rail
NCV8502PDW25G		SOW-16 Exposed Pad (Pb-Free)	47 Units/Rail
NCV8502PDW25R2		SOW-16 Exposed Pad	1000 Tape & Reel
NCV8502PDW25R2G		SOW-16 Exposed Pad (Pb-Free)	1000 Tape & Reel
NCV8502D33	3.3 V	SO-8	98 Units/Rail
NCV8502D33G		SO-8 (Pb-Free)	98 Units/Rail
NCV8502D33R2		SO-8	2500 Tape & Reel
NCV8502D33R2G		SO-8 (Pb-Free)	2500 Tape & Reel
NCV8502PDW33		SOW-16 Exposed Pad	47 Units/Rail
NCV8502PDW33G		SOW-16 Exposed Pad (Pb-Free)	47 Units/Rail
NCV8502PDW33R2		SOW-16 Exposed Pad	1000 Tape & Reel
NCV8502PDW33R2G		SOW-16 Exposed Pad (Pb-Free)	1000 Tape & Reel

†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

NCV8502 Series

ORDERING INFORMATION 供应商
[查询 NCV8502 供应商](#)

Device	Output Voltage	Package	Shipping†
NCV8502D50	5.0 V	SO-8	98 Units/Rail
NCV8502D50G		SO-8 (Pb-Free)	98 Units/Rail
NCV8502D50R2		SO-8	2500 Tape & Reel
NCV8502D50R2G		SO-8 (Pb-Free)	2500 Tape & Reel
NCV8502PDW50		SOW-16 Exposed Pad	47 Units/Rail
NCV8502PDW50G		SOW-16 Exposed Pad (Pb-Free)	47 Units/Rail
NCV8502PDW50R2		SOW-16 Exposed Pad	1000 Tape & Reel
NCV8502PDW50R2G		SOW-16 Exposed Pad (Pb-Free)	1000 Tape & Reel
NCV8502D80	8.0 V	SO-8	98 Units/Rail
NCV8502D80G		SO-8 (Pb-Free)	98 Units/Rail
NCV8502D80R2		SO-8	2500 Tape & Reel
NCV8502D80R2G		SO-8 (Pb-Free)	2500 Tape & Reel
NCV8502PDW80		SOW-16 Exposed Pad	47 Units/Rail
NCV8502PDW80G		SOW-16 Exposed Pad (Pb-Free)	47 Units/Rail
NCV8502PDW80R2		SOW-16 Exposed Pad	1000 Tape & Reel
NCV8502PDW80R2G		SOW-16 Exposed Pad (Pb-Free)	1000 Tape & Reel
NCV8502D100	10 V	SO-8	98 Units/Rail
NCV8502D100G		SO-8 (Pb-Free)	98 Units/Rail
NCV8502D100R2		SO-8	2500 Tape & Reel
NCV8502D100R2G		SO-8 (Pb-Free)	2500 Tape & Reel
NCV8502PDW100		SOW-16 Exposed Pad	47 Units/Rail
NCV8502PDW100G		SOW-16 Exposed Pad (Pb-Free)	47 Units/Rail
NCV8502PDW100R2		SOW-16 Exposed Pad	1000 Tape & Reel
NCV8502PDW100R2G		SOW-16 Exposed Pad (Pb-Free)	1000 Tape & Reel

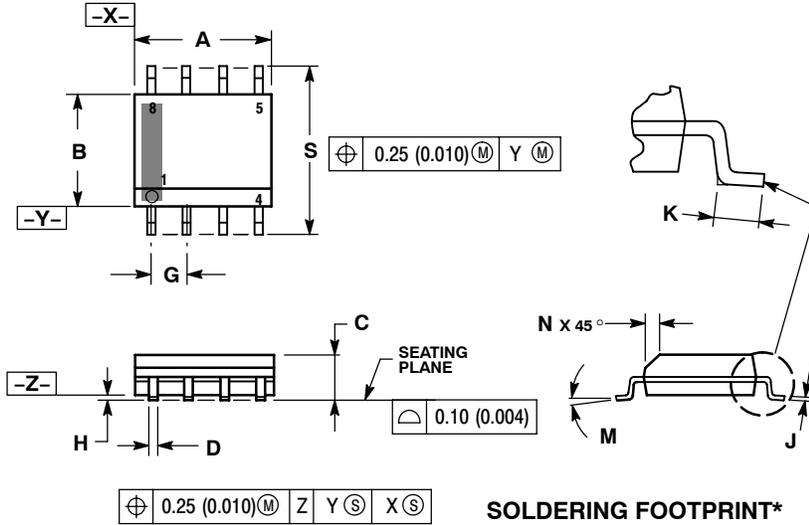
†For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specification Brochure, BRD8011/D.

NCV8502 Series

[查询"NCV8502DADJG"供应商](#)

PACKAGE DIMENSIONS

SOIC-8 NB
CASE 751-07
ISSUE AH

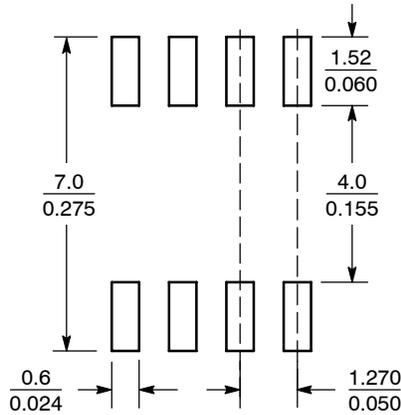


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751-01 THRU 751-06 ARE OBSOLETE. NEW STANDARD IS 751-07.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	4.80	5.00	0.189	0.197
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.053	0.069
D	0.33	0.51	0.013	0.020
G	1.27 BSC		0.050 BSC	
H	0.10	0.25	0.004	0.010
J	0.19	0.25	0.007	0.010
K	0.40	1.27	0.016	0.050
M	0°	8°	0°	8°
N	0.25	0.50	0.010	0.020
S	5.80	6.20	0.228	0.244

SOLDERING FOOTPRINT*



SCALE 6:1 (mm/inches)

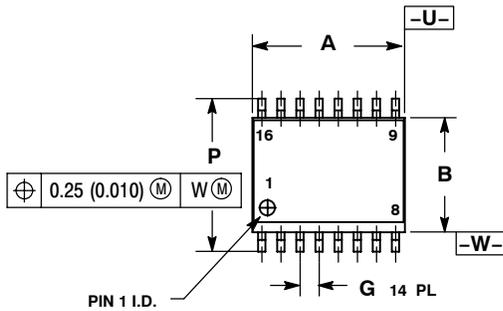
*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

NCV8502 Series

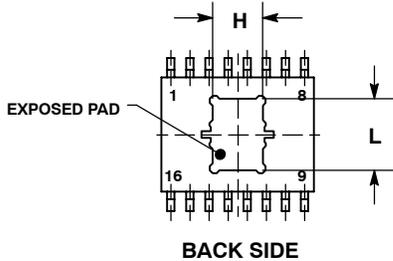
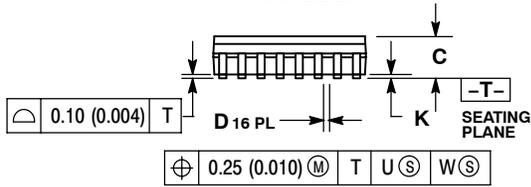
查询"NCV8502DADJG"供应商

PACKAGE DIMENSIONS

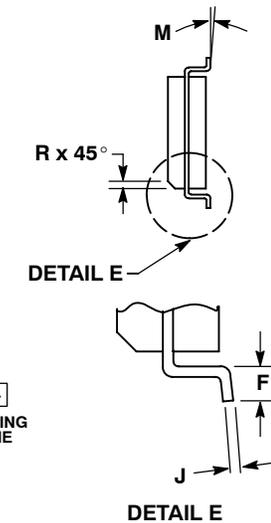
SOIC 16 LEAD WIDE BODY, EXPOSED PAD PDW SUFFIX CASE 751AG-01 ISSUE O



TOP SIDE



BACK SIDE

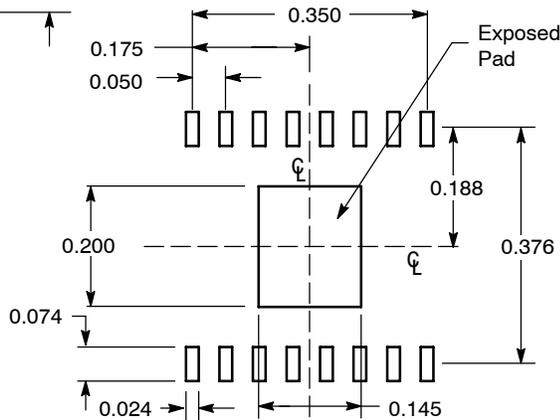


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSION A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE PROTRUSION SHALL BE 0.13 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.
6. 751R-01 OBSOLETE, NEW STANDARD 751R-02.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	10.15	10.45	0.400	0.411
B	7.40	7.60	0.292	0.299
C	2.35	2.65	0.093	0.104
D	0.35	0.49	0.014	0.019
F	0.50	0.90	0.020	0.035
G	1.27 BSC		0.050 BSC	
H	3.31	3.51	0.130	0.138
J	0.25	0.32	0.010	0.012
K	0.00	0.10	0.000	0.004
L	4.58	4.78	0.180	0.188
M	0°	7°	0°	7°
P	10.05	10.55	0.395	0.415
R	0.25	0.75	0.010	0.029

SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

SMART REGULATOR is a registered trademark of Semiconductor Components Industries, LLC.

ON Semiconductor and are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:
Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free USA/Canada
Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910
Japan Customer Focus Center
Phone: 81-3-5773-3850

ON Semiconductor Website: www.onsemi.com
Order Literature: <http://www.onsemi.com/orderlit>

For additional information, please contact your local Sales Representative