

3.3V Differential In 1:21 Differential Fanout Clock Driver with HCSL level Output

Description

The NB4N121K is a Clock differential input fanout distribution 1 to 21 HCSL level differential outputs, optimized for ultra low propagation delay variation. The NB4N121K is designed with HCSL clock distribution for FBDIMM applications in mind.

Inputs can accept differential LVPECL, CML, or LVDS levels. Single-ended LVPECL, CML, LVCMOS or LVTTL levels are accepted with the proper V_{REFAC} supply (see Figures 5, 10, 11, 12, and 13). Clock input pins incorporate an internal $50\ \Omega$ on die termination resistors.

Output drive current at I_{REF} (Pin 1) for 1X load is selected by connecting to GND. To drive a 2X load, connect I_{REF} to V_{CC} . See Figure 9.

The NB4N121K specifically guarantees low output-to-output skews. Optimal design, layout, and processing minimize skew within a device and from device to device. System designers can take advantage of the NB4N121K's performance to distribute low skew clocks across the backplane or the motherboard.

Features

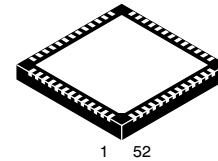
- Typical Input Clock Frequency 100, 133, 166, 200, 266, 333 and 400 MHz
- 340 ps Typical Rise and Fall Times
- 800 ps Typical Propagation Delay
- Δt_{pd} 100 ps Maximum Propagation Delay Variation Per Each Differential Pair
- <1 ps RMS Additive Clock jitter
- Operating Range: $V_{CC} = 3.0\text{ V}$ to 3.6 V with $V_{EE} = 0\text{ V}$
- Differential HCSL Output Level (700 mV Peak-to-Peak)
- Pb-Free Packages are Available*

*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.



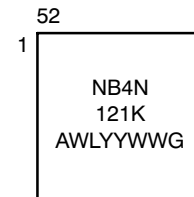
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**QFN-52
MN SUFFIX
CASE 485M**

MARKING DIAGRAM*



A = Assembly Site
 WL = Wafer Lot
 YY = Year
 WW = Work Week
 G = Pb-Free Package

*For additional marking information, refer to Application Note AND8002/D.

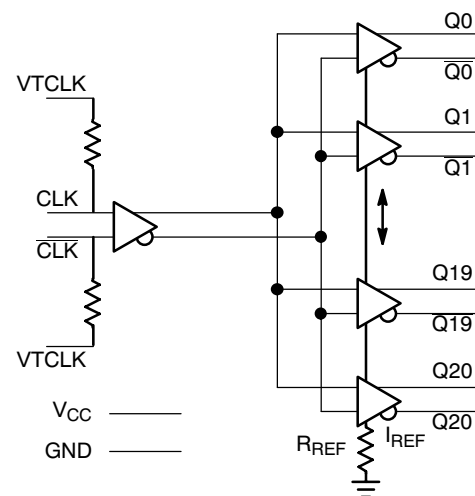


Figure 1. Pin Configuration (Top View)

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 9 of this data sheet.

NB4N121K

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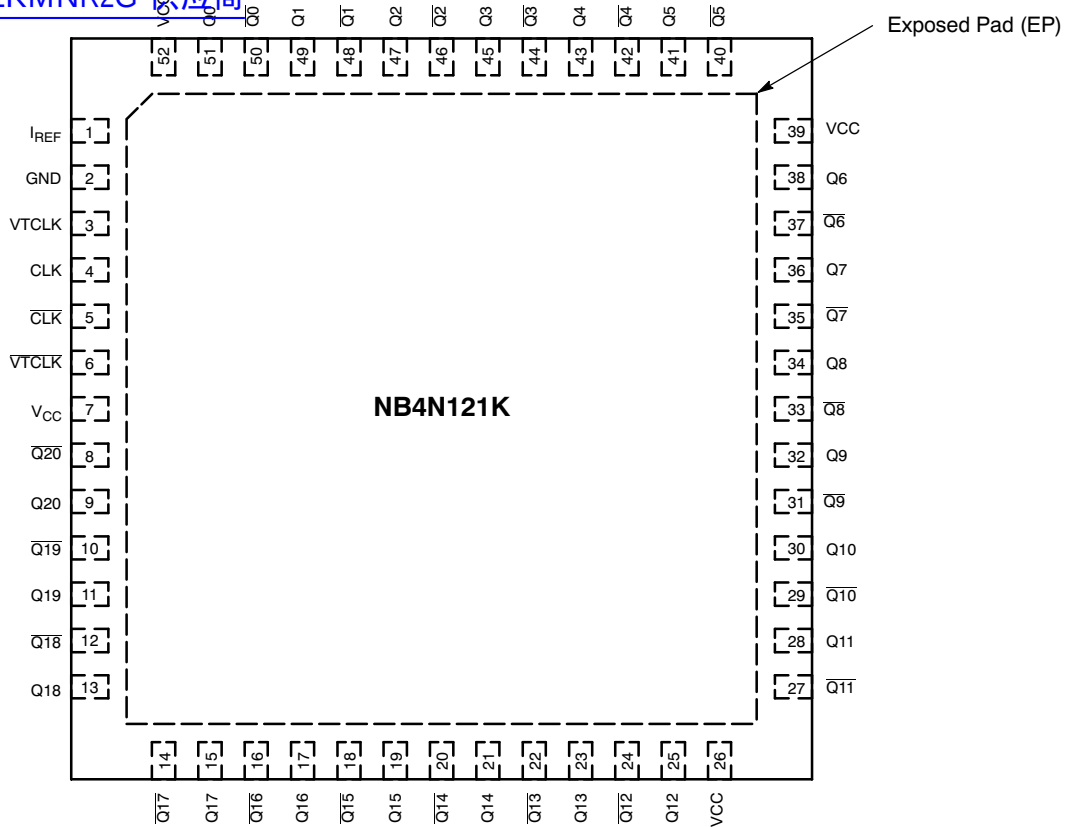


Figure 2. Pinout Configuration (Top View)

Table 1. PIN DESCRIPTION

Pin	Name	I/O	Description
1	I _{REF}	Output	Output current programming pin to select load drive. For 1X configuration, connect I _{REF} to GND, or for 2X configuration, connect I _{REF} to V _{CC} (See Figure 9).
2	GND	-	Supply Ground. GND pin must be externally connected to power supply to guarantee proper operation.
3, 6	VTCLK, VTCLK	-	Internal 50 Ω Termination Resistor connection Pins. In the differential configuration when the input termination pins are connected to the common termination voltage, and if no signal is applied then the device may be susceptible to self-oscillation.
4	CLK	LVPECL Input	CLOCK Input (TRUE)
5	CLK	LVPECL Input	CLOCK Input (INVERT)
7, 26, 39, 52	V _{CC}	-	Positive Supply pins. V _{CC} pins must be externally connected to a power supply to guarantee proper operation.
8, 10, 12, 14, 16, 18, 20, 22, 24, 27, 29, 31, 33, 35, 37, 40, 42, 44, 46, 48, 50	Q[20-0]	HCSL Output	Output (INVERT)
9, 11, 13, 15, 17, 19, 21, 23, 25, 28, 30, 32, 34, 36, 38, 41, 43, 45, 47, 49, 51	Q[20-0]	HCSL Output	Output (TRUE)
Exposed Pad	EP	GND	Exposed Pad. The thermally exposed pad (EP) on package bottom (see case drawing) must be attached to a sufficient heat-sinking conduit for proper thermal operation. (Note 1)

1. The exposed pad must be connected to the circuit board ground.

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Table 2. ATTRIBUTES

Characteristic	Value
Input Default State Resistors	None
ESD Protection Human Body Model	>2 kV
Moisture Sensitivity (Note 2) QFN-52	Level 3
Flammability Rating Oxygen Index: 28 to 34	UL 94 V-0 @ 0.125 in
Transistor Count	622
Meets or exceeds JEDEC Spec EIA/JESD78 IC Latchup Test	

2. For additional information, see Application Note AND8003/D.

Table 3. MAXIMUM RATINGS (Note 3)

Symbol	Parameter	Condition 1	Condition 2	Rating	Unit
V _{CC}	Positive Power Supply	GND = 0 V		6	V
V _I	Positive Input	GND = 0 V		GND - 0.3 ≤ V _I ≤ V _{CC}	V
V _{INPP}	Differential Input Voltage CLK - CLKb			1.2	V
I _{OUT}	Output Current	Continuous Surge		50 100	mA mA
T _A	Operating Temperature Range	QFN-52		-40 to +70	°C
T _{stg}	Storage Temperature Range			-65 to +150	°C
θ _{JA}	Thermal Resistance (Junction-to-Ambient) (Note 3)	0 lfpm 500 lfpm	QFN-52 QFN-52	25 19.6	°C/W °C/W
θ _{JC}	Thermal Resistance (Junction-to-Case)	2S2P (Note 4)	QFN-52	21	°C/W
T _{sol}	Wave Solder Pb-Free			265	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

3. JEDEC standard 51-6, multilayer board - 2S2P (2 signal, 2 power).

4. JEDEC standard multilayer board - 2S2P (2 signal, 2 power) with 8 filled thermal vias under exposed pad.

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Table 1. DC CHARACTERISTICS (V_{CC} = 3.0 V to 3.6 V, T_A = -40°C to +70°C Note 5)

Symbol	Characteristic	Min	Typ	Max	Unit
I _{GND}	GND Supply Current (All Outputs Loaded)	70	98	120	mA
I _{CC}	Power Supply Current (All Outputs Loaded) 1X 2X		420 780		mA
I _{IH}	Input HIGH Current CLKx, $\overline{\text{CLKx}}$		2.0	150	μA
I _{IL}	Input LOW Current CLKx, $\overline{\text{CLKx}}$	-150	-2.0		μA

DIFFERENTIAL INPUT DRIVEN SINGLE-ENDED (Figures 5 and 7)

V _{th}	Input Threshold Reference Voltage Range (Note 6)	1050		V _{CC} - 150	mV
V _{IH}	Single-Ended Input HIGH Voltage	V _{th} + 150		V _{CC}	mV
V _{IL}	Single-Ended Input LOW Voltage	GND		V _{th} - 150	mV

DIFFERENTIAL INPUTS DRIVEN DIFFERENTIALLY (Figures 6 and 8)

V _{IHD}	Differential Input HIGH Voltage	1200		V _{CC}	mV
V _{ILD}	Differential Input LOW Voltage	GND		V _{CC} - 75	mV
V _{ID}	Differential Input Voltage (V _{IHD} - V _{ILD})	75		2400	mV
V _{CMR}	Input Common Mode Range	1163		V _{CC} - 75	

HCSL OUTPUTS (Figure 4)

V _{OH}	Output HIGH Voltage	600	740	900	mV
V _{OL}	Output LOW Voltage	-150	0	150	mV

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lfpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

- Input parameters vary 1:1 with V_{CC}. Measurements taken with outputs in either 1X (all outputs loaded 50 Ω to GND) or 2X (all outputs loaded 25 Ω to GND) configuration, see Figure 9. For 1X configuration, connect I_{REF} to GND, or for 2X configuration, connect I_{REF} to V_{CC}.
- V_{th} is applied to the complementary input when operating in single ended mode.

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Table 5. AC CHARACTERISTICS

V_{CC} = 3.0 V to 3.6 V, GND = 0 V; -40°C to +70°C (Note 7)

Symbol	Characteristic	Min	Typ	Max	Unit
V _{OUTPP}	Output Voltage Amplitude (@ V _{INPPmin}) f _{in} = 133 MHz f _{in} = 166 MHz f _{in} = 200 MHz		725 725 725	900 900 900	mV
t _{PLH} , t _{PHL}	Propagation Delay to (See Figure 3) CLK/CLK̄ to Qx/Qx̄	550	800	950	ps
Δt _{PLH} , Δt _{PHL}	Propagation Delay Variations Variation Per Each Diff Pair CLK/CLK̄ to Qx/Qx̄ (Note 8) (See Figure 3)			100	ps
t _{SKEW}	Duty Cycle Skew (Note 9) Within-Device Skew, 1X Mode Only (Note 10) Within-Device Skew, 2X Mode (Note 10) Device-to-Device Skew (Note 10)			20 50 80 150	ps ps ps ps
t _{JITTER}	RMS Random Clock Jitter (Note 11) f _{in} = 133 MHz f _{in} = 166 MHz f _{in} = 200 MHz			1	ps
V _{INPP}	Input Voltage Swing/Sensitivity (Differential Configuration)	150		1200	mV
V _{cross}	Absolute Crossing Magnitude Voltage	250		550	mV
ΔV _{cross}	Variation in Magnitude of V _{cross}			150	mV
t _r , t _f	Absolute Magnitude in Output Risetime and Falltime (From 175 mV to 525 mV) Qx, Qx̄	175	340	700	ps
Δt _r , Δt _f	Variation in Magnitude of Risetime and Falltime (Single-Ended) (See Figure 4) Qx, Qx̄ 1X 2X			125 150	ps

NOTE: Device will meet the specifications after thermal equilibrium has been established when mounted in a test socket or printed circuit board with maintained transverse airflow greater than 500 lpm. Electrical parameters are guaranteed only over the declared operating temperature range. Functional operation of the device exceeding these conditions is not implied. Device specification limit values are applied individually under normal operating conditions and not valid simultaneously.

7. Measured by forcing V_{INPP} (MIN) from a 50% duty cycle clock source. Measurements taken with outputs in either 1X (all outputs loaded 50 Ω to GND) or 2X (all outputs loaded 25 Ω to GND) configuration, see Figure 9. For 1X configuration, connect I_{REF} to GND, or for 2X configuration, connect I_{REF} to V_{CC}. Typical gain is 20 dB.

8. Measured from the input pair crosspoint to each single output pair crosspoint across temp and voltage ranges.

9. Duty cycle skew is measured between differential outputs using the deviations of the sum of T_{pw-} and T_{pw+}.

10. Skew is measured between outputs under identical transition @ 133 MHz.

11. Additive RMS jitter with 50% duty cycle clock signal using phase noise integrated from 12 KHz to 33 MHz

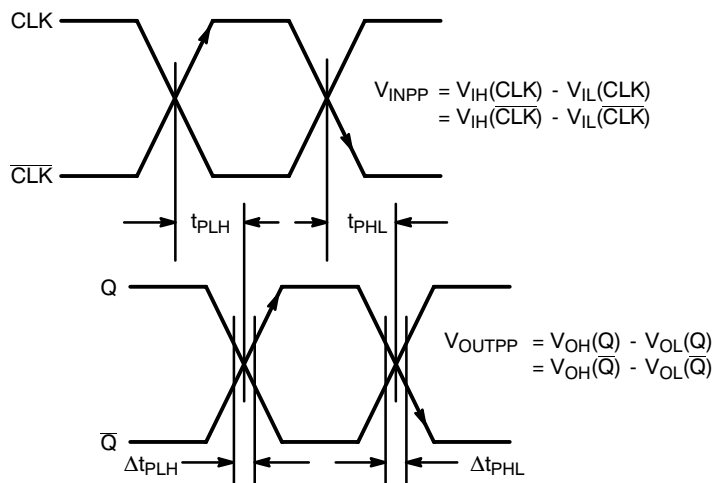


Figure 3. AC Reference Measurement

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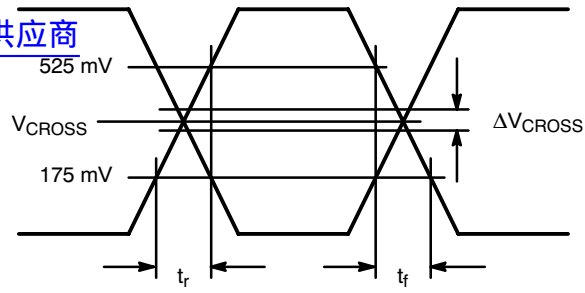


Figure 4. HCSL Output Parameter Characteristics

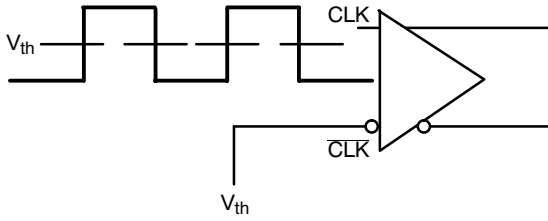


Figure 5. Differential Input Driven Single-Ended ($V_{th} = V_{REFAC}$)

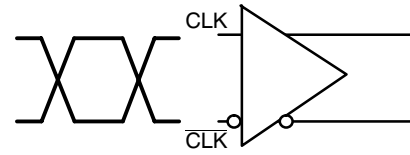


Figure 6. Differential Inputs Driven Differentially

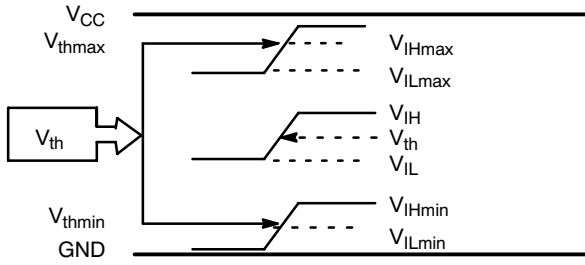


Figure 7. V_{th} Diagram

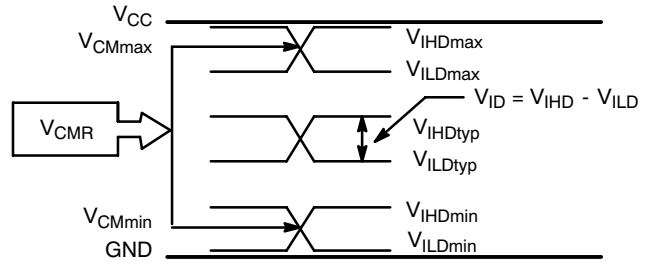


Figure 8. V_{CMR} Diagram

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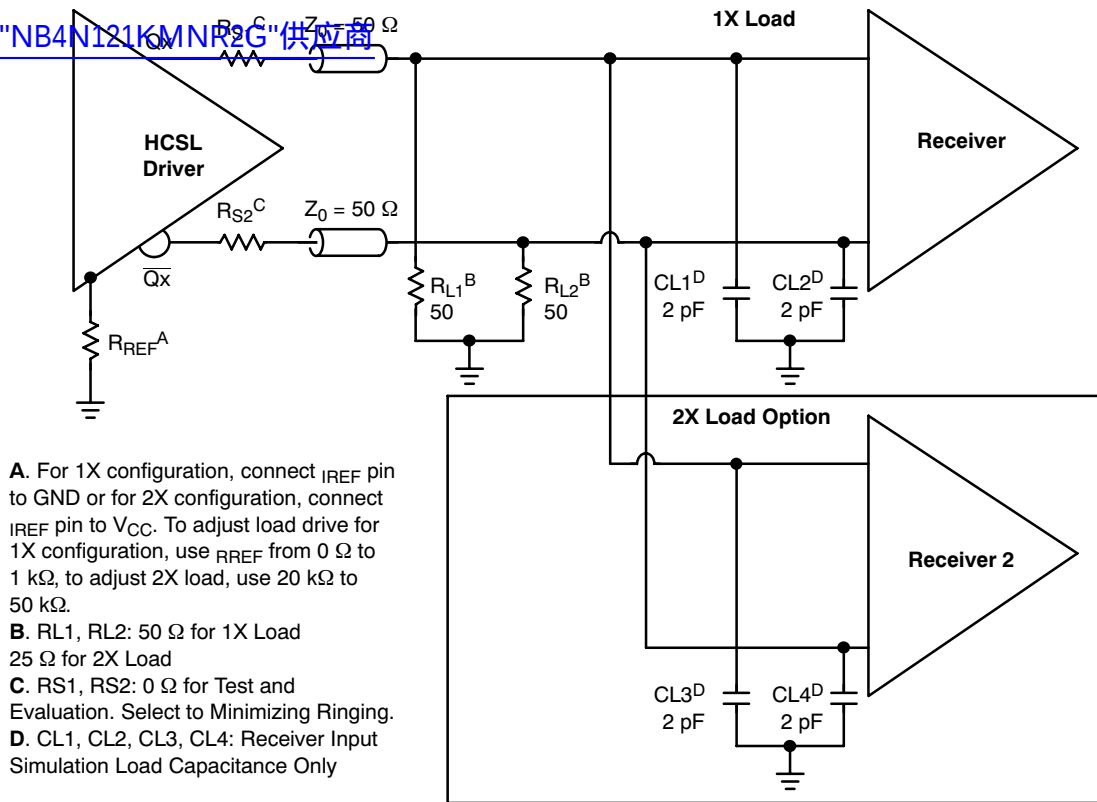
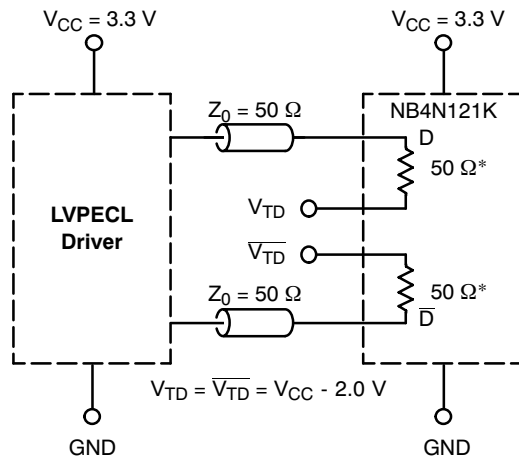
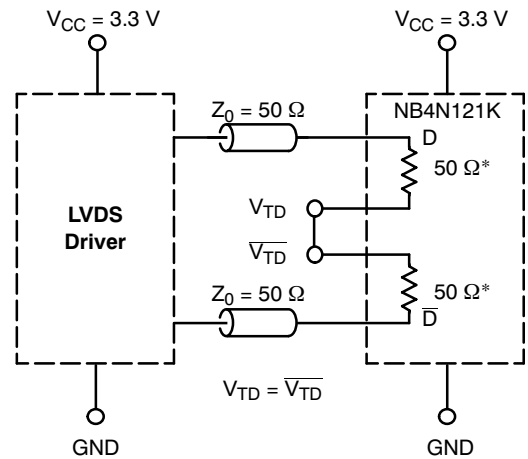


Figure 9. Typical Termination Configuration for Output Driver and Device Evaluation
C_{Lx} for Test Only (Representing Receiver Input Loading); Not Added to Application



*RTIN, Internal Input Termination Resistor

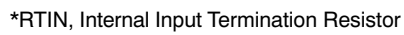
Figure 10. LVPECL Interface



*RTIN, Internal Input Termination Resistor

Figure 11. LVDS Interface

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LVCMOS/-LVTTL Driver

V_{CC}

GND

$Z_0 = 50 \Omega$

V_{TD}

$\overline{V_{TD}}$

$1.5 k\Omega^{**}$

GND

NB4N121K

D

$50 \Omega^*$

$\overline{D}$

$50 \Omega^*$

V_{CC}

GND

$V_{TD} = OPEN$

$\overline{D} = GND$

Figure 13. LVCMOS/LVTTL Interface



NB4N121K

[ORDERING INFORMATION](#) [查询NB4N121KMN2G"供应商"](#)

Device	Package	Shipping [†]
NB4N121KMN	QFN-52	260 Units / Tray
NB4N121KMNG	QFN-52 (Pb-Free)	260 Units / Tray
NB4N121KMNR2	QFN-52	2000 / Tape & Reel
NB4N121KMNR2G	QFN-52 (Pb-Free)	2000 / Tape & Reel

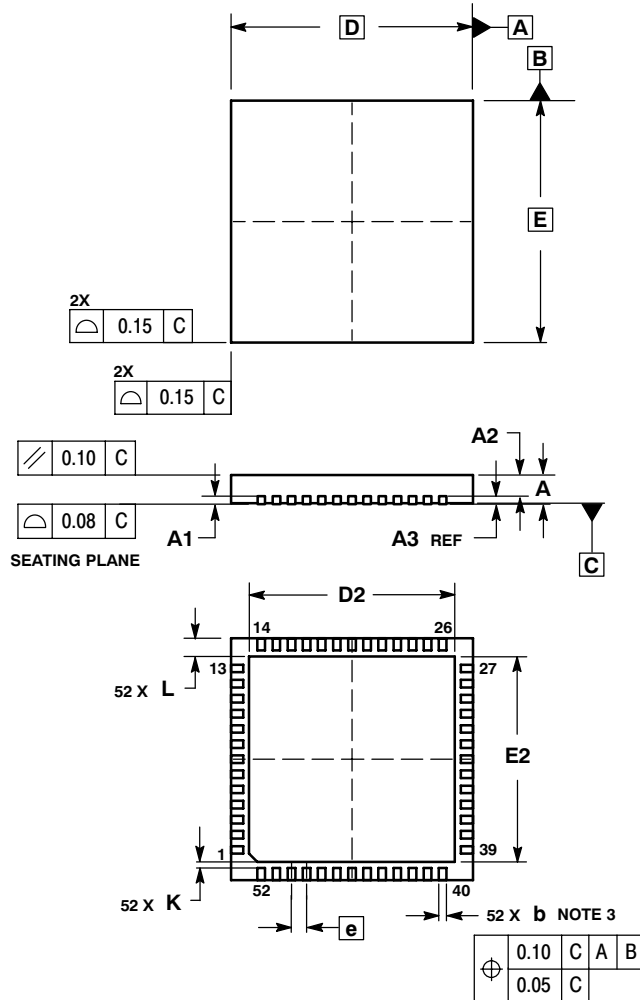
[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

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PACKAGE DIMENSIONS

52 PIN QFN 8x8
CASE 485M-01
ISSUE A



- NOTES:
1. DIMENSIONING AND TOLERANCING PER ASME Y14.5M, 1994.
 2. CONTROLLING DIMENSION: MILLIMETERS
 3. DIMENSION b APPLIES TO PLATED TERMINAL AND IS MEASURED BETWEEN 0.25 AND 0.30 MM FROM TERMINAL.
 4. COPLANARITY APPLIES TO THE EXPOSED PAD AS WELL AS THE TERMINALS.

DIM	MILLIMETERS	
	MIN	MAX
A	0.80	1.00
A1	0.00	0.05
A2	0.60	0.80
A3	0.20 REF	
b	0.18	0.30
D	8.00 BSC	
D2	6.50	6.80
E	8.00 BSC	
E2	6.50	6.80
e	0.50 BSC	
K	0.20	---
L	0.30	0.50

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