

N-Channel Synchronous MOSFETs with Break-Before-Make

FEATURES

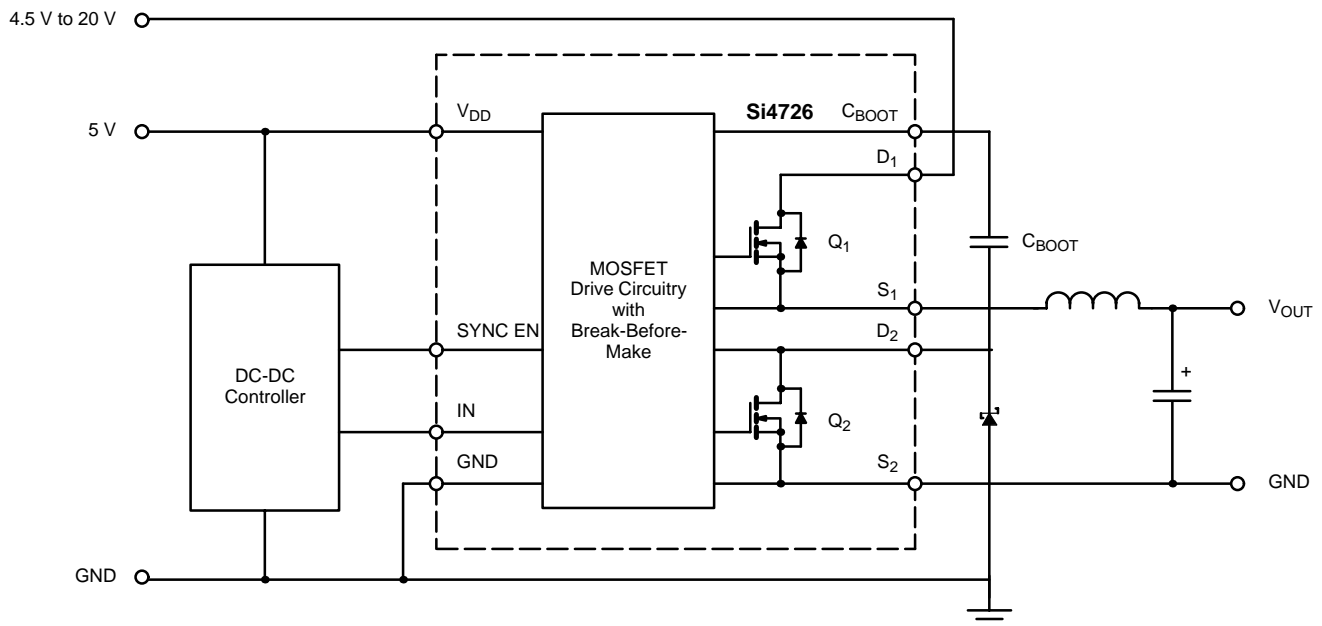
- 4.5- to 20-V Operation
- Driver Impedance— $3\ \Omega$
- Undervoltage Lockout
- Fast Switching Times (30 ns typ.)
- 20-V MOSFETs
- High Side: $0.0135\ \Omega$ @ $V_{DD} = 4.5\ \text{V}$
- Low Side: $0.0065\ \Omega$ @ $V_{DD} = 4.5\ \text{V}$
- Switching Frequency: 250 kHz to 1 MHz

DESCRIPTION

The Si4726CY n-channel synchronous MOSFET with break-before-make (BBM) is a high speed driver designed to operate in high frequency dc-dc switchmode power supplies. It's purpose is to simplify the use of n-channel MOSFETs in high frequency buck regulators. This device is design to be used with any single output PWM IC or ASIC to produce a

highly efficient low cost synchronous rectifier converter. A synchronous enable pin (disable = low, enable = high) controls the synchronous function for light load conditions. The Si4726CY is packaged in Vishay Siliconix's high performance LITTLE FOOT® SO-16 package.

FUNCTIONAL BLOCK DIAGRAM



ABSOLUTE MAXIMUM RATINGS (T _A = 25°C UNLESS OTHERWISE NOTED)				
Parameter	Symbol	Steady State	Unit	
Logic Supply	V _{DD}	7	V	
Logic Inputs	V _{IN}	-0.7 to V _{DD} + 0.3		
Drain-Source Voltage	V _{DS}	-1.0 to 20		
Bootstrap Voltage	V _{BOOT}	7		
Synchronous Pin Voltage	V _{SYNC}	-0.7 to V _{DD} + 0.3		
Maximum Power Dissipation ^a	P _D	4	W	
Operating Junction and Storage Temperature Range	Driver	T _J , T _{stg}	-65 to 125	°C
	MOSFETs		-65 to 150	

Notes

- a. Surface mounted on 1" x 1" FR4 board, full copper two sides.
 b. Pulse test: pulse width ≤ 300 μs, duty cycle ≤ 2%.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS			
Parameter	Symbol	Steady State	Unit
Drain Voltage	V _{D1}	4.5 to 20	V
Logic Supply	V _{DD}	4.5 to 5.5	
Input Logic High Voltage	V _{IH}	0.7 × V _{DD} to V _{DD}	
Input Logic Low Voltage	V _{IL}	-0.3 to 0.3 × V _{DD}	
Bootstrap Capacitor	C _{BOOT}	100 n to 1 μ	F
Ambient Temperature	T _A	-40 to 85	°C

THERMAL RESISTANCE RATINGS					
Parameter	Symbol	Typical	Maximum	Unit	
Highside Junction-to-Ambient ^a	Steady State	R _{thJA1}	85	105	°C/W
Lowside Junction-to-Ambient ^a		R _{thJA2}	68	85	
Highside Junction-to-Foot (Drain) ^b		R _{thJF1}	24	30	
Lowside Junction-to-Foot (Drain) ^b		R _{thJF2}	16	20	

Notes

- a. Surface Mounted on 1" x 1" FR4 Board.
 b. Junction-to-foot thermal impedance represents the effective thermal impedance of all heat carrying leads in parallel and is intended for use in conjunction with the thermal impedance of the PC board pads to ambient (R_{thJA} = R_{thJF} + R_{thPCB-A}). It can also be used to estimate chip temperature if power dissipation and the lead temperature of a heat carrying (drain) lead is known.



SPECIFICATIONS								
Parameter	Symbol	Test Conditions Unless Specified $T_J = 25^\circ\text{C}$ $4.5\text{ V} < V_{DD} < 5.5\text{ V}, 4.5\text{ V} < V_{D1} < 20\text{ V}$	Limits			Unit		
			Min	Typ	Max			
Power Supplies								
Logic Voltage	V_{DD}		4.5		5.5	V		
Logic Current	$I_{DD(EN)}$	$V_{DD} = 4.5\text{ V}, V_{IN} = 4.5\text{ V}$		280	500	μA		
	$I_{DD(DIS)}$	$V_{DD} = 4.5\text{ V}, V_{IN} = 0\text{ V}$		220	500			
Logic Input								
Logic Input Voltage (V_{IN})	High	V_{IH}	$V_{DD} = 4.5\text{ V}$	3.15	2.3	V		
	Low	V_{IL}		-0.3	2.25		0.8	
Protection								
Break-Before-Make Reference	V_{BBM}	$V_{DD} = 5.5\text{ V}$		2.4		V		
Undervoltage Lockout	V_{UVLO}	$\text{SYNC} = 4.5\text{ V}$	3.75	4	4.25			
Undervoltage Lockout Hysteresis	V_H			0.4				
MOSFET Drivers								
Driver Impedance	R_{DR1}	$V_{DD} = 4.5\text{ V}$	Driver 1		3.6	Ω		
	R_{DR2}		Driver 2		2			
MOSFETs								
Drain-Source Voltage	V_{DS}	$I_D = 250\ \mu\text{A}$		20		V		
Drain-Source On-State Resistance ^a	$r_{DS(on)1}$	$V_{DD} = 4.5\text{ V}, I_D = 10\text{ A}$ $T_J = 25^\circ\text{C}$	Q1		11	13.5	$\text{m}\Omega$	
	$r_{DS(on)2}$		Q2		4.6	6.5		
Diode Forward Voltage ^a	V_{SD1}	$I_S = 2\text{ A}, V_{GS} = 0\text{ V}$	Q1		0.7	1.1	V	
	V_{SD2}		Q2		0.7	1.1		
Dynamic^b (Unless Specified—$F_s = 250\text{ kHz}$, $\text{dc} = 10\%$. $V_{DD} = 5\text{ V}$, $I = 10\text{ A}$, Refer to Switching Test Setup)								
Rise Time	t_{rd1}	10% - 90%	Driver 1		35	60	ns	
	t_{rd2}		Driver 2		22	40		
Fall Time	t_{fd1}	90% - 10%	Driver 1		10	20		
	t_{fd2}		Driver 2		17.5	40		
Turn-Off Delay	$t_{d(off)1}$	See Timing Diagram	V_{IN} to G_1		63	130		
	$t_{d(off)2}$		V_{IN} to G_2		30	60		
Δt	Δt_{1-2}		G_1 to G_2		17.5	40		
	Δt_{2-1}		G_2 to G_1		38	80		
Rise Time	t_r		10% - 90%	S_1/D_2		35		60
Fall Time	t_f		90% - 10%	S_1/D_2		10		20
Source-Drain Reverse Recovery Time— Q_2	t_{fr2}	$I_F = 2.7\text{ A}, di/dt = 100\text{ A}/\mu\text{s}$			50	80		

Notes

- a. Pulse test: pulse width $\leq 300\ \mu\text{s}$; duty cycle $\leq 2\%$.
- b. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.

DETAILED BLOCK DIAGRAM

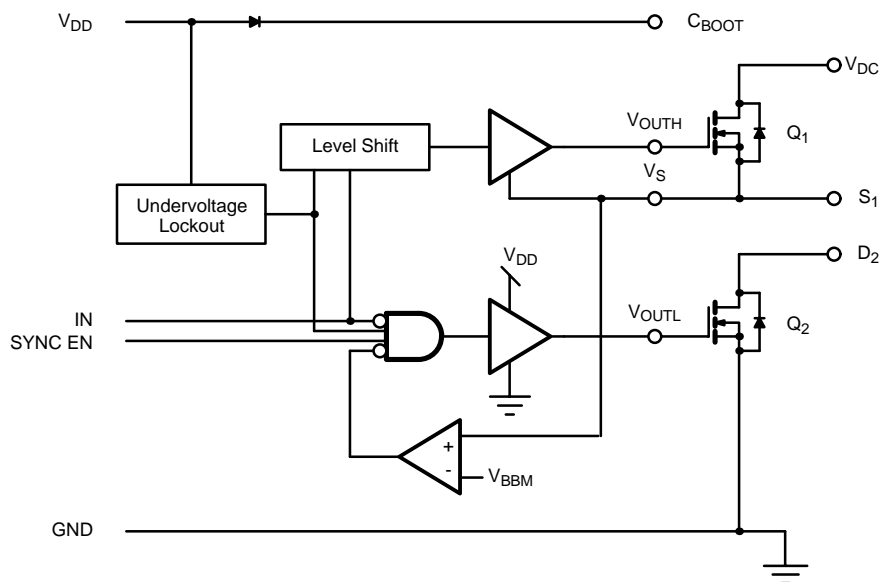
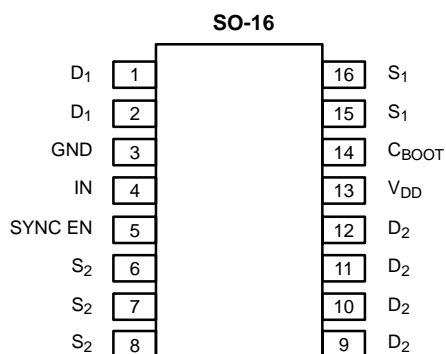


FIGURE 1.

PIN CONFIGURATION



Top View

Order Number: **Si4726CY**

TRUTH TABLE

Sync EN	V _{IN}	Q ₁	Q ₂
H	H	ON	OFF
H	L	OFF	ON
L	H	ON	OFF
L	L	OFF	OFF

PIN DESCRIPTION

Pin Number	Symbol	Description
1, 2	D ₁	Highside MOSFET Drain
3	GND	Ground
4	IN	Input Logic Signal
5	SYNC EN	Synchronous Enable
6, 7, 8	S ₂	Lowside MOSFET Source
9, 10, 11, 12	D ₂	Lowside MOSFET Drain
13	V _{DD}	Logic Supply
14	C _{BOOT}	Bootstrap Capacitor For Upper MOSFET
15, 16	S ₁	Highside MOSFET Source

TIMING DIAGRAM

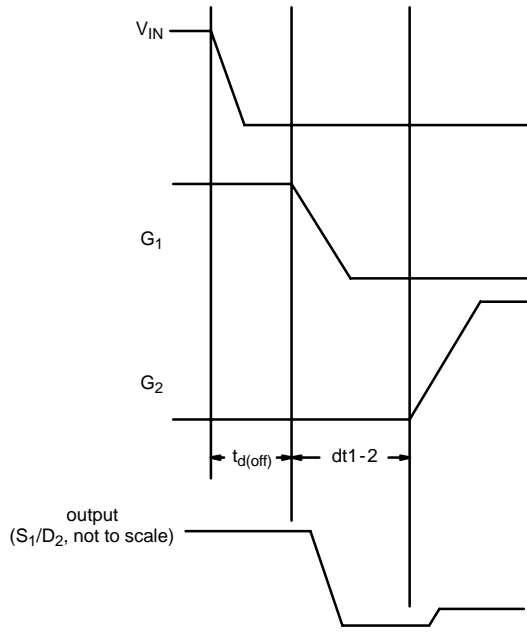


FIGURE 5. Δt_{1-2}

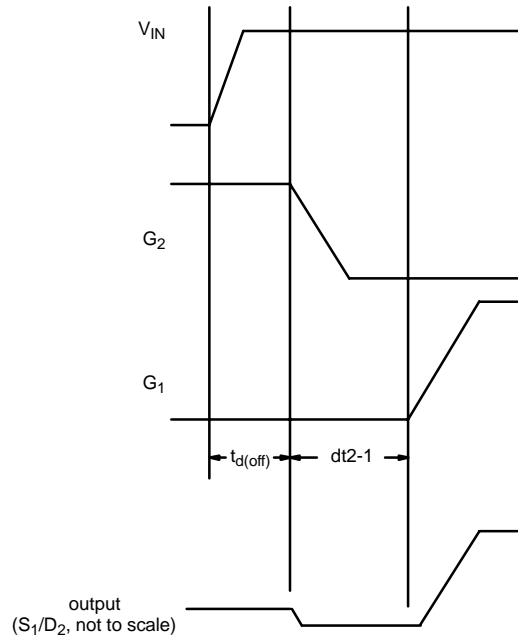


FIGURE 6. Δt_{2-1}

SWITCHING TEST SETUP

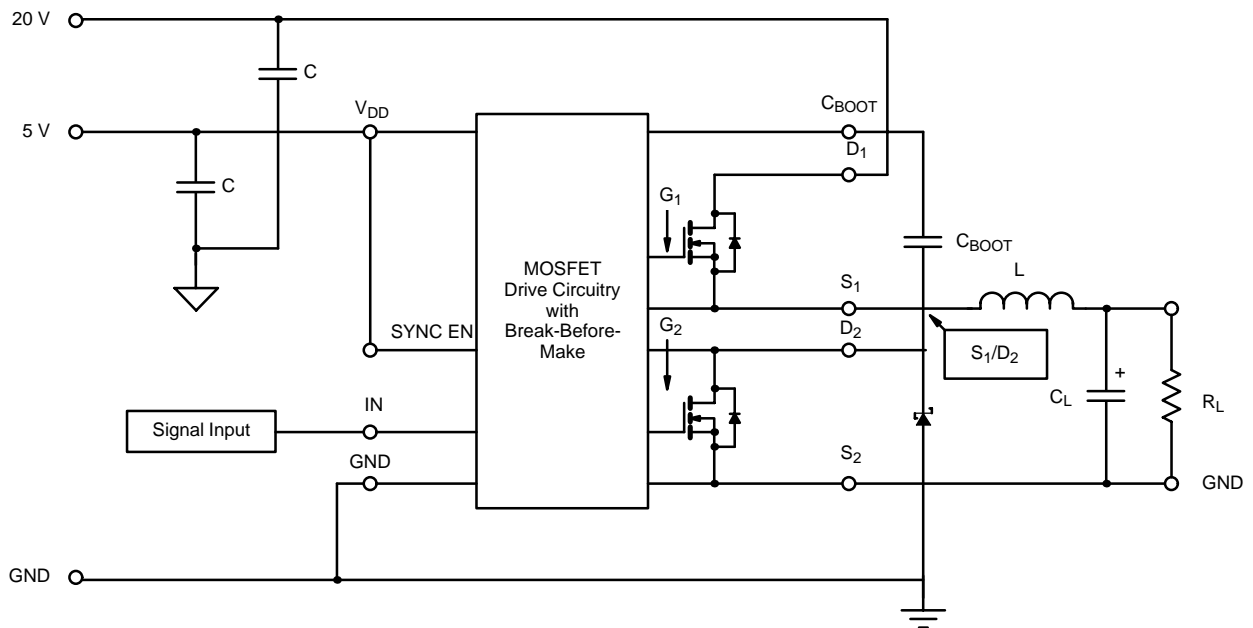
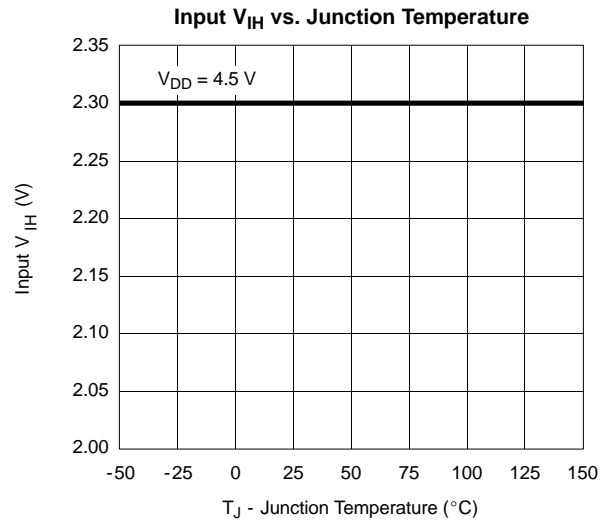
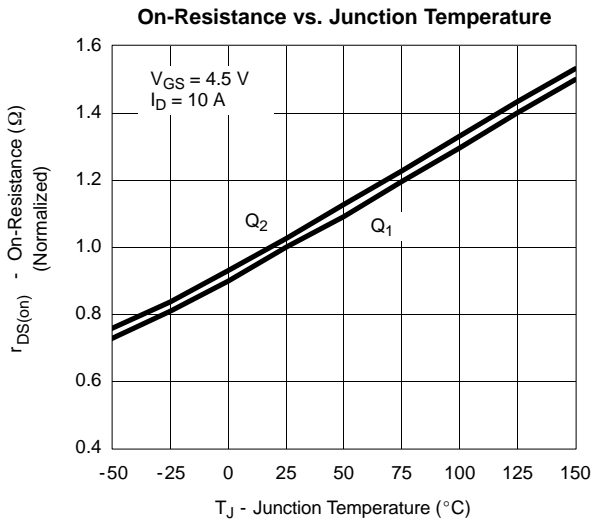
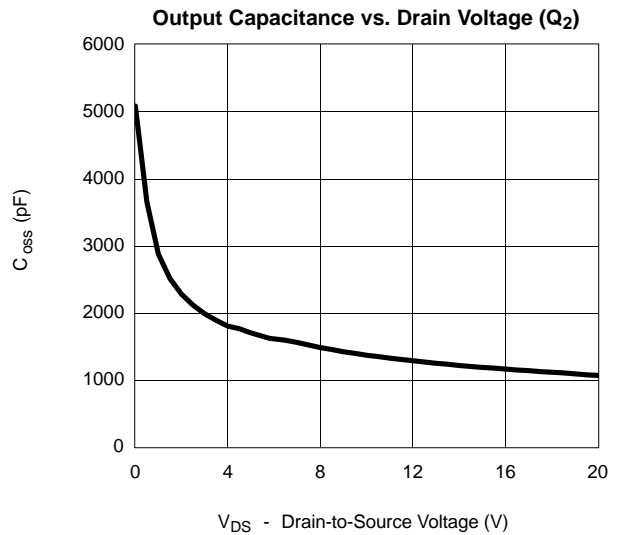
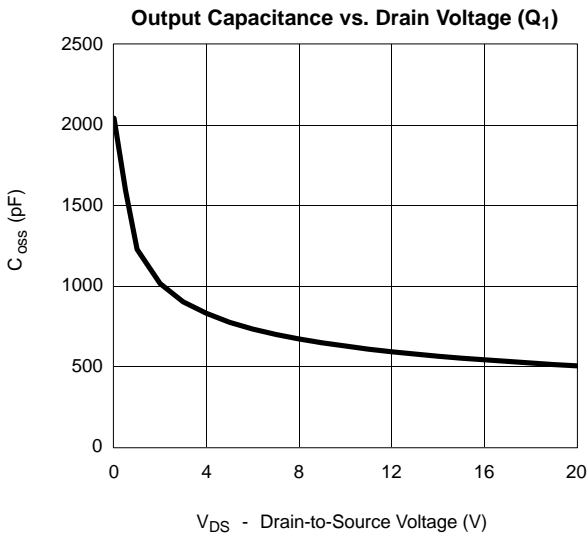
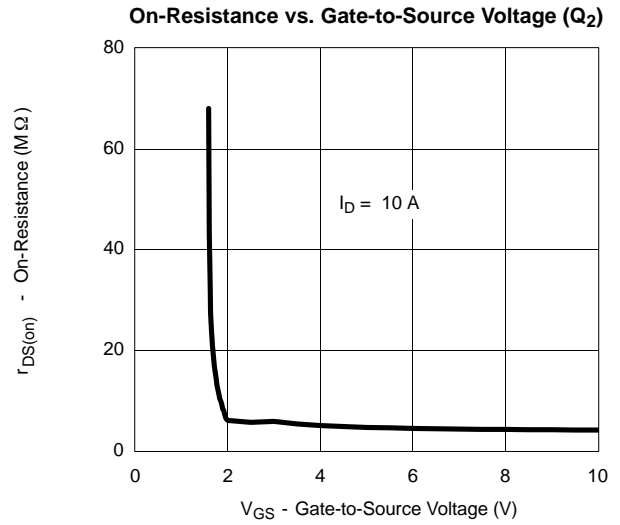
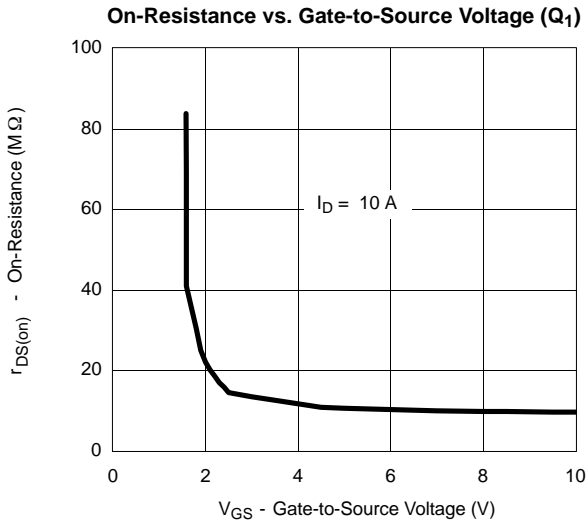


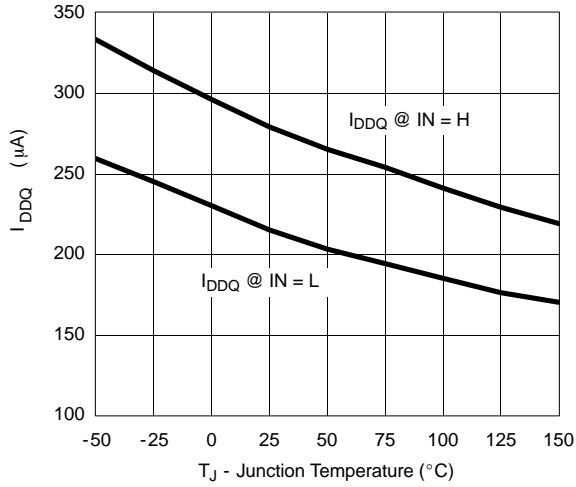
FIGURE 7.

TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

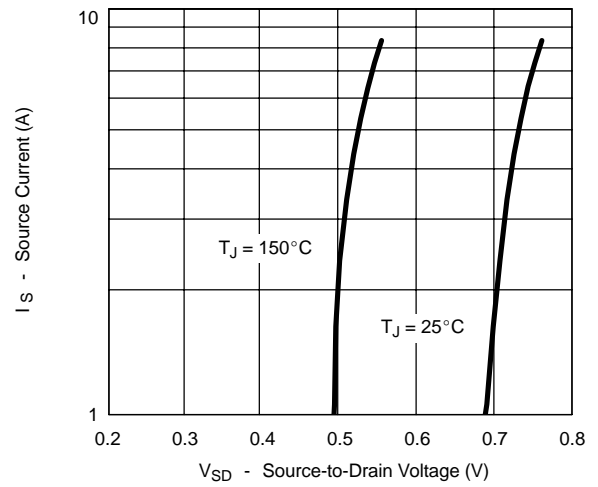


TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

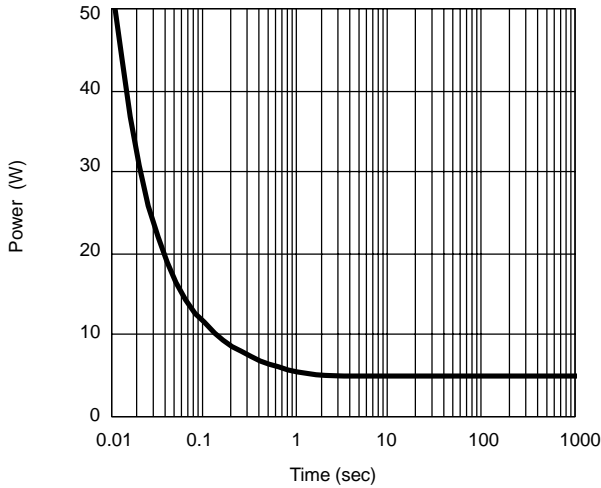
Input Current vs. Junction Temperature



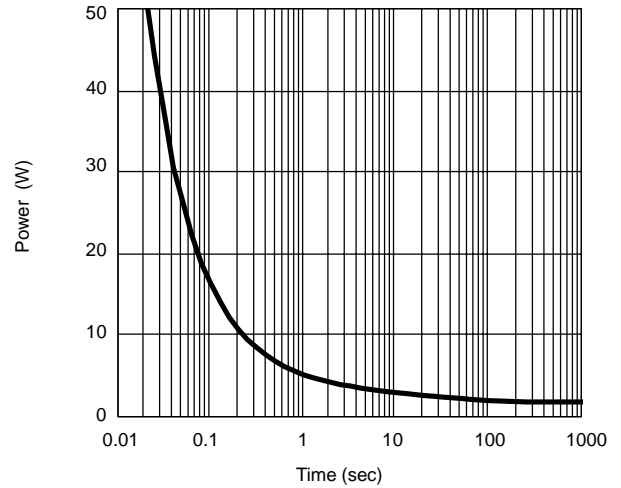
Source-Drain Diode Forward Voltage



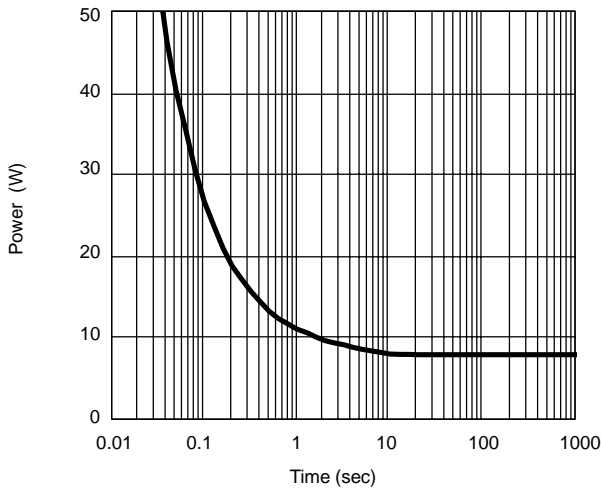
Single Pulse Power, Junction-to-Foot (Q₁)



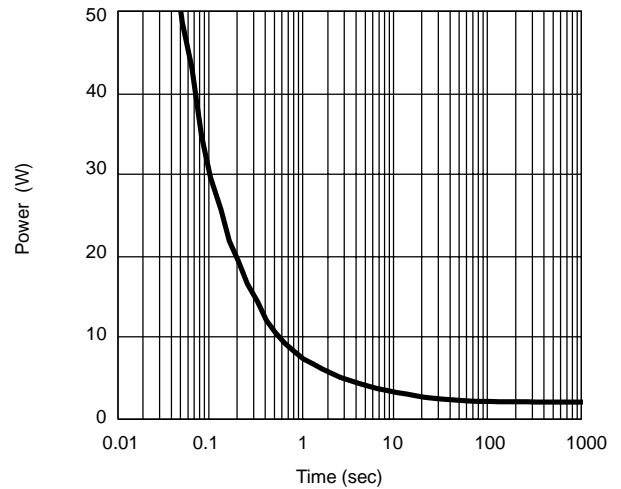
Single Pulse Power, Junction-to-Ambient (Q₁)



Single Pulse Power, Junction-to-Foot (Q₂)

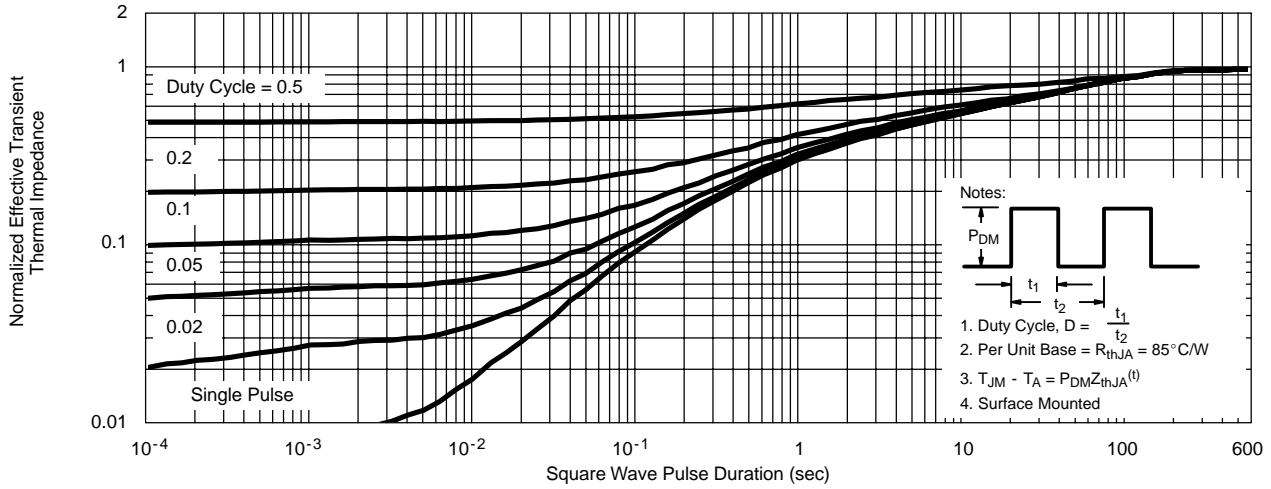


Single Pulse Power, Junction-to-Ambient (Q₂)

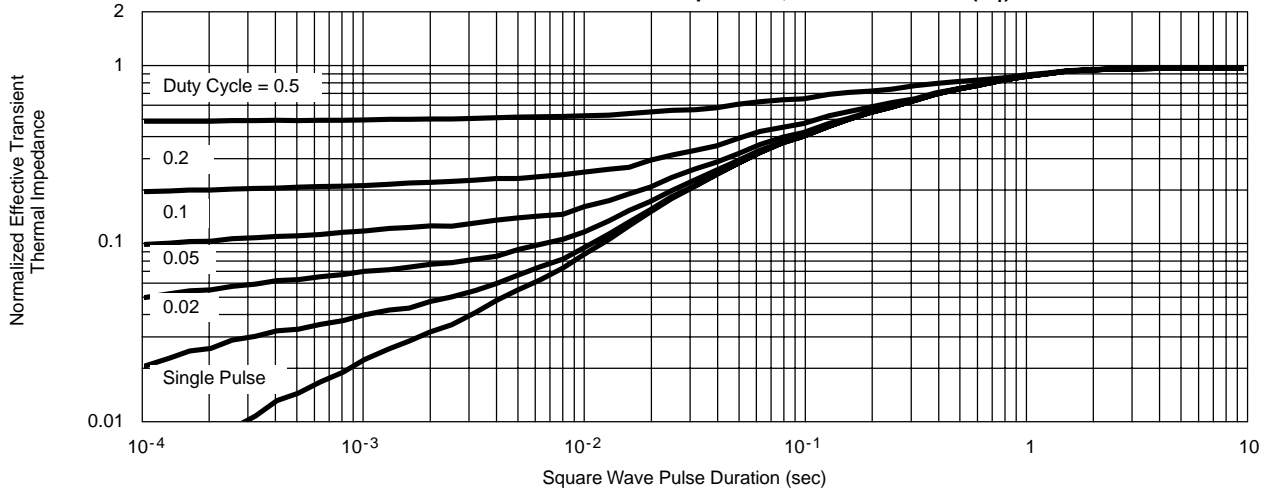


TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

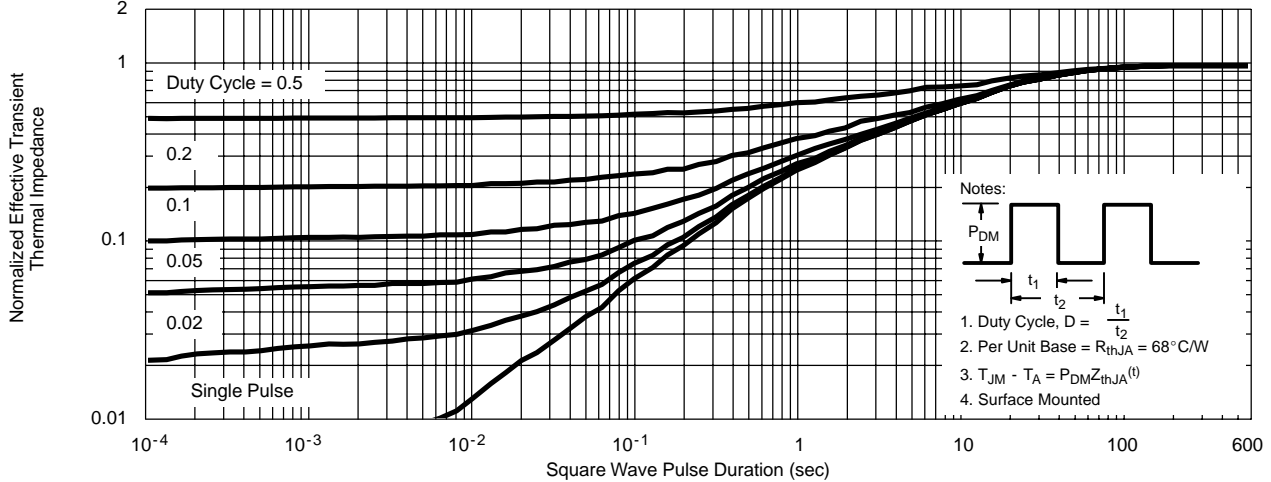
Normalized Thermal Transient Impedance, Junction-to-Ambient (Q_1)



Normalized Thermal Transient Impedance, Junction-to-Foot (Q_1)



Normalized Thermal Transient Impedance, Junction-to-Ambient (Q_2)





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TYPICAL CHARACTERISTICS (25°C UNLESS NOTED)

Normalized Thermal Transient Impedance, Junction-to-Foot (Q_2)

