Dual, Low Power, Precision Rail-to-Rail Output Op Amp

AD8622

FEATURES

- Very low offset voltage
  - 125 μV maximum
- Supply current: 215 μA/amp typical
- Input bias current: 200 pA maximum
- Low input offset voltage drift: 1.2 μV/°C maximum
- Very low voltage noise: 11 nV/√Hz
- Operating temperature: −40°C to +125°C
- Rail-to-rail output swing
- Unity gain stable
- ±2.5 V to ±15 V operation

APPLICATIONS

- Portable precision instrumentation
- Laser diode control loops
- Strain gage amplifiers
- Medical instrumentation
- Thermocouple amplifiers

PIN CONFIGURATIONS

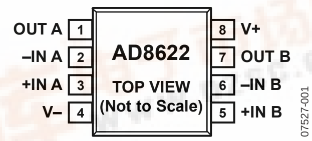

Figure 1. 8-Lead Narrow-Body SOIC

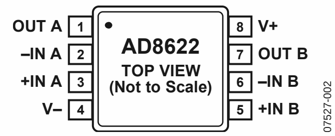

Figure 2. 8-Lead MSOP

GENERAL DESCRIPTION

The AD8622 is a dual, precision rail-to-rail output operational amplifier with a low supply current of only 350 μA maximum over temperature and supply voltages. It also offers ultralow offset, drift, and voltage noise combined with very low input bias current over the full operating temperature range.

With typical offset voltage of only 10 μV, offset drift of 0.5 μV/°C, and noise of only 0.2 μV p-p (0.1 Hz to 10 Hz), it is perfectly suited for applications where large error sources cannot be tolerated. Many systems can take advantage of the low noise, dc precision, and rail-to-rail output swing provided by the AD8622 to maximize the signal-to-noise ratio and dynamic range for low power operation. The AD8622 is specified for the extended industrial temperature range of −40°C to +125°C and is available in lead-free SOIC and MSOP packages.

Table 1. Low Power Op Amps

Supply	40 V	36 V	12 V to 16 V	5 V
Single	OP97	OP777 OP1177	OP196 AD8663	AD8603
Dual	OP297	OP727 OP2177 AD706	OP296 AD8667	AD8607
Quad	OP497	OP747 OP4177 AD704	OP496 AD8669	AD8609

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REVISION HISTORY

7/09—Revision 0: Initial Version

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS—±15 V OPERATION

V_S = ±15 V, V_{CM} = 0 V, T_A = +25°C, unless otherwise specified.

Table 2.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}			10	125	μV
		−40°C ≤ T_A ≤ +125°C			230	μV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	−40°C ≤ T_A ≤ +125°C		0.5	1.2	μV/°C
Input Bias Current	I_B			45	200	pA
		−40°C ≤ T_A ≤ +125°C			500	pA
Input Offset Current	I_{OS}			35	200	pA
		−40°C ≤ T_A ≤ +125°C			500	pA
Input Voltage Range			−13.8		+13.8	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = −13.8 V to +13.8 V	125	135		dB
		−40°C ≤ T_A ≤ +125°C	112			dB
Open-Loop Gain	A_{VO}	R_L = 10 kΩ, V_O = −13.5 V to +13.5 V	125	137		dB
		−40°C ≤ T_A ≤ +125°C	120			dB
Input Resistance, Differential Mode	R_{INDM}			1		GΩ
Input Resistance, Common Mode	R_{INCM}			1		TΩ
Input Capacitance, Differential Mode	C_{INDM}			5.5		pF
Input Capacitance, Common Mode	C_{INCM}			3		pF
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	R_L = 100 kΩ to ground	14.94	14.97		V
		−40°C ≤ T_A ≤ +125°C	14.84			V
		R_L = 10 kΩ to ground	14.86	14.89		V
		−40°C ≤ T_A ≤ +125°C	14.75			V
Output Voltage Low	V_{OL}	R_L = 100 kΩ to ground		−14.97	−14.94	V
		−40°C ≤ T_A ≤ +125°C			−14.92	V
		R_L = 10 kΩ to ground		−14.89	−14.90	V
		−40°C ≤ T_A ≤ +125°C			−14.80	V
Short-Circuit Current	I_{SC}			±40		mA
Closed-Loop Output Impedance	Z_{OUT}	f = 1 kHz, A_V = 1		1.5		Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = ±2.0 V to ±18.0 V	125	145		dB
		−40°C ≤ T_A ≤ +125°C	120			dB
Supply Current/Amplifier	I_{SY}	I_O = 0 mA		215	250	μA
		−40°C ≤ T_A ≤ +125°C			350	μA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 10 kΩ, A_V = 1		0.48		V/μs
Gain Bandwidth Product	GBP	C_L = 35 pF, A_V = 1		600		kHz
Phase Margin	Φ_M	C_L = 35 pF, A_V = 1		72		Degrees
NOISE PERFORMANCE						
Voltage Noise	e_n p-p	f = 0.1 Hz to 10 Hz		0.2		μV p-p
Voltage Noise Density	e_n	f = 1 kHz		11		nV/√Hz
Uncorrelated Current Noise Density	i_n	f = 1 kHz		0.15		pA/√Hz
Correlated Current Noise Density	i_n	f = 1 kHz		0.06		pA/√Hz

ELECTRICAL CHARACTERISTICS—±2.5 V OPERATION

V_S = ±2.5 V, V_{CM} = 0 V, T_A = +25°C, unless otherwise specified.

Table 3.

Parameter	Symbol	Conditions	Min	Typ	Max	Unit
INPUT CHARACTERISTICS						
Offset Voltage	V_{OS}			10	125	µV
		−40°C ≤ T_A ≤ +125°C			230	µV
Offset Voltage Drift	$\Delta V_{OS}/\Delta T$	−40°C ≤ T_A ≤ +125°C		0.5	1.2	µV/°C
Input Bias Current	I_B			30	200	pA
		−40°C ≤ T_A ≤ +125°C			400	pA
Input Offset Current	I_{OS}			25	200	pA
		−40°C ≤ T_A ≤ +125°C			300	pA
Input Voltage Range		−40°C ≤ T_A ≤ +125°C	−1.3		+1.3	V
Common-Mode Rejection Ratio	CMRR	V_{CM} = −1.3 V to +1.3 V	110	120		dB
		−40°C ≤ T_A ≤ +125°C	107			dB
Open-Loop Gain	A_{VO}	R_L = 10 kΩ, V_O = −2.0 V to +2.0 V	118	135		dB
		−40°C ≤ T_A ≤ +125°C	109			dB
Input Resistance, Differential Mode	R_{INDM}			1		GΩ
Input Resistance, Common Mode	R_{INDM}			1		TΩ
Input Capacitance, Differential Mode	C_{INDM}			5.5		pF
Input Capacitance, Common Mode	C_{INCM}			3		pF
OUTPUT CHARACTERISTICS						
Output Voltage High	V_{OH}	R_L = 100 kΩ to ground	2.45	2.49		V
		−40°C ≤ T_A ≤ +125°C	2.41			V
		R_L = 10 kΩ to ground	2.40	2.45		V
		−40°C ≤ T_A ≤ +125°C	2.36			V
Output Voltage Low	V_{OL}	R_L = 100 kΩ to ground		−2.49	−2.45	V
		−40°C ≤ T_A ≤ +125°C			−2.41	V
		R_L = 10 kΩ to ground		−2.45	−2.40	V
		−40°C ≤ T_A ≤ +125°C			−2.36	V
Short-Circuit Current	I_{SC}			±30		mA
Closed-Loop Output Impedance	Z_{OUT}	f = 1 kHz, A_V = 1		2		Ω
POWER SUPPLY						
Power Supply Rejection Ratio	PSRR	V_S = ±2.0 V to ±18.0 V	125	145		dB
		−40°C ≤ T_A ≤ +125°C	120			dB
Supply Current/Amplifier	I_{SY}	I_O = 0 mA		175	225	µA
		−40°C ≤ T_A ≤ +125°C			310	µA
DYNAMIC PERFORMANCE						
Slew Rate	SR	R_L = 10 kΩ, A_V = 1		0.28		V/µs
Gain Bandwidth Product	GBP	C_L = 35 pF, A_V = 1		580		kHz
Phase Margin	Φ_M	C_L = 35 pF, A_V = 1		72		Degrees
NOISE PERFORMANCE						
Voltage Noise	e_n p-p	f = 0.1 Hz to 10 Hz		0.2		µV p-p
Voltage Noise Density	e_n	f = 1 kHz		12		nV/√Hz
Uncorrelated Current Noise Density	i_n	f = 1 kHz		0.15		pA/√Hz
Correlated Current Noise Density	i_n	f = 1 kHz		0.07		pA/√Hz

ABSOLUTE MAXIMUM RATINGS

Table 4.

Parameter	Rating
Supply Voltage	± 18 V
Input Voltage	±V supply
Input Current[1]	±10 mA
Differential Input Voltage[2]	±10 V
Output Short-Circuit Duration to GND	Indefinite
Storage Temperature Range	−65°C to +150°C
Operating Temperature Range	−40°C to +125°C
Junction Temperature Range	−65°C to +150°C
Lead Temperature (Soldering, 60 sec)	300°C

[1] The input pins have clamp diodes to the power supply pins. The input current should be limited to 10 mA or less whenever input signals exceed the power supply rail by 0.5 V.
[2] Differential input voltage is limited to 10 V or the supply voltage, whichever is less.

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

THERMAL RESISTANCE

θ_{JA} is specified for the worst-case conditions, that is, a device soldered in a circuit board for surface-mount packages. This was measured using a standard 4-layer board.

Table 5. Thermal Resistance

Package Type	θ_{JA}	θ_{JC}	Unit
8-Lead SOIC_N (R-8)	158	43	°C/W
8-Lead MSOP (RM-8)	185	53	°C/W

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

TYPICAL PERFORMANCE CHARACTERISTICS

T_A = 25°C, unless otherwise noted.

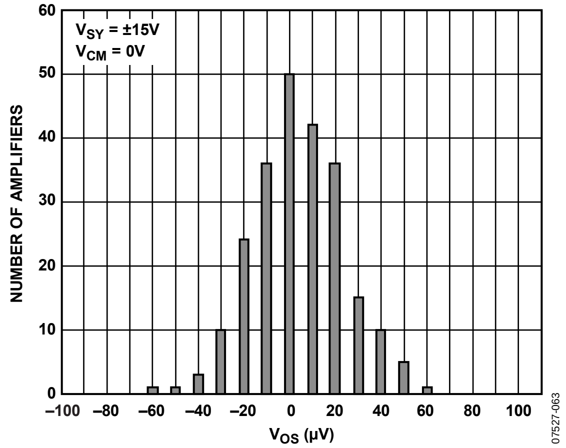
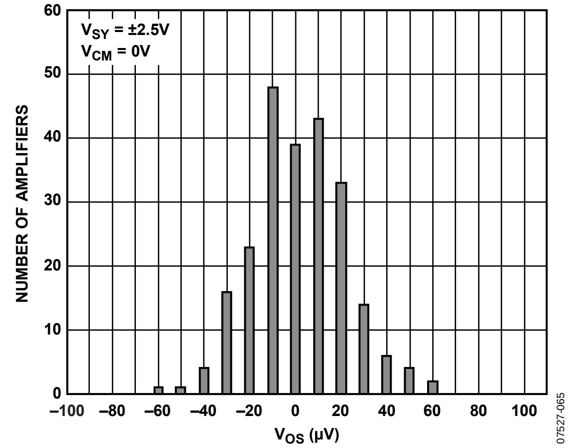


Figure 3. Input Offset Voltage Distribution



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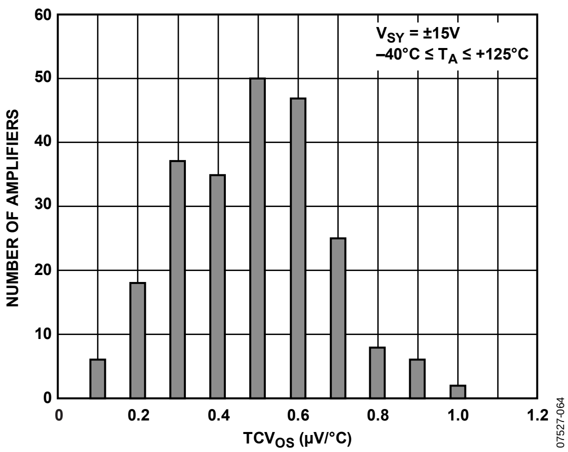


Figure 4. Input Offset Voltage Drift Distribution

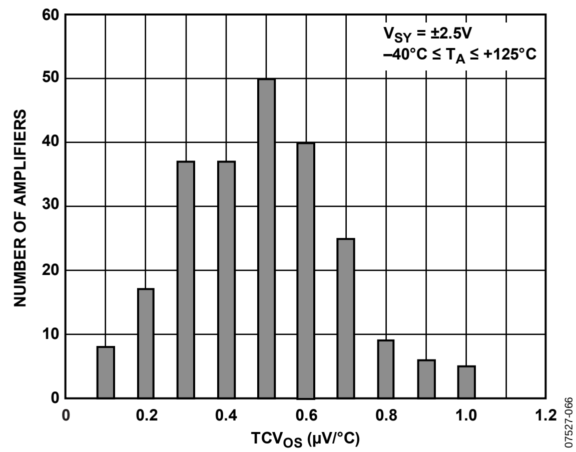


Figure 7. Input Offset Voltage Drift Distribution

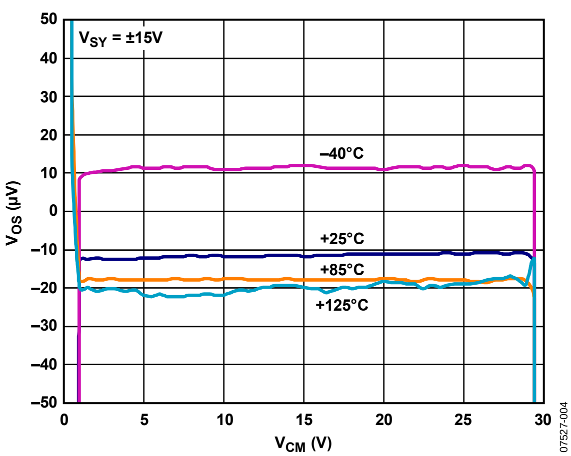


Figure 5. Input Offset Voltage vs. Common-Mode Voltage

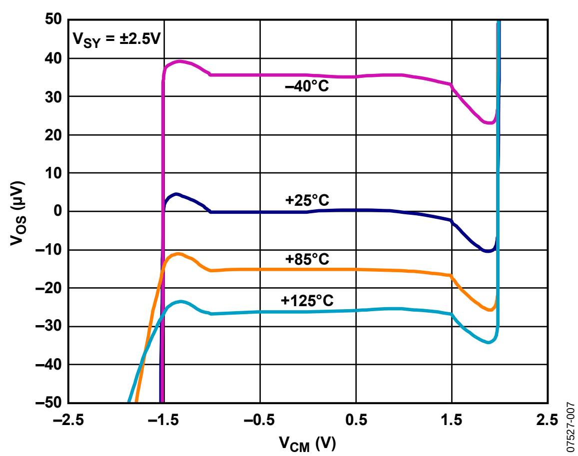


Figure 8. Input Offset Voltage vs. Common-Mode Voltage

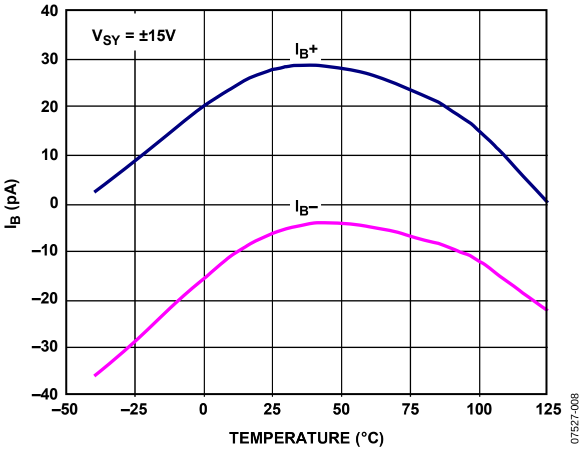
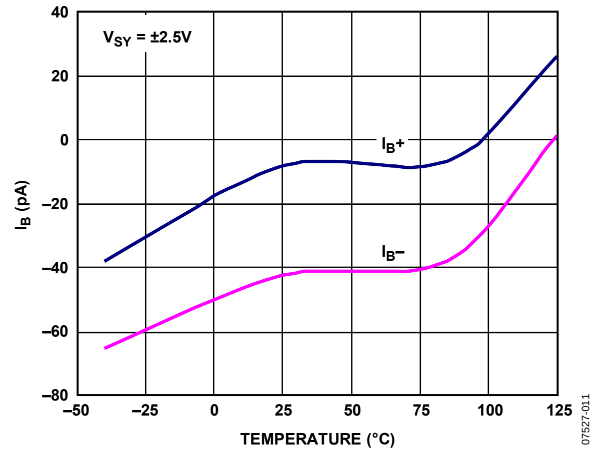


Figure 9. Input Bias Current vs. Temperature



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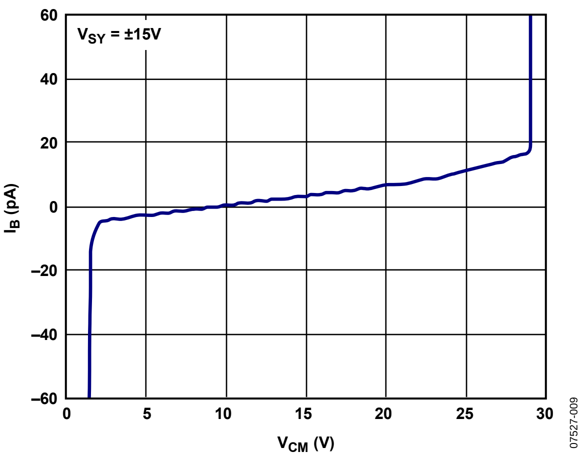
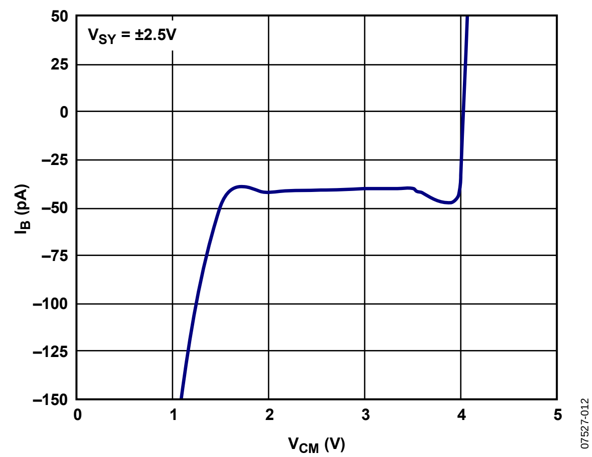


Figure 10. Input Bias Current vs. Common-Mode Voltage



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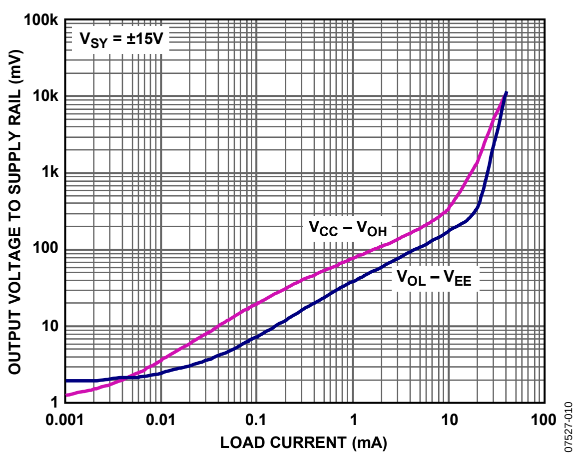


Figure 11. Output Voltage to Supply Rail vs. Load Current

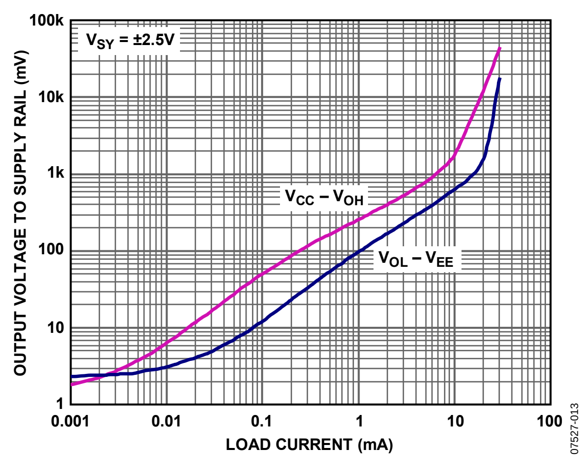


Figure 14. Output Voltage to Supply Rail vs. Load Current

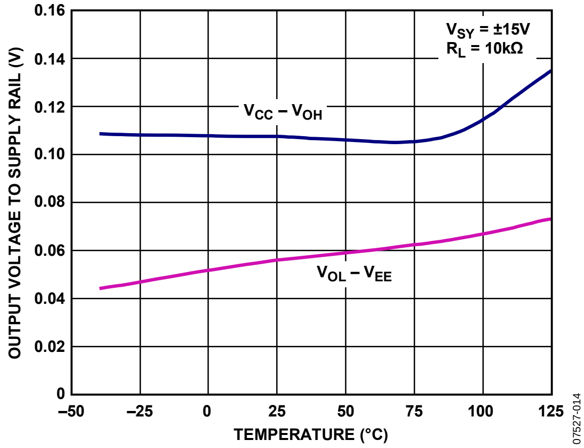


Figure 15. Output Voltage to Supply Rail vs. Temperature

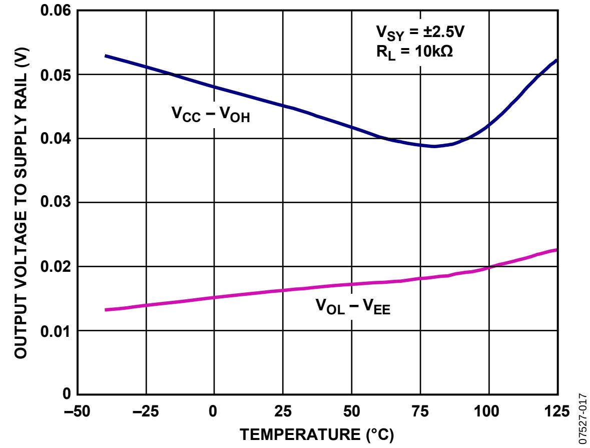


Figure 18. Output Voltage to Supply Rail vs. Temperature

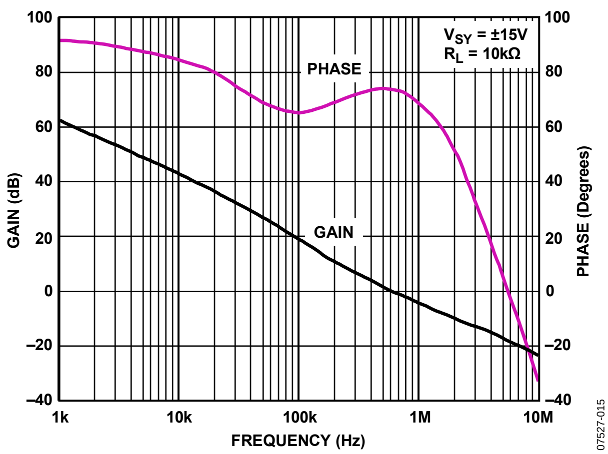
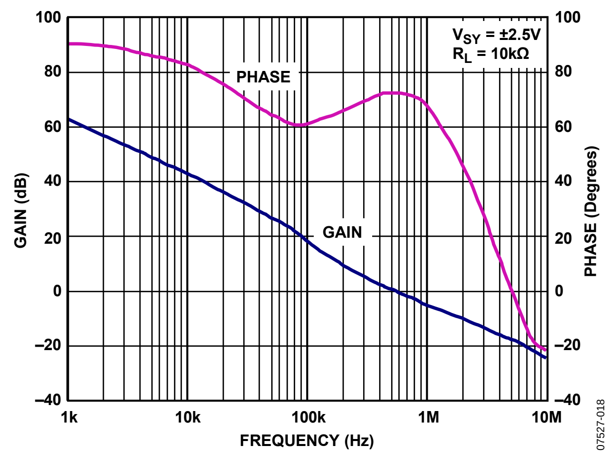


Figure 16. Open-Loop Gain and Phase vs. Frequency



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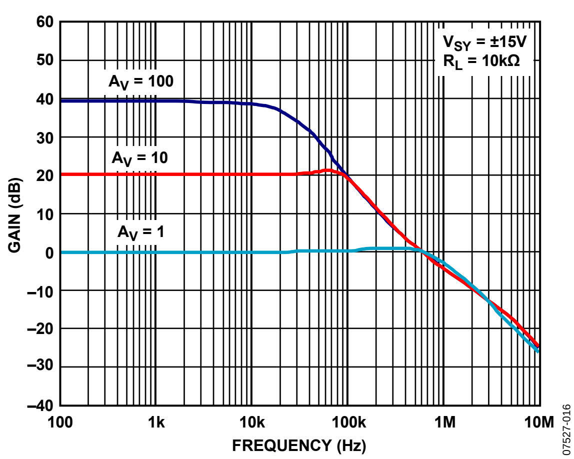

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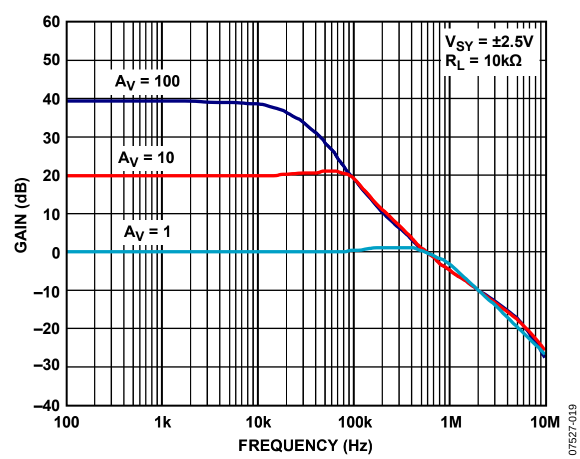

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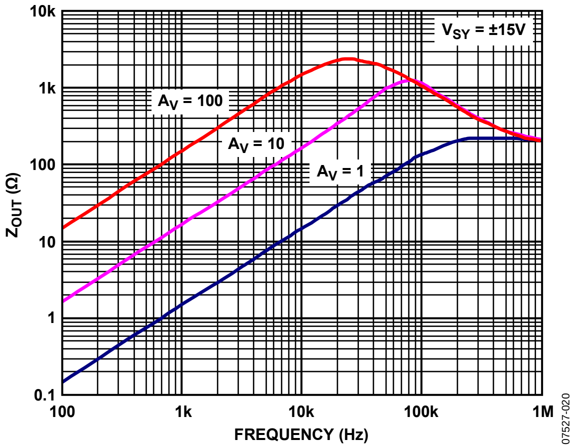


Figure 21. Output Impedance vs. Frequency

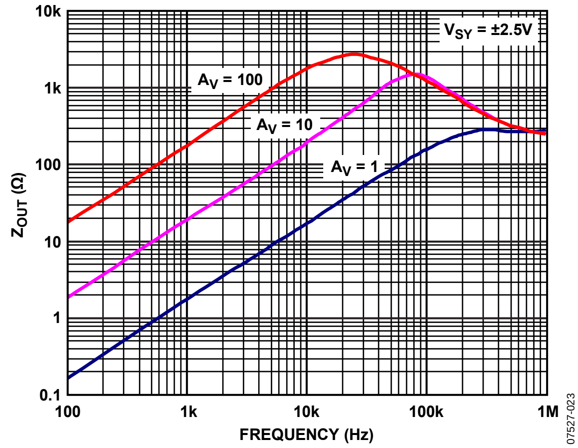


Figure 24. Output Impedance vs. Frequency

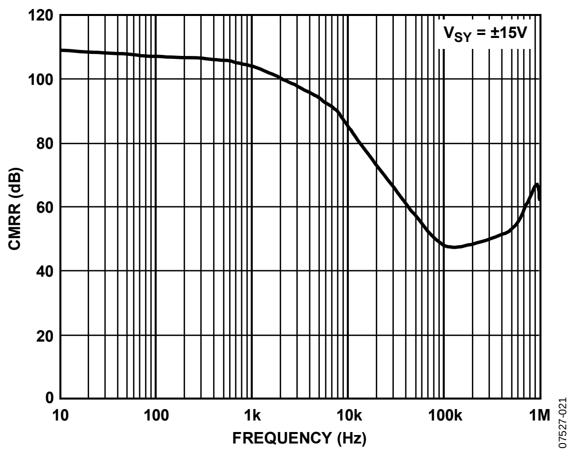


Figure 22. CMRR vs. Frequency

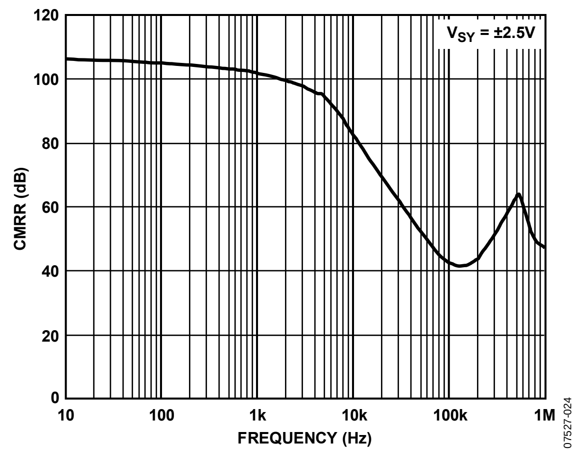


Figure 25. CMRR vs. Frequency

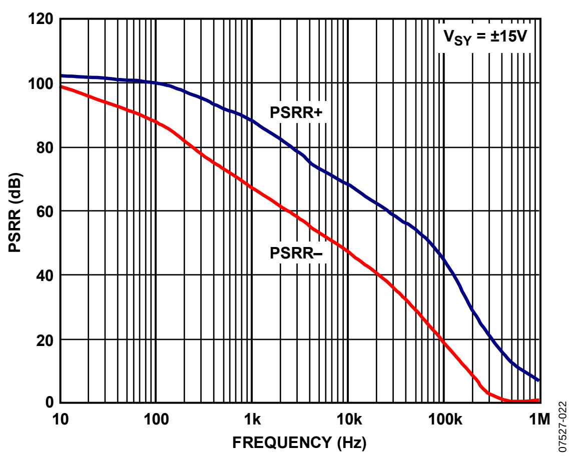


Figure 23. PSRR vs. Frequency

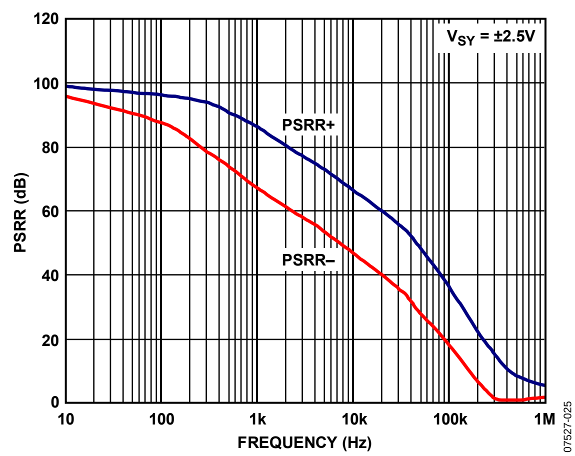


Figure 26. PSRR vs. Frequency

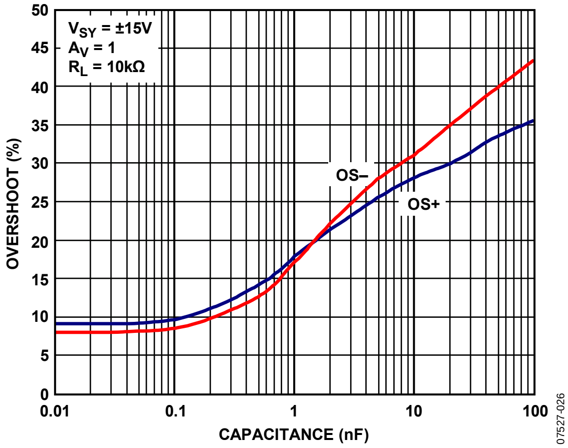


Figure 27. Small-Signal Overshoot vs. Load Capacitance

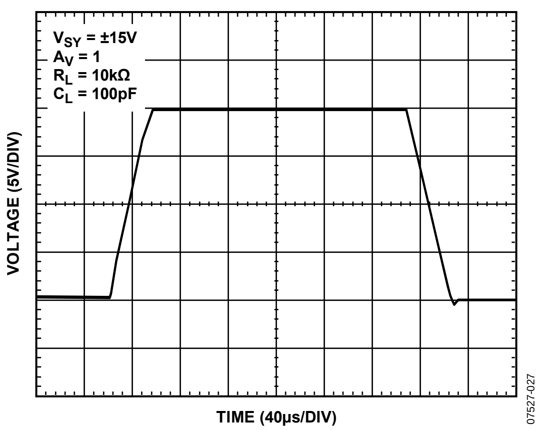


Figure 28. Large-Signal Transient Response

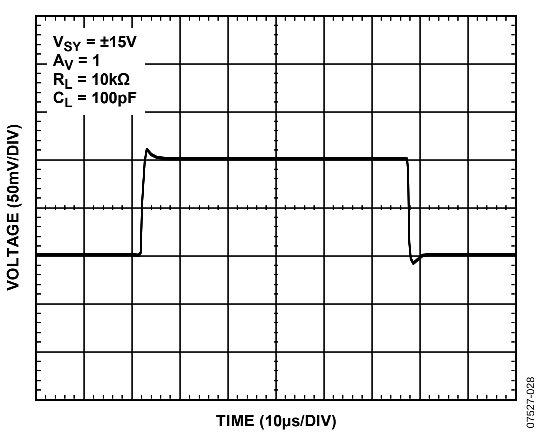


Figure 29. Small-Signal Transient Response

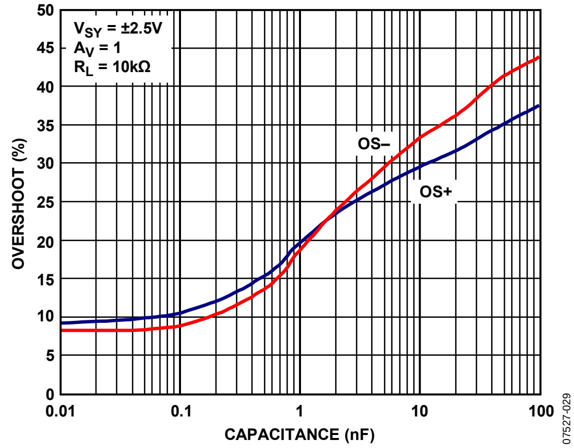


Figure 30. Small-Signal Overshoot vs. Load Capacitance

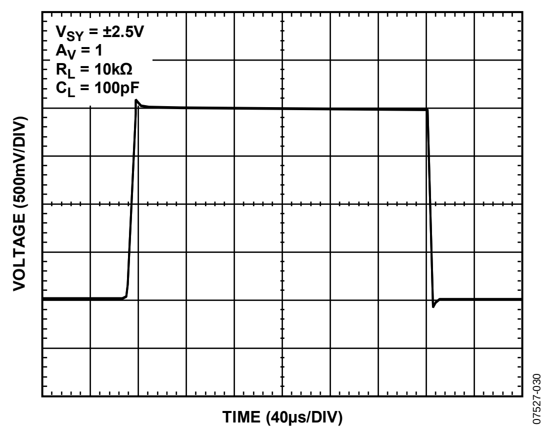


Figure 31. Large-Signal Transient Response

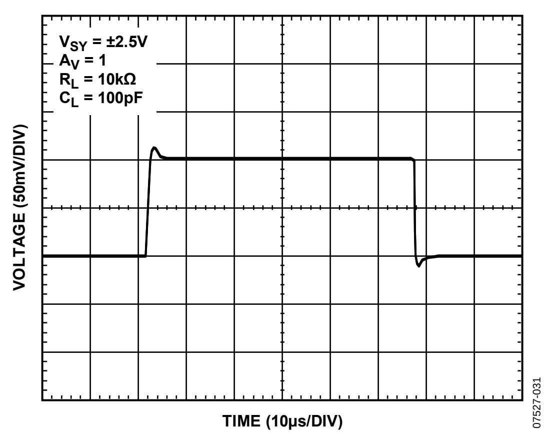


Figure 32. Small-Signal Transient Response

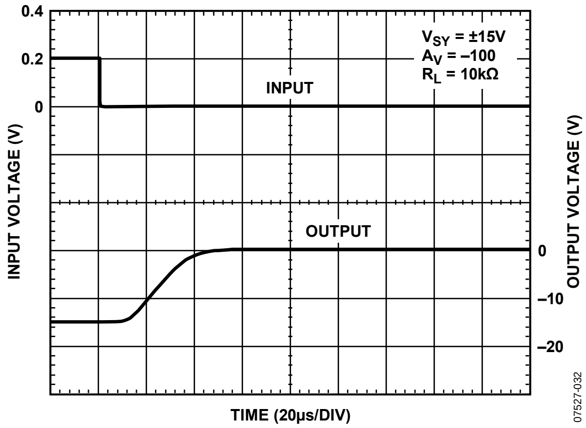


Figure 33. Negative Overload Recovery

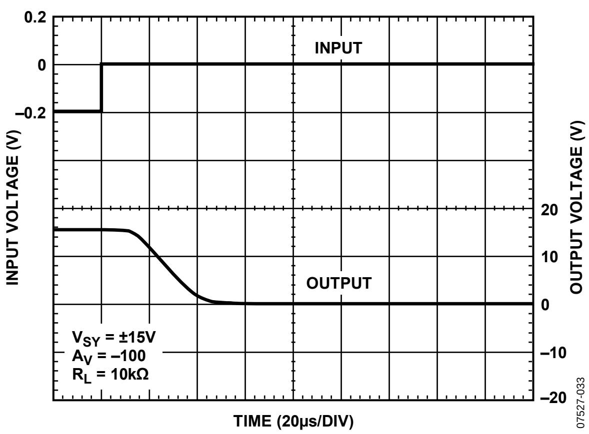


Figure 34. Positive Overload Recovery

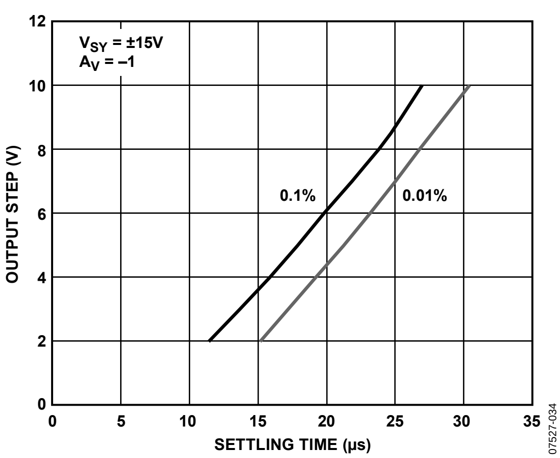


Figure 35. Output Step vs. Settling Time

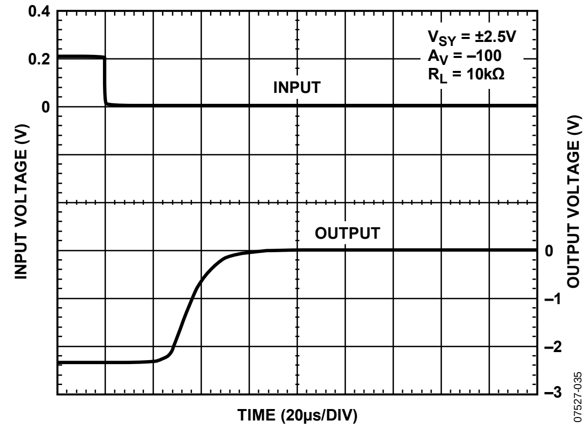


Figure 36. Negative Overload Recovery

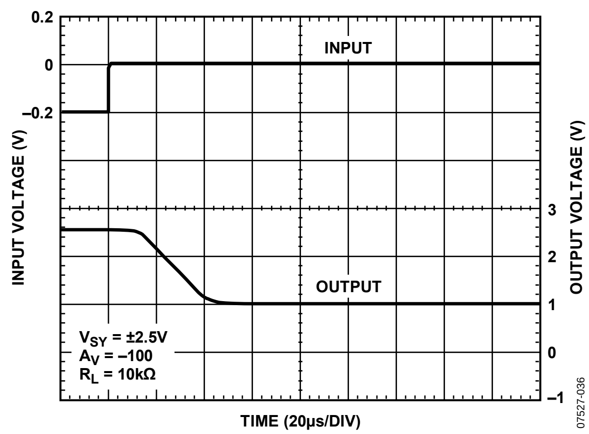


Figure 37. Positive Overload Recovery

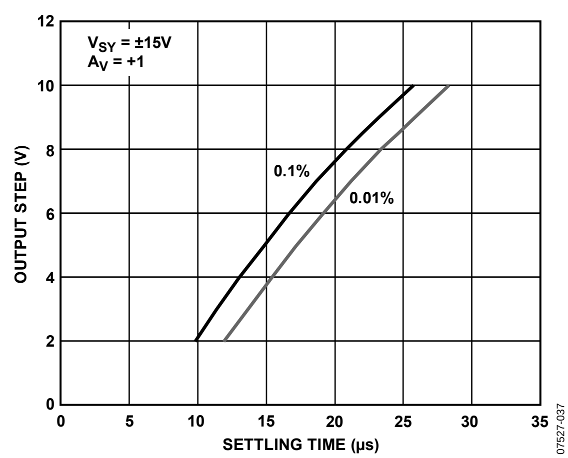


Figure 38. Output Step vs. Settling Time

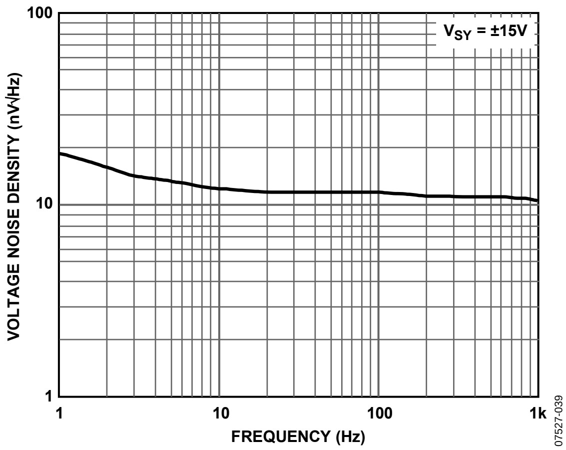


Figure 39. Voltage Noise Density vs. Frequency

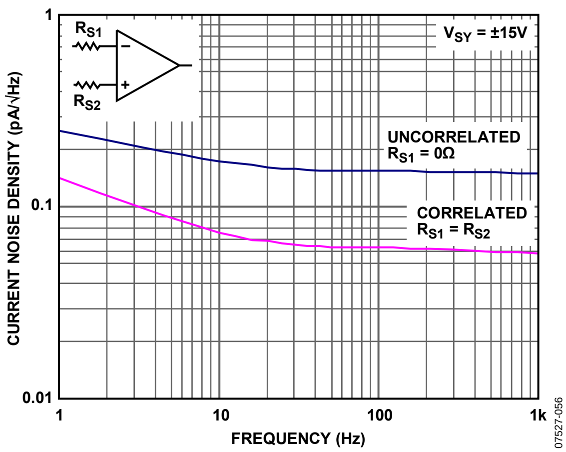


Figure 40. Current Noise Density vs. Frequency

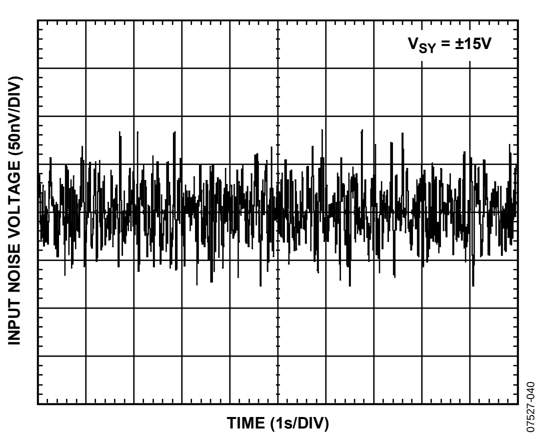


Figure 41. 0.1 Hz to 10 Hz Noise

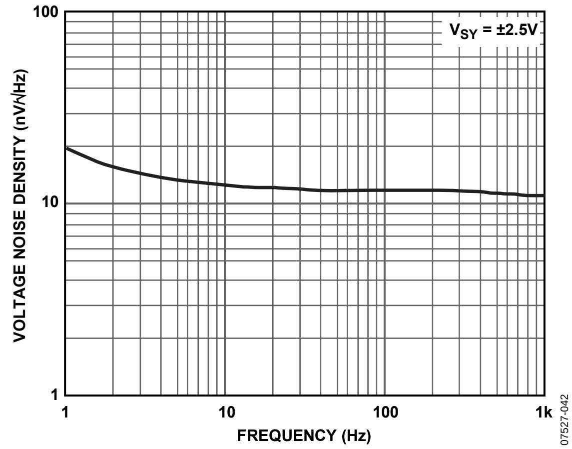


Figure 42. Voltage Noise Density vs. Frequency

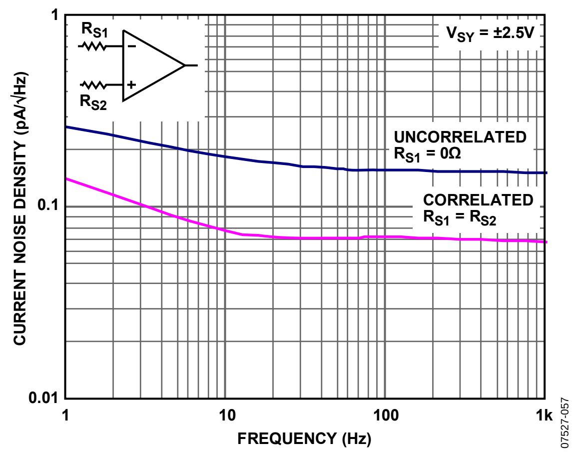


Figure 43. Current Noise Density vs. Frequency

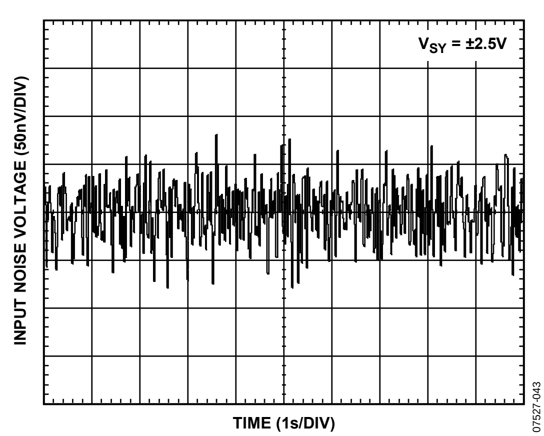


Figure 44. 0.1 Hz to 10 Hz Noise

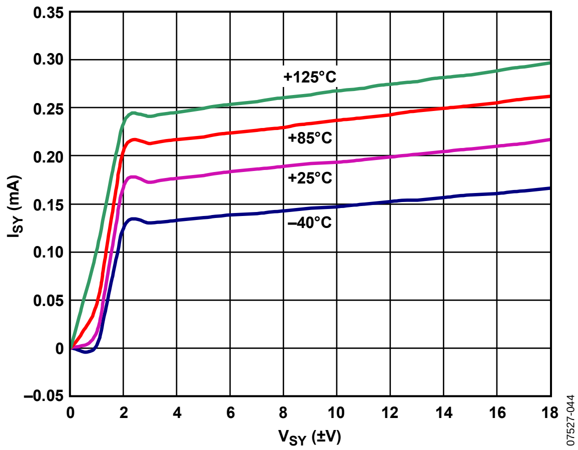


Figure 45. Supply Current vs. Supply Voltage

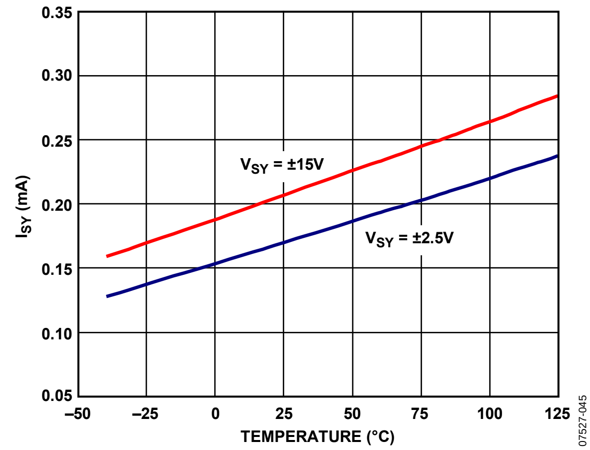


Figure 48. Supply Current vs. Temperature

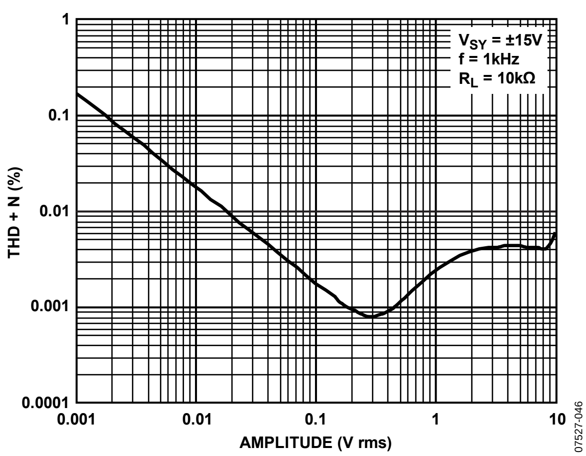


Figure 46. THD + Noise vs. Amplitude

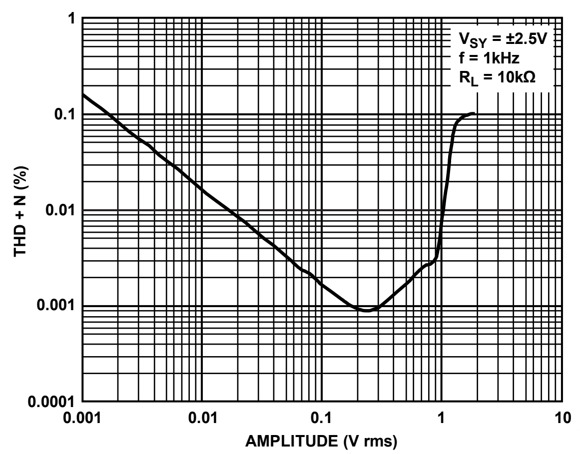


Figure 49. THD + Noise vs. Amplitude

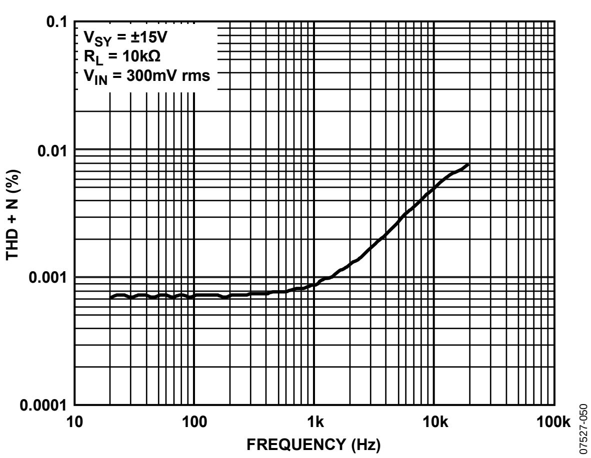


Figure 47. THD + Noise vs. Frequency

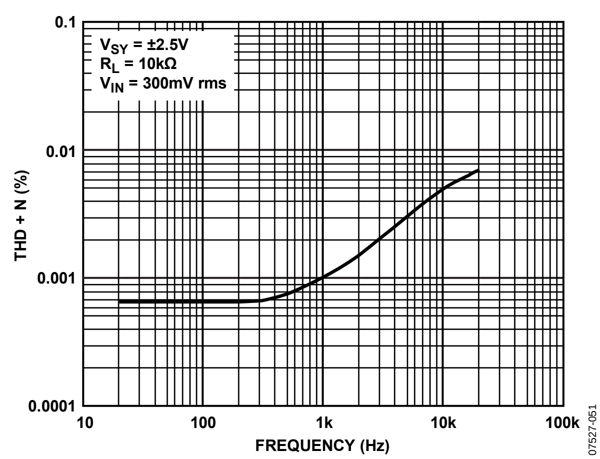


Figure 50. THD + Noise vs. Frequency

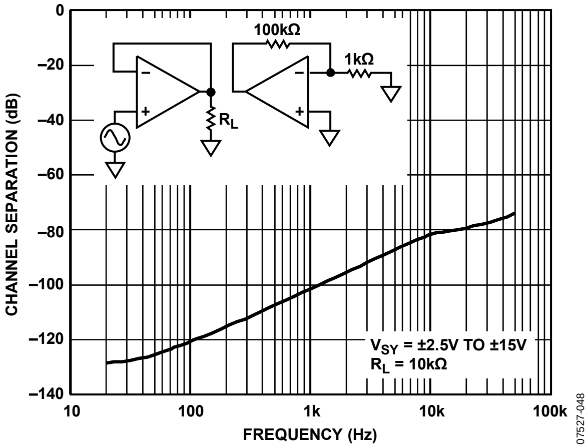


Figure 51. Channel Separation vs. Frequency

APPLICATIONS INFORMATION

INPUT PROTECTION

The maximum differential input voltage that can be applied to the AD8622 is determined by the internal diodes connected across its inputs and series resistors at each input. These internal diodes and series resistors limit the maximum differential input voltage to ±10 V and are needed to prevent base-emitter junction breakdown from occurring in the input stage of the AD8622 when very large differential voltages are applied. In addition, the internal resistors limit the currents that flow through the diodes. However, in applications where large differential voltages can be inadvertently applied to the device, large currents may still flow through these diodes. In such a case, external resistors must be placed at both inputs of the op amp to limit the input currents to ±10 mA (see Figure 52).

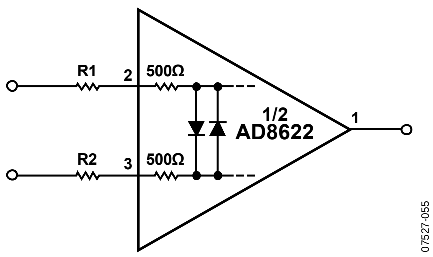


Figure 52. Input Protection

PHASE REVERSAL

An undesired phenomenon, phase reversal (also known as phase inversion) occurs in many op amps when one or both of the inputs are driven beyond the specified input voltage range (IVR), in effect reversing the polarity of the output. In some cases, phase reversal can induce lockups and even cause equipment damage as well as self destruction.

The AD8622 amplifiers have been carefully designed to prevent output phase reversal when both inputs are maintained within the specified input voltage range. In addition, even if one or both inputs exceed the input voltage range but remain within the supply rails, the output still does not phase reverse. Figure 53 shows the input/output waveforms of the AD8622 configured as a unity-gain buffer with a supply voltage of ±15 V.

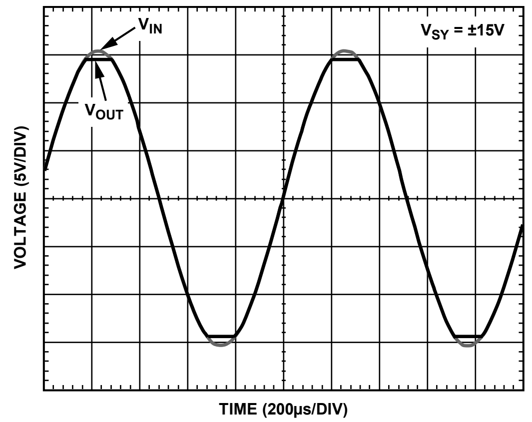
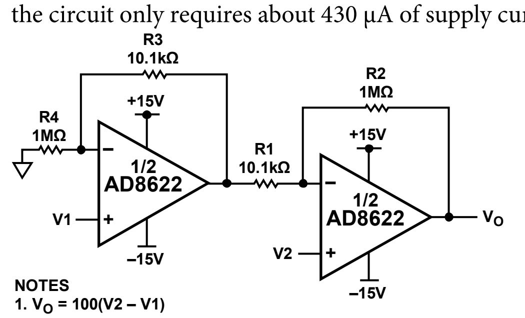


Figure 53. No Phase Reversal

MICROPOWER INSTRUMENTATION AMPLIFIER

The AD8622 is a dual, high precision, rail-to-rail output op amp operating at just 215 µA quiescent current per amplifier. Its ultralow offset, offset drift, and voltage noise, combined with its very low bias current and high common-mode rejection ratio (CMRR), are ideally suited for high accuracy and micropower instrumentation amplifier.

Figure 54 shows the classic 2-op-amp instrumentation amplifier with four resistors using the AD8622. The key to high CMRR for this instrumentation amplifier are resistors that are well matched from both the resistive ratio and the relative drift. For true difference amplification, matching of the resistor ratio is very important, where R3/R4 = R1/R2. Assuming perfectly matched resistors, the gain of the circuit is 1 + R2/R1, which is approximately 100. Tighter matching of two op amps in one package, like the AD8622, offers a significant boost in performance over the classical 3-op-amp configuration. Overall, the circuit only requires about 430 µA of supply current.



NOTES
1. $V_O = 100(V2 – V1)$
2. TYPICAL: 0.01mV < |V2 – V1| < 149.7mV
3. TYPICAL: –14.97V < V_O < +14.97V
4. USE MATCHED RESISTORS.

Figure 54. Micropower Instrumentation Amplifier

HALL SENSOR SIGNAL CONDITIONING

The AD8622 is also highly suitable for high accuracy, low power signal conditioning circuits. One such use is in Hall sensor signal conditioning (see Figure 55). The magnetic sensitivity of a Hall element is proportional to the bias voltage applied across it. With 1 V bias voltage, the Hall element consumes about 2.5 mA of supply current and has a sensitivity of 5.5 mV/mT typical. To reduce power consumption, bias voltage must be reduced, but at the risk of lower sensitivity. The only way to achieve higher sensitivity is by introducing a gain using a precision micropower amplifier. The AD8622, with all its features, is well suited to amplify the sensitivity of the Hall element.

The ADR121 is a precision micropower 2.5 V voltage reference. A precision voltage reference is required to hold a constant current so that the Hall voltage only depends on the intensity of the magnetic field. Using the 4.12k:98.8k resistive divider, the bias voltage of the Hall element is reduced to 100 mV, leading to only 250 μA of power consumption. The 3-op-amp in-amp configuration of the AD8622 then increases the sensitivity to 55 mV/mT. Using the AD8622 to amplify the sensor signal can reduce power while also achieving higher sensitivity. The total current consumed is just 1.2 mA, resulting in 21× improvement in sensitivity/power.

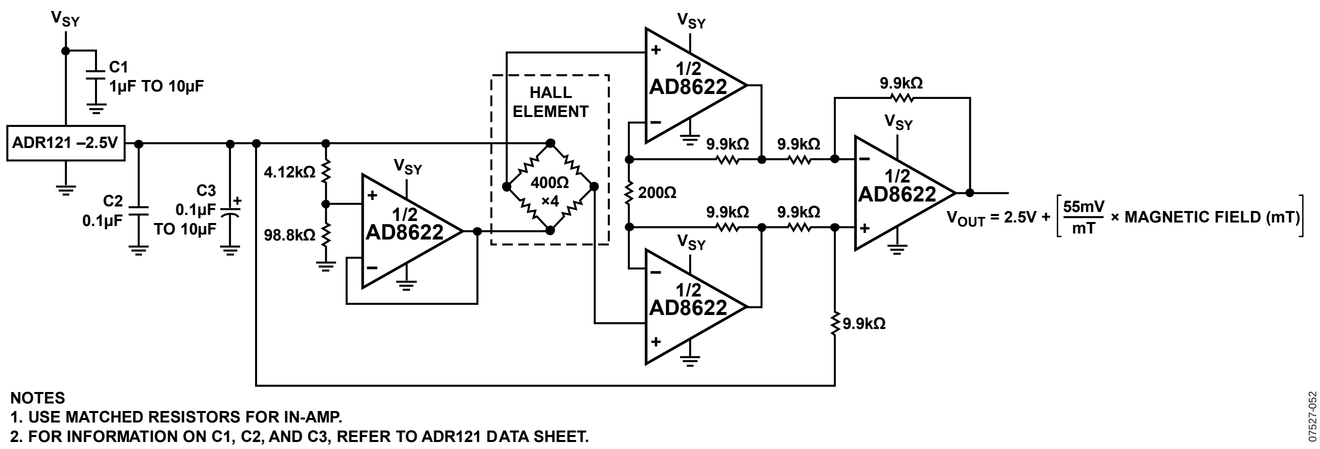


Figure 55. Hall Sensor Signal Conditioning

SIMPLIFIED SCHEMATIC

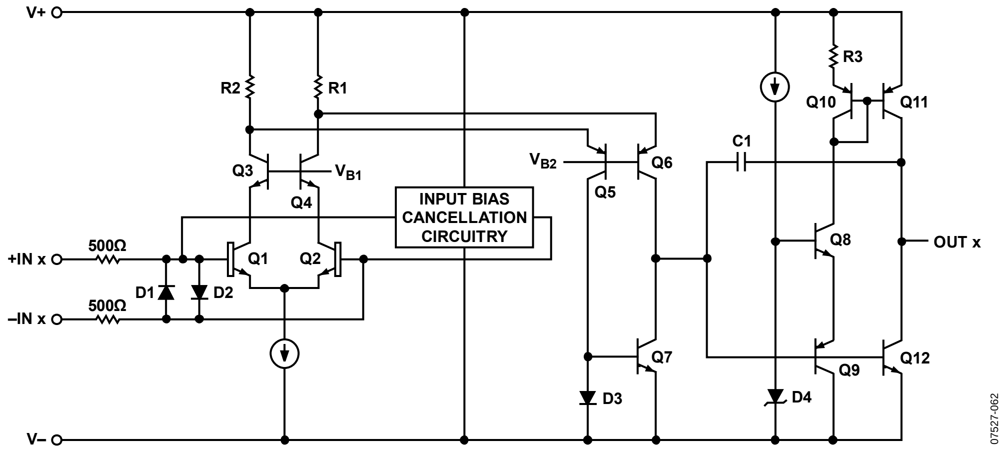


Figure 56. Simplified Schematic

OUTLINE DIMENSIONS

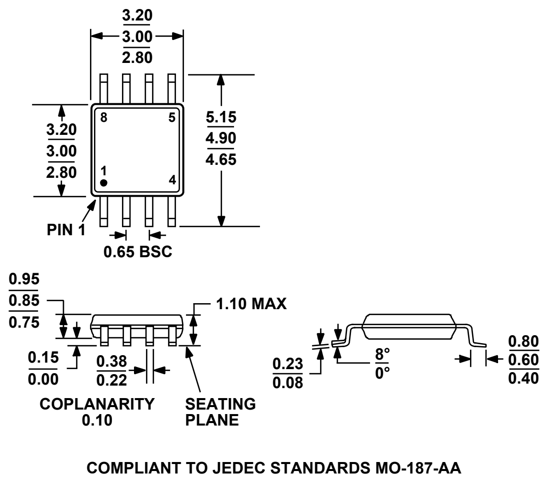


Figure 57. 8-Lead Mini Small Outline Package [MSOP]
(RM-8)
Dimensions shown in millimeters

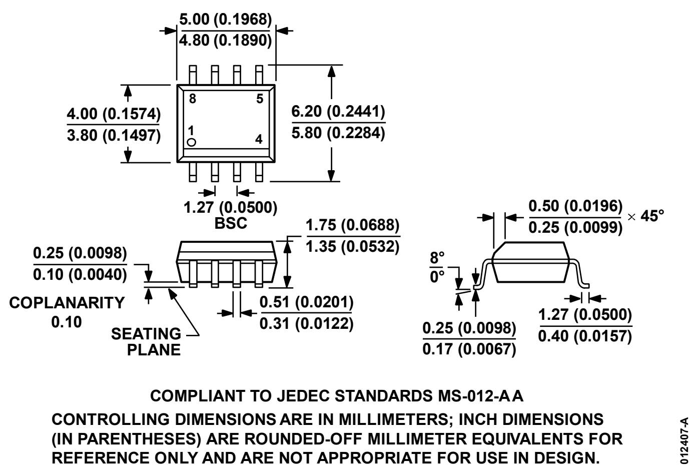


Figure 58. 8-Lead Standard Small Outline Package [SOIC_N]
Narrow Body
(R-8)
Dimensions shown in millimeters and (inches)

ORDERING GUIDE

Model	Temperature Range	Package Description	Package Option	Branding
AD8622ARMZ[1]	−40°C to +125°C	8-Lead MSOP	RM-8	A1P
AD8622ARMZ-REEL[1]	−40°C to +125°C	8-Lead MSOP	RM-8	A1P
AD8622ARMZ-R7[1]	−40°C to +125°C	8-Lead MSOP	RM-8	A1P
AD8622ARZ[1]	−40°C to +125°C	8-Lead SOIC_N	R-8	
AD8622ARZ-REEL[1]	−40°C to +125°C	8-Lead SOIC_N	R-8	
AD8622ARZ-REEL7[1]	−40°C to +125°C	8-Lead SOIC_N	R-8	

[1] Z = RoHS Compliant Part.

NOTES

NOTES