查询"5962-9754701Q2A"供应商

| REVISIONS | | | |
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| LTR | DESCRIPTION | DATE (YR-MO-DA) | APPROVED |
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| REV | | | | | | | | | | | | | | | | | | | |
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| REV STATUS OF SHEETS | REV | | | | | | | | | | | | | | | |
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| | SHEET | 1 | 2 | 3 | 4 | 5 | 6 | 7 | 8 | 9 | 10 | 11 | 12 | | |

| | | |
|---|---|---|
| PMIC N/A | PREPARED BY<br>Larry E. Shaw | DEFENSE SUPPLY CENTER COLUMBUS<br>COLUMBUS, OHIO 43216 |
| **STANDARD MICROCIRCUIT DRAWING**<br>THIS DRAWING IS AVAILABLE FOR USE BY ALL DEPARTMENTS AND AGENCIES OF THE DEPARTMENT OF DEFENSE<br>AMSC N/A | CHECKED BY<br>Tuan D. Nguyen<br>APPROVED BY<br>Ray L. Monnin<br>DRAWING APPROVAL DATE<br>97-03-14<br>REVISION LEVEL | MICROCIRCUIT, DIGITAL, BIPOLAR, LOW-POWER SCHOTTKY TTL, 4-BIT MAGNITUDE COMPARATORS, MONOLITHIC SILICON<br>SIZE A · CAGE CODE 67268 · **5962-97547**<br>SHEET 1 OF 12 |

ESC FORM 193
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5962-E105-97

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1. SCOPE

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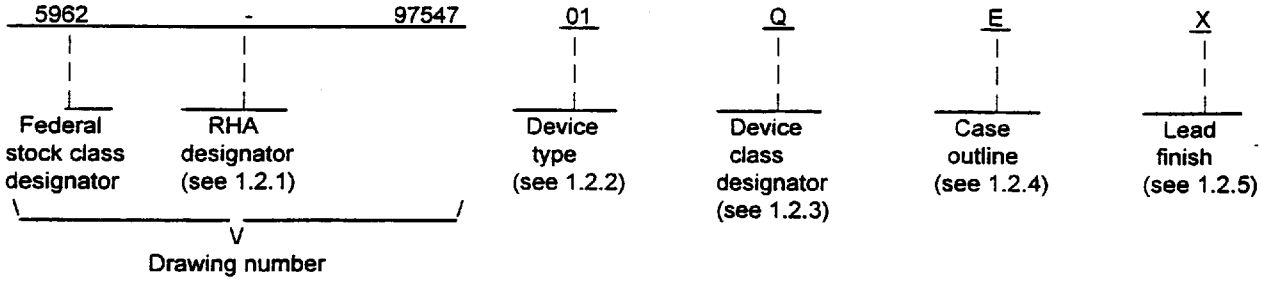
1.1 Scope. This drawing documents two product assurance class levels consisting of high reliability (device classes Q and M) and space application (device class V). A choice of case outlines and lead finishes are available and are reflected in the Part or Identifying Number (PIN). When available, a choice of Radiation Hardness Assurance (RHA) levels are reflected in the PIN.

1.2 PIN. The PIN is as shown in the following example:




1.2.1 RHA designator. Device classes Q and V RHA marked devices meet the MIL-PRF-38535 specified RHA levels and are marked with the appropriate RHA designator. Device class M RHA marked devices meet the MIL-PRF-38535, appendix A specified RHA levels and are marked with the appropriate RHA designator. A dash (-) indicates a non-RHA device.

1.2.2 Device type(s). The device type(s) identify the circuit function as follows:

| Device type | Generic number | Circuit function |
|---|---|---|
| 01 | 54LS85 | 4-bit magnitude comparators |

1.2.3 Device class designator. The device class designator is a single letter identifying the product assurance level as follows:

| Device class | Device requirements documentation |
|---|---|
| M | Vendor self-certification to the requirements for MIL-STD-883 compliant, non-JAN class level B microcircuits in accordance with MIL-PRF-38535, appendix A |
| Q or V | Certification and qualification to MIL-PRF-38535 |

1.2.4 Case outline(s). The case outline(s) are as designated in MIL-STD-1835 and as follows:

| Outline letter | Descriptive designator | Terminals | Package style |
|---|---|---|---|
| E | GDIP1-T16 or CDIP2-T16 | 16 | Dual-in-line |
| F | GDFP2-F16 or CDFP3-F16 | 16 | Flat pack |
| 2 | CQCC1-N20 | 20 | Square chip carrier |

1.2.5 Lead finish. The lead finish is as specified in MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.



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1.3 Absolute maximum ratings. 1/ 2/ 3/

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| | |
|---|---|
| Supply voltage range ($V_{CC}$) | 7.0 V dc |
| Input voltage | 7.0 V dc |
| Operating free-air temperature range | -55° C to +125° C |
| Maximum power dissipation ($P_D$) | 140 mW |
| Storage temperature range | -65° C to +150° C |
| Thermal resistance, junction-to-case ($\Theta_{JC}$) | See MIL-STD-1835 |
| Junction temperature ($T_J$) | 150° C |

1.4 Recommended operating conditions. 2/ 3/

| | |
|---|---|
| Supply voltage range ($V_{CC}$) | +4.5 V dc to +5.5 V dc |
| Minimum high level input voltage ($V_{IH}$) | +2.0 V |
| Maximum low level input voltage ($V_{IL}$) | +0.7 V |
| Maximum high level output current ($I_{OH}$) | -400 µA |
| Maximum low level output current ($I_{OL}$) | +4 mA |
| Case operating temperature range ($T_C$) | -55° C to +125° C |

1.5 Digital logic testing for device classes Q and V.

| | |
|---|---|
| Fault coverage measurement of manufacturing logic tests (MIL-STD-883, test method 5011) | XX percent 4/ |

2. APPLICABLE DOCUMENTS

2.1 Government specification, standards, and handbooks. The following specification, standards, and handbooks form a part of this drawing to the extent specified herein. Unless otherwise specified, the issues of these documents are those listed in the issue of the Department of Defense Index of Specifications and Standards (DoDISS) and supplement thereto, cited in the solicitation.

SPECIFICATION

MILITARY

MIL-PRF-38535 - Integrated Circuits, Manufacturing, General Specification for.

STANDARDS

MILITARY

MIL-STD-883 - Test Methods and Procedures for Microelectronics.
MIL-STD-973 - Configuration Management.
MIL-STD-1835 - Microcircuit Case Outlines.

HANDBOOKS

MILITARY

MIL-HDBK-103 - List of Standard Microcircuit Drawings (SMD's).
MIL-HDBK-780 - Standard Microcircuit Drawings.

(Unless otherwise indicated, copies of the specification, standards, and handbooks are available from the Standardization Document Order Desk, 700 Robbins Avenue, Building 4D, Philadelphia, PA 19111-5094.)

1/ Stresses above the absolute maximum rating may cause permanent damage to the device. Extended operation at the maximum levels may degrade performance and affect reliability.

2/ Unless otherwise noted, all voltages are referenced to GND.

3/ The limits for the parameters specified herein shall apply over the full specified $V_{CC}$ range and case temperature range of -55° C to +125° C. Unused inputs must be held high or low.

4/ Values will be added when they become available.



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2.2 Order of precedence. In the event of a conflict between the text of this drawing and the references cited herein, the text of this drawing takes precedence. Nothing in this document, however, supersedes applicable laws and regulations unless a specific exemption has been obtained.

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3. REQUIREMENTS

3.1 Item requirements. The individual item requirements for device classes Q and V shall be in accordance with MIL-PRF-38535 and as specified herein or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. The individual item requirements for device class M shall be in accordance with MIL-PRF-38535, appendix A for non-JAN class level B devices and as specified herein.

3.2 Design, construction, and physical dimensions. The design, construction, and physical dimensions shall be as specified in MIL-PRF-38535 and herein for device classes Q and V or MIL-PRF-38535, appendix A and herein for device class M.

3.2.1 Terminal connections. The terminal connections shall be as specified on figure 1.

3.2.2 Truth table. The truth table shall be as specified on figure 2.

3.2.3 Test circuit and timing waveforms. The block or logic diagram(s) shall be as specified on figure 3.

3.3 Electrical performance characteristics and postirradiation parameter limits. Unless otherwise specified herein, the electrical performance characteristics and postirradiation parameter limits are as specified in table I and shall apply over the full case operating temperature range.

3.4 Electrical test requirements. The electrical test requirements shall be the subgroups specified in table II. The electrical tests for each subgroup are defined in table I.

3.5 Marking. The part shall be marked with the PIN listed in 1.2 herein. In addition, the manufacturer's PIN may also be marked as listed in MIL-HDBK-103. For packages where marking of the entire SMD PIN number is not feasible due to space limitations, the manufacturer has the option of not marking the "5962-" on the device. For RHA product using this option, the RHA designator shall still be marked. Marking for device classes Q and V shall be in accordance with MIL-PRF-38535. Marking for device class M shall be in accordance with MIL-PRF-38535, appendix A.

3.5.1 Certification/compliance mark. The certification mark for device classes Q and V shall be a "QML" or "Q" as required in MIL-PRF-38535. The compliance mark for device class M shall be a "C" as required in MIL-PRF-38535, appendix A.

3.6 Certificate of compliance. For device classes Q and V, a certificate of compliance shall be required from a QML-38535 listed manufacturer in order to supply to the requirements of this drawing (see 6.6.1 herein). For device class M, a certificate of compliance shall be required from a manufacturer in order to be listed as an approved source of supply in MIL-HDBK-103 (see 6.6.2 herein). The certificate of compliance submitted to DSCC-VA prior to listing as an approved source of supply for this drawing shall affirm that the manufacturer's product meets, for device classes Q and V, the requirements of MIL-PRF-38535 and herein or for device class M, the requirements of MIL-PRF-38535, appendix A and herein.

3.7 Certificate of conformance. A certificate of conformance as required for device classes Q and V in MIL-PRF-38535 or for device class M in MIL-PRF-38535, appendix A shall be provided with each lot of microcircuits delivered to this drawing.

3.8 Notification of change for device class M. For device class M, notification to DSCC-VA of change of product (see 6.2 herein) involving devices acquired to this drawing is required for any change as defined in MIL-STD-973.

3.9 Verification and review for device class M. For device class M, DSCC, DSCC's agent, and the acquiring activity retain the option to review the manufacturer's facility and applicable required documentation. Offshore documentation shall be made available onshore at the option of the reviewer.

3.10 Microcircuit group assignment for device class M. Device class M devices covered by this drawing shall be in microcircuit group number 101 (see MIL-PRF-38535, appendix A).



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TABLE I. Electrical performance characteristics.

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| Test | | Symbol | Conditions $-55°C \le T_C \le +125°C$ $4.5\ V \le V_{CC} \le 5.5\ V$ unless otherwise specified | $V_{CC}$ | Group A subgroups | Limits 1/ | | Unit |
|---|---|---|---|---|---|---|---|---|
| | | | | | | Min | Max | |
| Input clamp voltage | | $V_{IK}$ | $I_I$ = -18mA | 4.5 V | 1, 2, 3 | | -1.5 | V |
| Short circuit output current | | $I_{OS}$ 2/ | | 5.5 V | 1, 2, 3 | -20 | -100 | mA |
| High level output voltage | | $V_{OH}$ | $V_{IL}$ = 0.7 V, $I_{OH}$ = -400 µA $V_{IH}$ = 2 V | 4.5 V | 1, 2, 3 | 2.5 | | V |
| Low level output voltage | | $V_{OL}$ | $V_{IH}$ = 2 V, $I_{OL}$ = 4 mA, $V_{IL}$ = 0.7 V | 4.5 V | 1, 2, 3 | | 0.4 | V |
| Input current at maximum input voltage | A<B, A>B inputs | $I_I$ | $V_I$ = 7 V | 5.5 V | 1, 2, 3 | | 0.1 | mA |
| | all other inputs | $I_I$ | $V_I$ = 7 V | 5.5 V | 1, 2, 3 | | 0.3 | mA |
| High-level input current | A<B, A>B inputs | $I_{IH}$ | $V_I$ = 2.7 V | 5.5 V | 1, 2, 3 | | 20 | µA |
| | all other inputs | $I_{IH}$ | $V_I$ = 2.7 V | 5.5 V | 1, 2, 3 | | 60 | µA |
| Low-level input current | A<B, A>B inputs | $I_{IL}$ | $V_I$ = 0.4 V | 5.5 V | 1, 2, 3 | | -0.4 | mA |
| | all other inputs | $I_{IL}$ | $V_I$ = 0.4 V | 5.5 V | 1, 2, 3 | | -1.2 | mA |
| Supply current | | $I_{CC}$ | $V_I$ = 4.5 V 3/ | 5.5 V | 1, 2, 3 | | 20 | mA |
| Functional test | | 4/ | $V_{IN} = V_{IH}$ Min or $V_{IL}$ Max Verify output $V_O$ See 4.4.1b | 4.5 V | 7, 8 | L | H | |
| | | | | 5.5 V | 7, 8 | L | H | |

See footnotes at end of table.



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TABLE I. Electrical performance characteristics - Continued.

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| Test | Symbol | Conditions -55°C ≤ TC ≤ +125°C 4.5 V ≤ VCC ≤ 5.5 V unless otherwise specified | To Output | Number of gate levels | Limits 1/ Min | Limits 1/ Max | Unit |
|---|---|---|---|---|---|---|---|
| Propagation delay time, low-to-high-level output Any A or B data input | $t_{PLH}$ | Group A Subgroup = 9 | A < B, A > B | 1 | | 36 | ns |
| | | | | 2 | | 36 | |
| | | | | 3 | | 36 | |
| | | $V_{CC}$ = 5 V | A = B | 4 | | 45 | |
| Propagation delay time, high-to-low level output Any A or B data input | $t_{PHL}$ | $T_A$ = 25 V | A < B, A > B | 1 | | 30 | ns |
| | | $C_L$ = 15 pF, | | 2 | | 30 | |
| | | $R_L$ = 2 kΩ, See Note 5 | | 3 | | 30 | |
| | | | A = B | 4 | | 45 | |
| Propagation delay time, low-to-high-level output, A < B or A = B input | $t_{PLH}$ | | A > B | 1 | | 22 | ns |
| Propagation delay time, high-to-low-level output, A < B or A = B input | $t_{PHL}$ | | A > B | 1 | | 17 | ns |
| Propagation delay time, low-to-high-level output, A = B input | $t_{PLH}$ | | A = B | 2 | | 20 | ns |
| Propagation delay time, high-to-low-level output, A = B input | $t_{PHL}$ | | A = B | 2 | | 26 | ns |
| Propagation delay time, low-to-high-level output, A > B or A = B input | $t_{PLH}$ | | A < B | 1 | | 22 | ns |
| Propagation delay time, high-to-low-level output, A > B or A = B input | $t_{PHL}$ | | A < B | 1 | | 17 | ns |

See footnotes of following page.



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1/ For negative and positive voltage and current values, the sign designates the potential difference in reference to GND and the direction of current flow, respectively, and the absolute value of the magnitude, not the sign, is relative to the minimum and maximum limits, as applicable, listed herein.

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2/ Not more than one output should be shorted at a time, and the duration of the short-circuit should not exceed one second.

3/ $I_{CC}$ is measured with outputs open, A = B grounded, and all other inputs at 4.5 V.

4/ Tests shall be performed in sequence, attributes data only. Functional tests shall include the truth table and other logic patterns used for fault detection. The test vectors used to verify the truth table shall, at a minimum, test all functions of each input and output. All possible input to output logic patterns per function shall be guaranteed, if not tested, to the truth table in figure 2 herein. Functional tests shall be performed in sequence as approved by the qualifying activity on qualified devices. Allowable tolerances per MIL-STD-883 may be incorporated. For outputs L ≤ 0.8 V, H ≥ 2.0 V.

5/ Test circuit and timing waveforms are shown in Figure 4.

| Device type | 01 | |
|---|---|---|
| Case outlines | E and F | 2 |
| Terminal number | Terminal symbol | |
| 1 | B3 | NC |
| 2 | A<Bin | B3 |
| 3 | A=Bin | A<Bin |
| 4 | A>Bin | A=Bin |
| 5 | A>Bout | A>Bin |
| 6 | A=Bout | NC |
| 7 | A<Bout | A>Bout |
| 8 | GND | A=Bout |
| 9 | B0 | A<Bout |
| 10 | A0 | GND |
| 11 | B1 | NC |
| 12 | A1 | B0 |
| 13 | A2 | A0 |
| 14 | B2 | B1 |
| 15 | A3 | A1 |
| 16 | $V_{CC}$ | NC |
| 17 | — | A2 |
| 18 | — | B2 |
| 19 | — | A3 |
| 20 | — | $V_{CC}$ |

NC = No connection

FIGURE 1. Terminal connections.



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| COMPARING INPUTS | | | | CASCADING INPUTS | | | OUTPUTS | | |
|---|---|---|---|---|---|---|---|---|---|
| A3, B3 | A2, B2 | A1, B1 | A0, B0 | A > B | A < B | A = B | A > B | A < B | A = B |
| A3 > B3 | X | X | X | X | X | X | H | L | L |
| A3 < B3 | X | X | X | X | X | X | L | H | L |
| A3 = B3 | A2 > B2 | X | X | X | X | X | H | L | L |
| A3 = B3 | A2 < B2 | X | X | X | X | X | L | H | L |
| A3 = B2 | A2 = B2 | A1 > B1 | X | X | X | X | H | L | L |
| A3 = B3 | A2 = B2 | A1 < B1 | X | X | X | X | L | H | L |
| A2 = B3 | A2 = B2 | A1 = B1 | A0 > B0 | X | X | X | H | L | L |
| A3 = B3 | A2 = B2 | A1 = B1 | A0 < B0 | X | X | X | L | H | L |
| A3 = B3 | A2 = B2 | A1 = B1 | A0 = B0 | H | L | L | H | L | L |
| A3 = B3 | A2 = B2 | A1 = B1 | A0 = B0 | L | H | L | L | H | L |
| A3 = B3 | A2 = B2 | A1 = B1 | A0 = B0 | X | X | H | L | L | H |
| A3 = B3 | A2 = B2 | A1 = B1 | A0 = BO | H | H | L | L | L | L |
| A3 = B3 | A2 = B2 | A1 = B1 | A0 = B0 | L | L | L | H | H | L |

H = High level voltage
L = Low level voltage
X = Irrelevant

FIGURE 2. Truth table.



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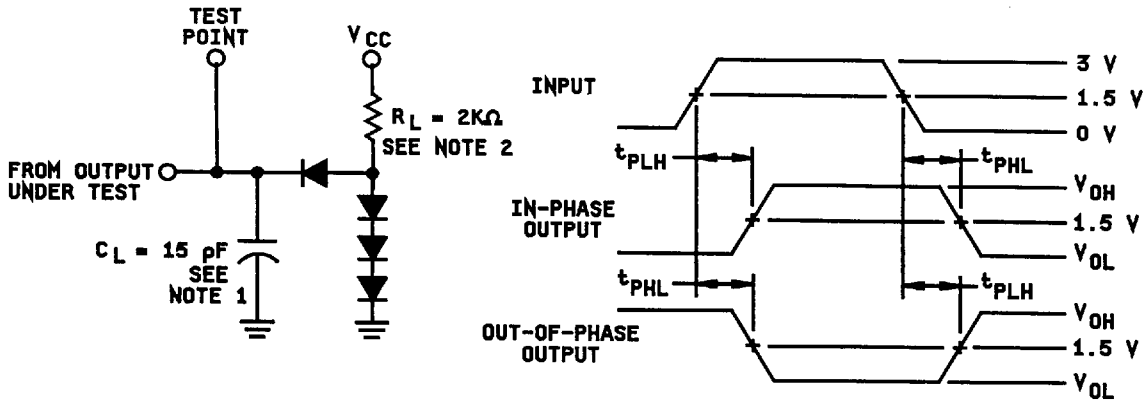


NOTES: 1. $C_L$ includes probe and jig capacitance.
2. All diodes are 1N3064 or equivalent

FIGURE 3. Test circuit and timing waveforms.



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4. QUALITY ASSURANCE PROVISIONS

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4.1 Sampling and inspection. For device classes Q and V, sampling and inspection procedures shall be in accordance with MIL-PRF-38535 or as modified in the device manufacturer's Quality Management (QM) plan. The modification in the QM plan shall not affect the form, fit, or function as described herein. For device class M, sampling and inspection procedures shall be in accordance with MIL-PRF-38535, appendix A.

4.2 Screening. For device classes Q and V, screening shall be in accordance with MIL-PRF-38535, and shall be conducted on all devices prior to qualification and technology conformance inspection. For device class M, screening shall be in accordance with method 5004 of MIL-STD-883, and shall be conducted on all devices prior to quality conformance inspection.

4.2.1 Additional criteria for device class M.

a. Burn-in test, method 1015 of MIL-STD-883.

(1) Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015.

(2) $T_A$ = +125°C, minimum.

b. Interim and final electrical test parameters shall be as specified in table II herein.

4.2.2 Additional criteria for device classes Q and V.

a. The burn-in test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The burn-in test circuit shall be maintained under document revision level control of the device manufacturer's Technology Review Board (TRB) in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1015 of MIL-STD-883.

b. Interim and final electrical test parameters shall be as specified in table II herein.

c. Additional screening for device class V beyond the requirements of device class Q shall be as specified in MIL-PRF-38535, appendix B.

4.3 Qualification inspection for device classes Q and V. Qualification inspection for device classes Q and V shall be in accordance with MIL-PRF-38535. Inspections to be performed shall be those specified in MIL-PRF-38535 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4 Conformance inspection. Technology conformance inspection for classes Q and V shall be in accordance with MIL-PRF-38535 including groups A, B, C, D, and E inspections and as specified herein except where option 2 of MIL-PRF-38535 permits alternate in-line control testing. Quality conformance inspection for device class M shall be in accordance with MIL-PRF-38535, appendix A and as specified herein. Inspections to be performed for device class M shall be those specified in method 5005 of MIL-STD-883 and herein for groups A, B, C, D, and E inspections (see 4.4.1 through 4.4.4).

4.4.1 Group A inspection.

a. Tests shall be as specified in table II herein.

b. For device class M, subgroups 7 and 8 tests shall be sufficient to verify the truth table. For device classes Q and V, subgroups 7 and 8 shall include verifying the functionality of the device; these tests shall have been fault graded in accordance with MIL-STD-883, test method 5012 (see 1.5 herein).



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TABLE II. Electrical test requirements.

| Test requirements | Subgroups (in accordance with MIL-STD-883, method 5005, table I) | Subgroups (in accordance with MIL-PRF-38535, table III) | |
|---|---|---|---|
| | Device class M | Device class Q | Device class V |
| Interim electrical parameters (see 4.2) | - - - | - - - | - - - |
| Final electrical parameters (see 4.2) | 1/ 1, 2, 3, 7, 8, 9 | 1/ 1, 2, 3, 7,8, 9 | 2/ 1, 2, 3, 7,8, 9 |
| Group A test requirements (see 4.4) | 1, 2, 3, 7, 8, 9 | 1, 2, 3, 7, 8, 9 | 1, 2, 3, 7, 8, 9 |
| Group C end-point electrical parameters (see 4.4) | 1, 2, 3 | 1, 2, 3 | 1, 2, 3, 7, 8, 9 |
| Group D end-point electrical parameters (see 4.4) | 1, 2, 3 | 1, 2, 3 | 1, 2, 3 |
| Group E end-point electrical parameters (see 4.4) | 1, 7, 9 | 1, 7, 9 | 1, 7, 9 |

1/ PDA applies to subgroup 1.
2/ PDA applies to subgroups 1 and 7.

4.4.2 Group C inspection. The group C inspection end-point electrical parameters shall be as specified in table II herein.

4.4.2.1 Additional criteria for device class M. Steady-state life test conditions, method 1005 of MIL-STD-883:

a. Test condition A, B, C, or D. The test circuit shall be maintained by the manufacturer under document revision level control and shall be made available to the preparing or acquiring activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

b. $T_A$ = +125°C, minimum.

c. Test duration: 1,000 hours, except as permitted by method 1005 of MIL-STD-883.

4.4.2.2 Additional criteria for device classes Q and V. The steady-state life test duration, test condition and test temperature, or approved alternatives shall be as specified in the device manufacturer's QM plan in accordance with MIL-PRF-38535. The test circuit shall be maintained under document revision level control by the device manufacturer's TRB in accordance with MIL-PRF-38535 and shall be made available to the acquiring or preparing activity upon request. The test circuit shall specify the inputs, outputs, biases, and power dissipation, as applicable, in accordance with the intent specified in test method 1005 of MIL-STD-883.

4.4.3 Group D inspection. The group D inspection end-point electrical parameters shall be as specified in table II herein.



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4.4.4 Group E inspection. Group E inspection is required only for parts intended to be marked as radiation hardness assured (see 3.5 herein).

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a. End-point electrical parameters shall be as specified in table II herein.

b. For device classes Q and V, the devices or test vehicle shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535 for the RHA level being tested. For device class M, the devices shall be subjected to radiation hardness assured tests as specified in MIL-PRF-38535, appendix A for the RHA level being tested. All device classes must meet the postirradiation end-point electrical parameter limits as defined in table I at $T_A$ = +25°C ±5°C, after exposure, to the subgroups specified in table II herein.

c. When specified in the purchase order or contract, a copy of the RHA delta limits shall be supplied.

5. PACKAGING

5.1 Packaging requirements. The requirements for packaging shall be in accordance with MIL-PRF-38535 for device classes Q and V or MIL-PRF-38535, appendix A for device class M.

6. NOTES

6.1 Intended use. Microcircuits conforming to this drawing are intended for use for Government microcircuit applications (original equipment), design applications, and logistics purposes.

6.1.1 Replaceability. Microcircuits covered by this drawing will replace the same generic device covered by a contractor-prepared specification or drawing.

6.1.2 Substitutability. Device class Q devices will replace device class M devices.

6.2 Configuration control of SMD's. All proposed changes to existing SMD's will be coordinated with the users of record for the individual documents. This coordination will be accomplished in accordance with MIL-STD-973 using DD Form 1692, Engineering Change Proposal.

6.3 Record of users. Military and industrial users should inform Defense Supply Center Columbus when a system application requires configuration control and which SMD's are applicable to that system. DSCC will maintain a record of users and this list will be used for coordination and distribution of changes to the drawings. Users of drawings covering microelectronic devices (FSC 5962) should contact DSCC-VA, telephone (614) 692-0525.

6.4 Comments. Comments on this drawing should be directed to DSCC-VA , Columbus, Ohio 43216-5000, or telephone (614) 692-0674.

6.5 Abbreviations, symbols, and definitions. The abbreviations, symbols, and definitions used herein are defined in MIL-PRF-38535 and MIL-HDBK-1331.

6.6 Sources of supply.

6.6.1 Sources of supply for device classes Q and V. Sources of supply for device classes Q and V are listed in QML-38535. The vendors listed in QML-38535 have submitted a certificate of compliance (see 3.6 herein) to DSCC-VA and have agreed to this drawing.

6.6.2 Approved sources of supply for device class M. Approved sources of supply for class M are listed in MIL-HDBK-103. The vendors listed in MIL-HDBK-103 have agreed to this drawing and a certificate of compliance (see 3.6 herein) has been submitted to and accepted by DSCC-VA.



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查询"5962-9754701Q2A"供应商

STANDARD MICROCIRCUIT DRAWING BULLETIN

DATE: 97-3-14

Approved sources of supply for SMD 5962-97547 are listed below for immediate acquisition information only and shall be added to MIL-HDBK-103 and QML-38535 during the next revision. MIL-HDBK-103 and QML-38535 will be revised to include the addition or deletion of sources. The vendors listed below have agreed to this drawing and a certificate of compliance has been submitted to and accepted by DSCC-VA. This bulletin is superseded by the next dated revision of MIL-HDBK-103 and QML-38535.

| Standard microcircuit drawing PIN 1/ | Vendor CAGE number | Vendor similar PIN 2/ |
|---|---|---|
| 5962-9754701QEA | 01295 | SNJ54LS85J |
| 5962-9754701QFA | 01295 | SNJ54LS85W |
| 5962-9754701Q2A | 01295 | SNJ54LS85FK |

1/ The lead finish shown for each PIN representing a hermetic package is the most readily available from the manufacturer listed for that part. The device manufacturers listed herein are authorized to supply alternate lead finishes "A", "B", or "C" at their discretion. Contact the listed approved source of supply for further information.

2/ Caution. Do not use this number for item acquisition. Items acquired to this number may not satisfy the performance requirements of this drawing.

| Vendor CAGE number | Vendor name and address |
|---|---|
| 01295 | Texas Instruments Incorporated<br>13500 N. Central Expressway<br>P.O. Box 655303<br>Dallas, TX 75265<br>Point of contact:<br>I-20 at FM 1788<br>Midland, TX 79711-0448 |

The information contained herein is disseminated for convenience only and the Government assumes no liability whatsoever for any inaccuracies in the information bulletin.

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