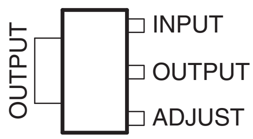
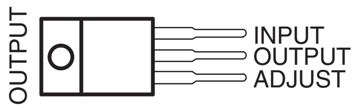
FEATURES

- **Output Voltage Range Adjustable From 1.25 V to 37 V**
- **Output Current Greater Than 1.5 A**
- **Internal Short-Circuit Current Limiting**
- **Thermal Overload Protection**
- **Output Safe-Area Compensation**

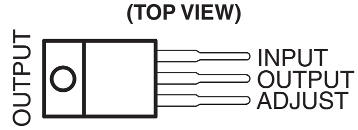
DCY (SOT-223) PACKAGE (TOP VIEW)



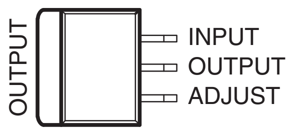
KC (TO-220) PACKAGE (TOP VIEW)



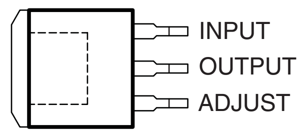
KCS (TO-220) PACKAGE (TOP VIEW)



KTE PACKAGE (TOP VIEW)



KTT (TO-263) PACKAGE (TOP VIEW)



DESCRIPTION/ORDERING INFORMATION

The LM317 is an adjustable three-terminal positive-voltage regulator capable of supplying more than 1.5 A over an output-voltage range of 1.25 V to 37 V. It is exceptionally easy to use and requires only two external resistors to set the output voltage. Furthermore, both line and load regulation are better than standard fixed regulators.

In addition to having higher performance than fixed regulators, this device includes on-chip current limiting, thermal overload protection, and safe operating-area protection. All overload protection remains fully functional, even if the ADJUST terminal is disconnected.

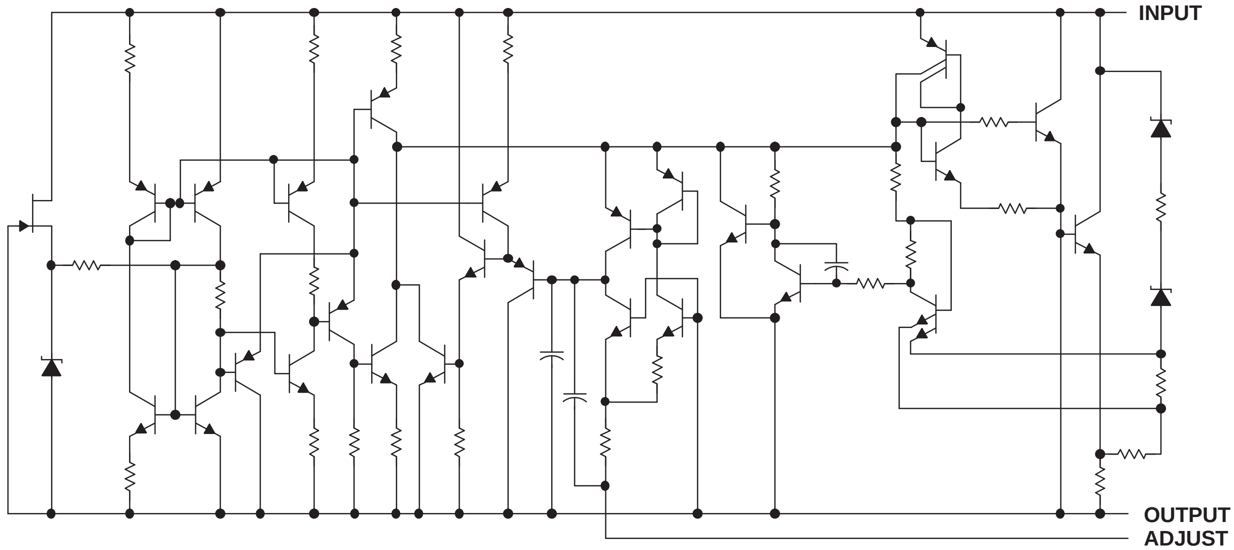
The LM317 is versatile in its applications, including uses in programmable output regulation and local on-card regulation. Or, by connecting a fixed resistor between the ADJUST and OUTPUT terminals, the LM317 can function as a precision current regulator. An optional output capacitor can be added to improve transient response. The ADJUST terminal can be bypassed to achieve very high ripple-rejection ratios, which are difficult to achieve with standard three-terminal regulators.

ORDERING INFORMATION(1)

T_A	PACKAGE(2)		ORDERABLE PART NUMBER	TOP-SIDE MARKING
0°C to 125°C	PowerFLEX™ – KTE	Reel of 2000	LM317KTER	LM317
	SOT-223 – DCY	Tube of 80	LM317DCY	L3
		Reel of 2500	LM317DCYR	
	TO-220 – KC	Tube of 50	LM317KC	LM317
	TO-220, short shoulder – KCS	Tube of 20	LM317KCS	
	TO-263 – KTT	Reel of 500	LM317KTTR	LM317

(1) For the most current package and ordering information, see the Package Option Addendum at the end of this document, or see the TI web site at www.ti.com.
(2) Package drawings, standard packing quantities, thermal data, symbolization, and PCB design guidelines are available at www.ti.com/sc/package.

SCHEMATIC DIAGRAM



Absolute Maximum Ratings[1]

over virtual junction temperature range (unless otherwise noted)

		MIN	MAX	UNIT
$V_I - V_O$	Input-to-output differential voltage		40	V
T_J	Operating virtual junction temperature		150	°C
	Lead temperature 1,6 mm (1/16 in) from case for 10 s		260	°C
T_{stg}	Storage temperature range	–65	150	°C

(1) Stresses beyond those listed under "absolute maximum ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.

Package Thermal Data[1]

PACKAGE	BOARD	θ_{JA}	θ_{JC}	θ_{JP}[2]
PowerFLEX™ (KTE)	High K, JESD 51-5	23°C/W	3°C/W	
SOT-223 (DCY)	High K, JESD 51-7	53°C/W	30.6°C/W	
TO-220 (KC/KCS)	High K, JESD 51-5	19°C/W	17°C/W	3°C/W
TO-263 (KTT)	High K, JESD 51-5	25.3°C/W	18°C/W	1.94°C/W

(1) Maximum power dissipation is a function of T_J(max), θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) - T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.
(2) For packages with exposed thermal pads, such as QFN, PowerPAD™, or PowerFLEX™, θ_{JP} is defined as the thermal resistance between the die junction and the bottom of the exposed pad.

Recommended Operating Conditions

		MIN	MAX	UNIT
$V_I - V_O$	Input-to-output differential voltage	3	40	V
I_O	Output current		1.5	A
T_J	Operating virtual junction temperature	0	125	°C

Electrical Characteristics

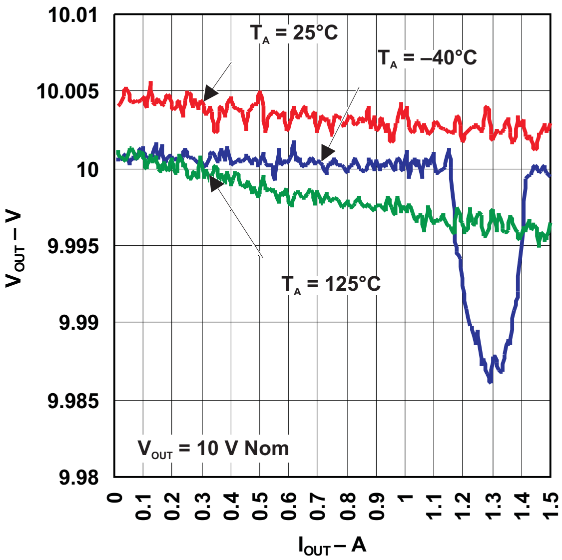
over recommended ranges of operating virtual junction temperature (unless otherwise noted)

PARAMETER	TEST CONDITIONS(1)			MIN	TYP	MAX	UNIT
Line regulation(2)	$V_I - V_O$ = 3 V to 40 V		T_J = 25°C		0.01	0.04	%/V
			T_J = 0°C to 125°C		0.02	0.07	
Load regulation	I_O = 10 mA to 1500 mA	C_{ADJ} = 10 µF,(3) T_J = 25°C	$V_O \le 5$ V			25	mV
			$V_O \ge 5$ V		0.1	0.5	$\%V_O$
		T_J = 0°C to 125°C	$V_O \le 5$ V		20	70	mV
			$V_O \ge 5$ V		0.3	1.5	$\%V_O$
Thermal regulation	20-ms pulse,	T_J = 25°C			0.03	0.07	$\%V_O$/W
ADJUST terminal current					50	100	µA
Change in ADJUST terminal current	$V_I - V_O$ = 2.5 V to 40 V, $P_D \le 20$ W, I_O = 10 mA to 1500 mA				0.2	5	µA
Reference voltage	$V_I - V_O$ = 3 V to 40 V, $P_D \le 20$ W, I_O = 10 mA to 1500 mA			1.2	1.25	1.3	V
Output-voltage temperature stability	T_J = 0°C to 125°C				0.7		$\%V_O$
Minimum load current to maintain regulation	$V_I - V_O$ = 40 V				3.5	10	mA
Maximum output current	$V_I - V_O \le 15$ V,	$P_D < P_{MAX}$(4)		1.5	2.2		A
	$V_I - V_O \le 40$ V,	$P_D < P_{MAX}$(4),	T_J = 25°C	0.15	0.4		
RMS output noise voltage (% of V_O)	f = 10 Hz to 10 kHz,	T_J = 25°C			0.003		$\%V_O$
Ripple rejection	V_O = 10 V,	f = 120 Hz	C_{ADJ} = 0 µF(3)		57		dB
			C_{ADJ} = 10 µF(3)	62	64		
Long-term stability	T_J = 25°C				0.3	1	%/1k hr

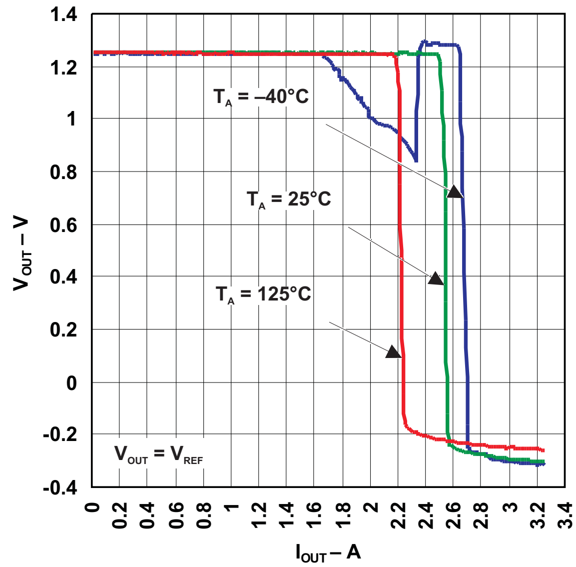
(1) Unless otherwise noted, the following test conditions apply: $|V_I - V_O|$ = 5 V and I_{OMAX} = 1.5 A, T_J = 0°C to 125°C. Pulse testing techniques are used to maintain the junction temperature as close to the ambient temperature as possible.
(2) Line regulation is expressed here as the percentage change in output voltage per 1-V change at the input.
(3) C_{ADJ} is connected between the ADJUST terminal and GND.
(4) Maximum power dissipation is a function of T_J(max), θ_{JA}, and T_A. The maximum allowable power dissipation at any allowable ambient temperature is $P_D = (T_J(max) - T_A)/\theta_{JA}$. Operating at the absolute maximum T_J of 150°C can affect reliability.

TYPICAL CHARACTERISTICS

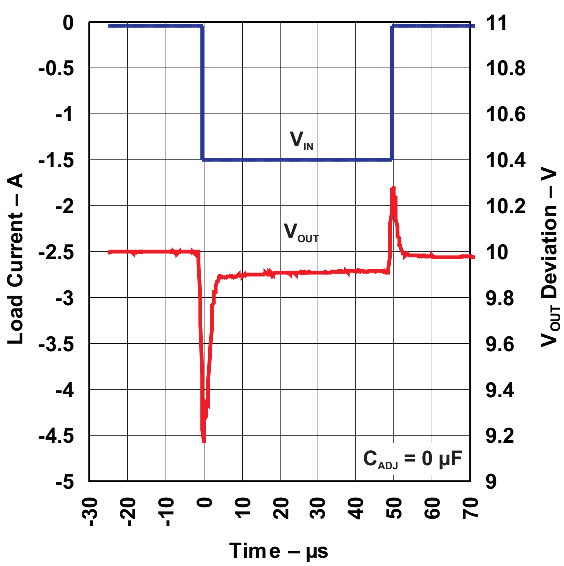
LOAD REGULATION



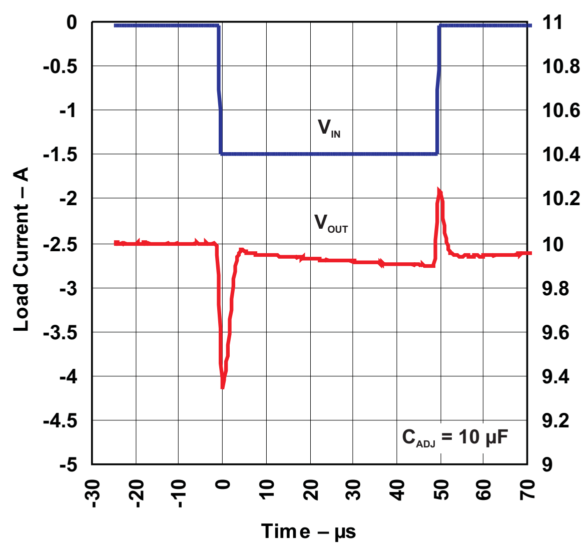
LOAD REGULATION



LOAD TRANSIENT RESPONSE

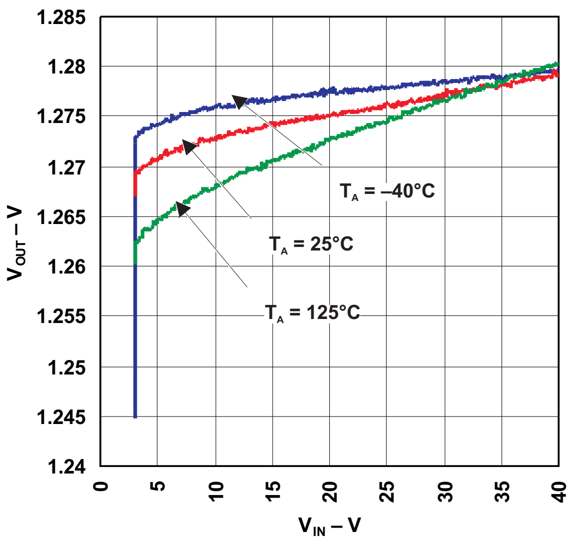


LOAD TRANSIENT RESPONSE

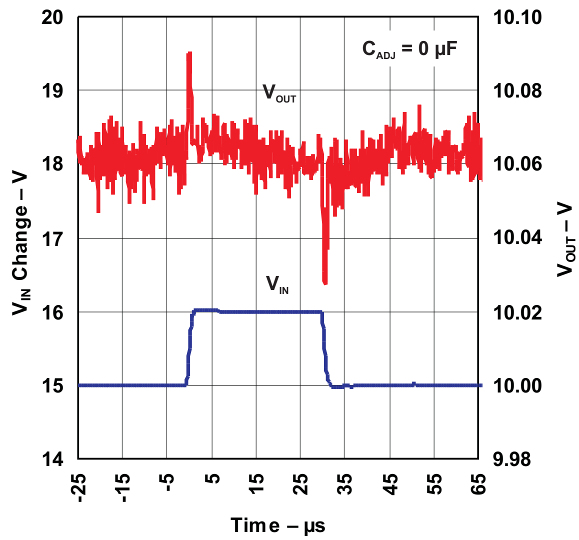


TYPICAL CHARACTERISTICS (continued)

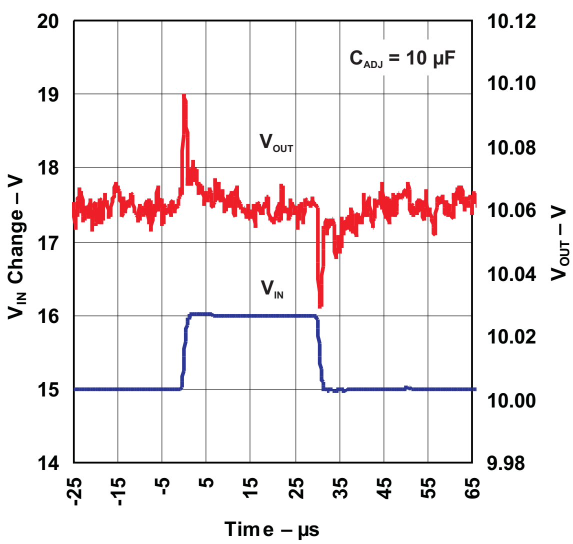
LINE REGULATION



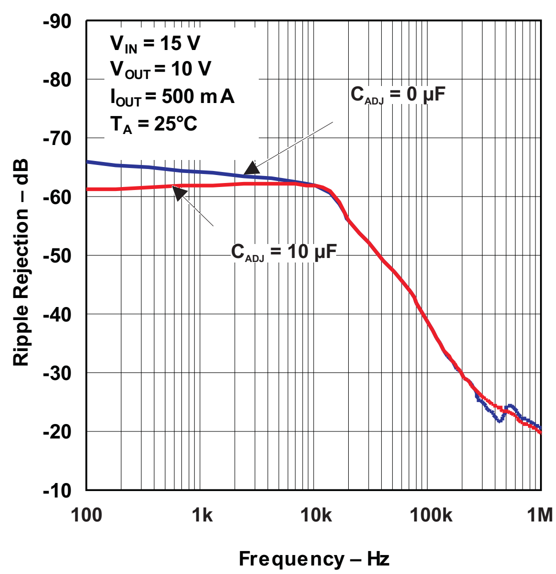
LINE TRANSIENT RESPONSE



LINE TRANSIENT RESPONSE

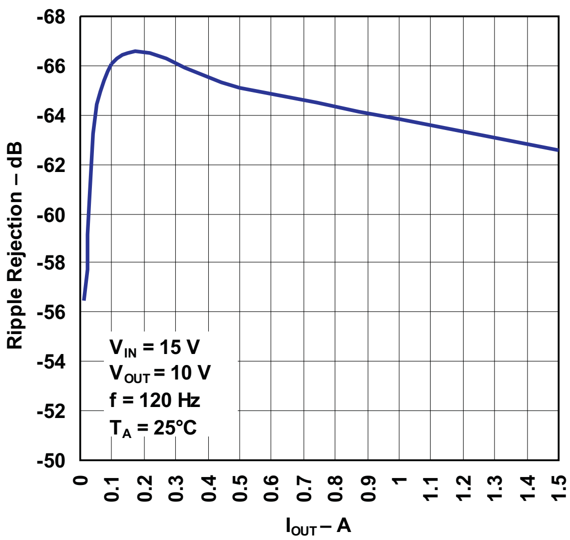


RIPPLE REJECTION
vs
FREQUENCY

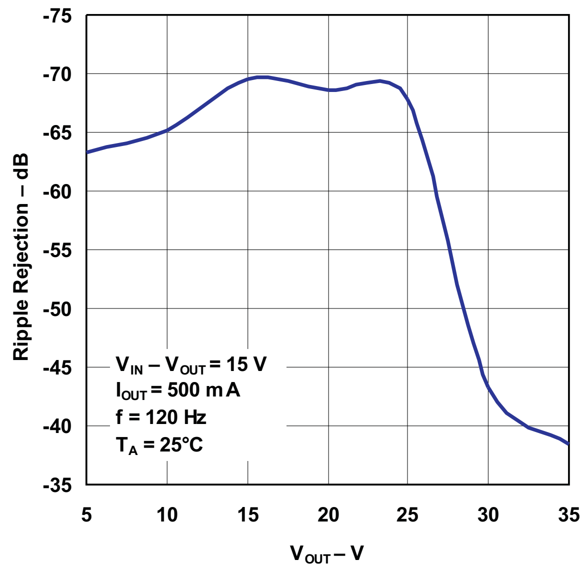


TYPICAL CHARACTERISTICS (continued)

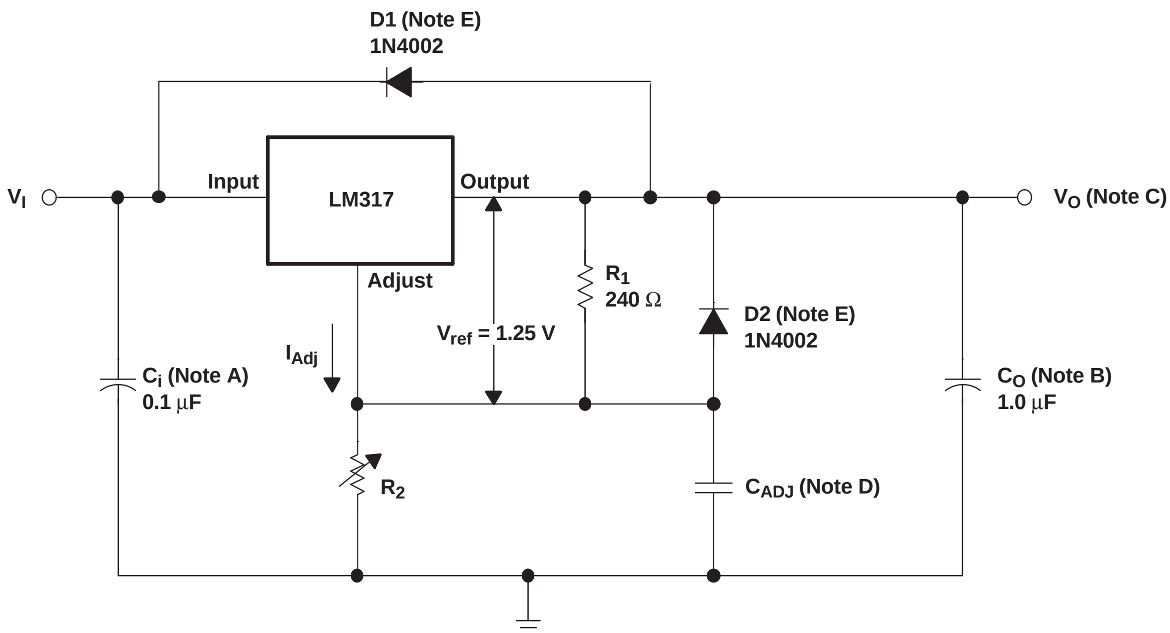
RIPPLE REJECTION
vs
OUTPUT CURRENT



RIPPLE REJECTION
vs
OUTPUT VOLTAGE



APPLICATION INFORMATION



NOTES: A. C_i is not required, but is recommended, particularly if the regulator is not in close proximity to the power-supply filter capacitors. A 0.1-µF disc or 1-µF tantalum provides sufficient bypassing for most applications, especially when adjustment and output capacitors are used.

B. C_O improves transient response, but is not needed for stability.

C. V_O is calculated as shown:

$$V_O = V_{ref}\left(1 + \frac{R_2}{R_1}\right) + (I_{Adj} \times R_2)$$

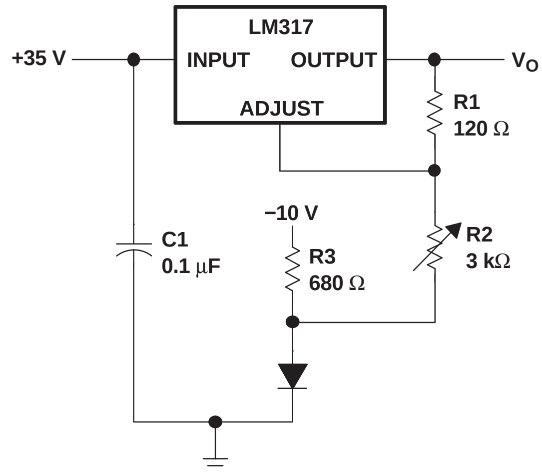
Because I_{Adj} typically is 50 µA, it is negligible in most applications.

D. C_{ADJ} is used to improve ripple rejection; it prevents amplification of the ripple as the output voltage is adjusted higher. If C_{ADJ} is used, it is best to include protection diodes.

E. If the input is shorted to ground during a fault condition, protection diodes provide measures to prevent the possibility of external capacitors discharging through low-impedance paths in the IC. By providing low-impedance discharge paths for C_O and C_{ADJ}, respectively, D1 and D2 prevent the capacitors from discharging into the output of the regulator.

Figure 1. Adjustable Voltage Regulator

APPLICATION INFORMATION (continued)

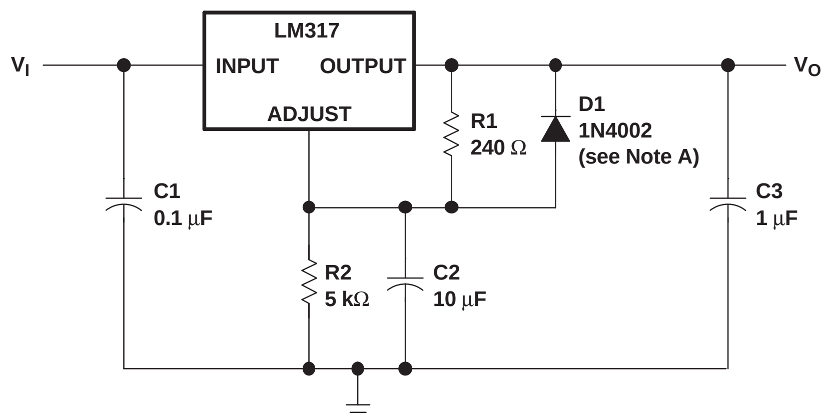


V_O is calculated as:

$$V_O = V_{ref}\left(1 + \frac{R2 + R3}{R1}\right) + I_{Adj}(R2 + R3) - 10\ V$$

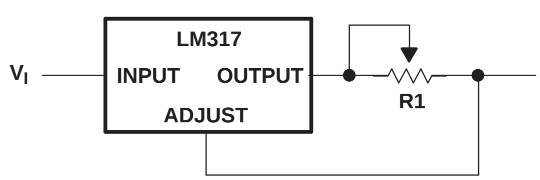
Since I_{Adj} typically is 50 µA, it is negligible in most applications.

Figure 2. 0-V to 30-V Regulator Circuit



NOTE A: D1 discharges C2 if the output is shorted to ground.

Figure 3. Adjustable Regulator Circuit With Improved Ripple Rejection



$I_{limit} = \frac{1.2}{R1}$

Figure 4. Precision Current-Limiter Circuit

APPLICATION INFORMATION (continued)

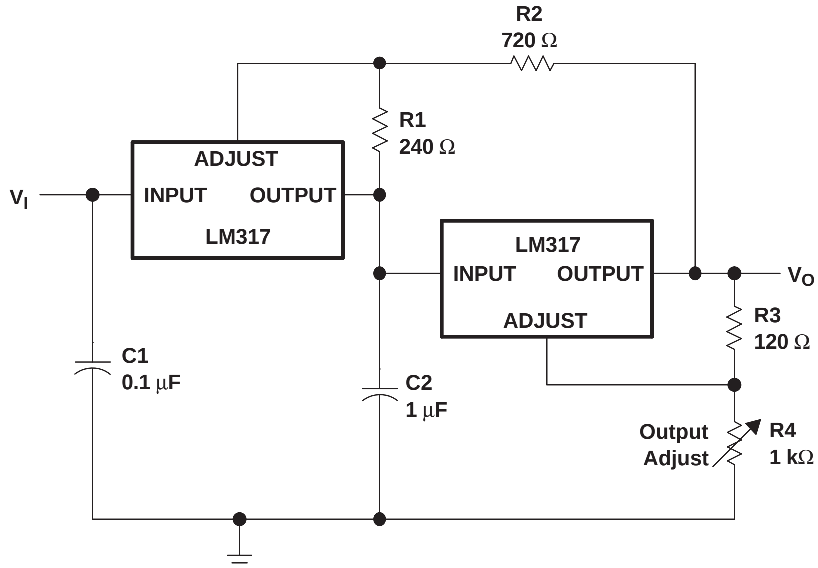


Figure 5. Tracking Preregulator Circuit

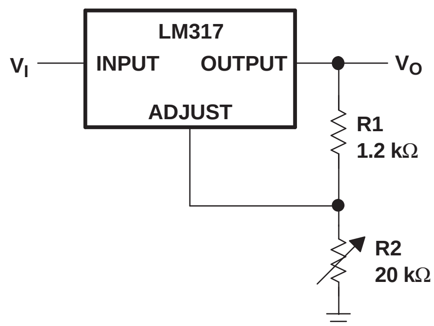
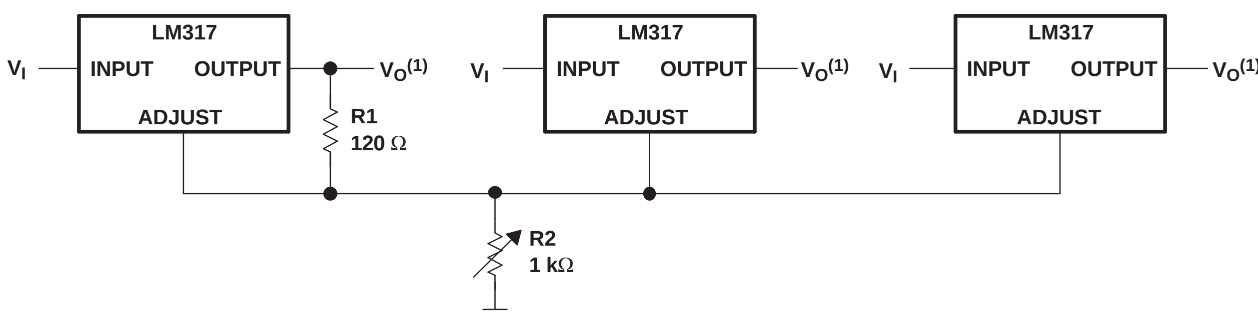


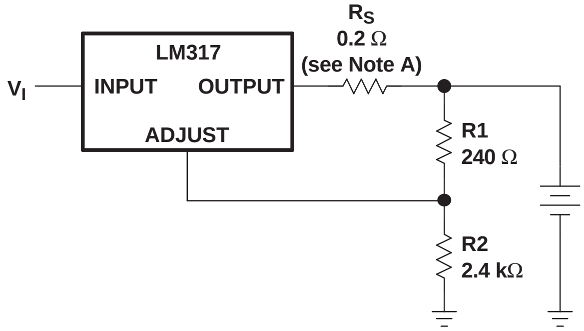
Figure 6. 1.25-V to 20-V Regulator Circuit With Minimum Program Current



(1) Minimum load current from each output is 10 mA. All output voltages are within 200 mV of each other.

Figure 7. Adjusting Multiple On-Card Regulators With a Single Control

APPLICATION INFORMATION (continued)



NOTE A: R_S controls the output impedance of the charger.

$$Z_{OUT} = R_S\left(1 + \frac{R2}{R1}\right)$$

The use of R_S allows for low charging rates with a fully charged battery.

Figure 8. Battery-Charger Circuit

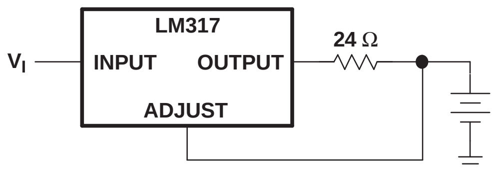


Figure 9. 50-mA Constant-Current Battery-Charger Circuit

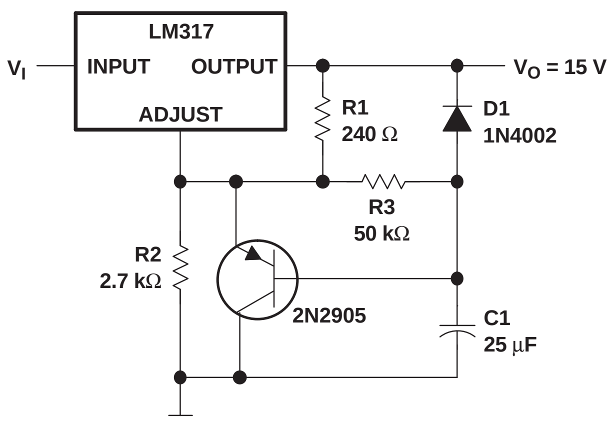


Figure 10. Slow Turn-On 15-V Regulator Circuit

APPLICATION INFORMATION (continued)

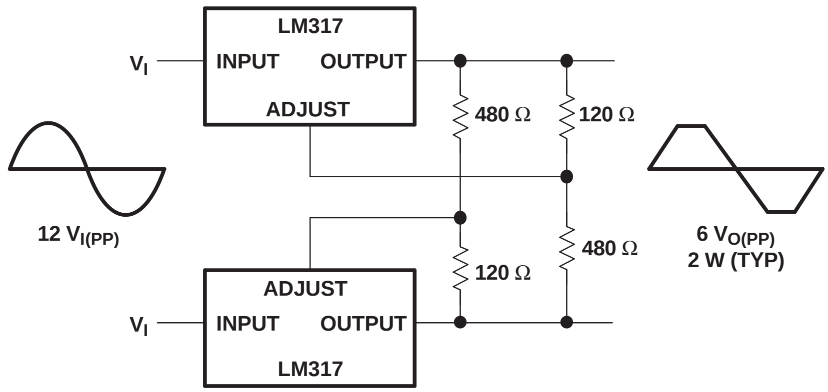
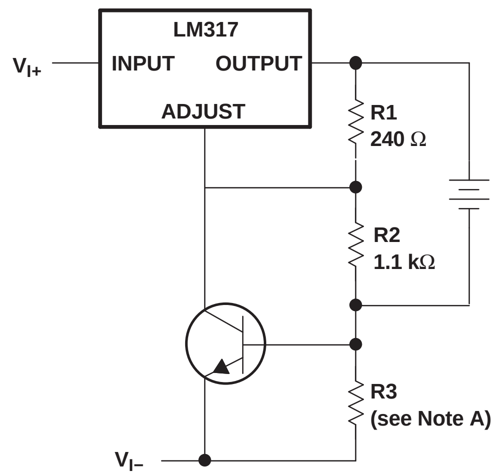


Figure 11. AC Voltage-Regulator Circuit



NOTE A: R3 sets the peak current (0.6 A for a 1-Ω resistor).

Figure 12. Current-Limited 6-V Charger Circuit

APPLICATION INFORMATION (continued)

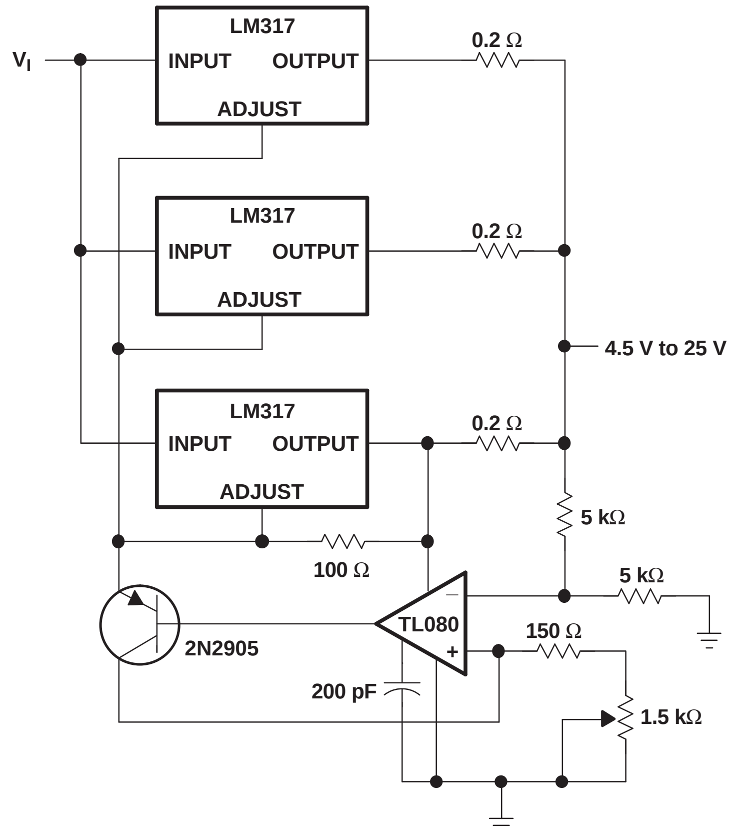
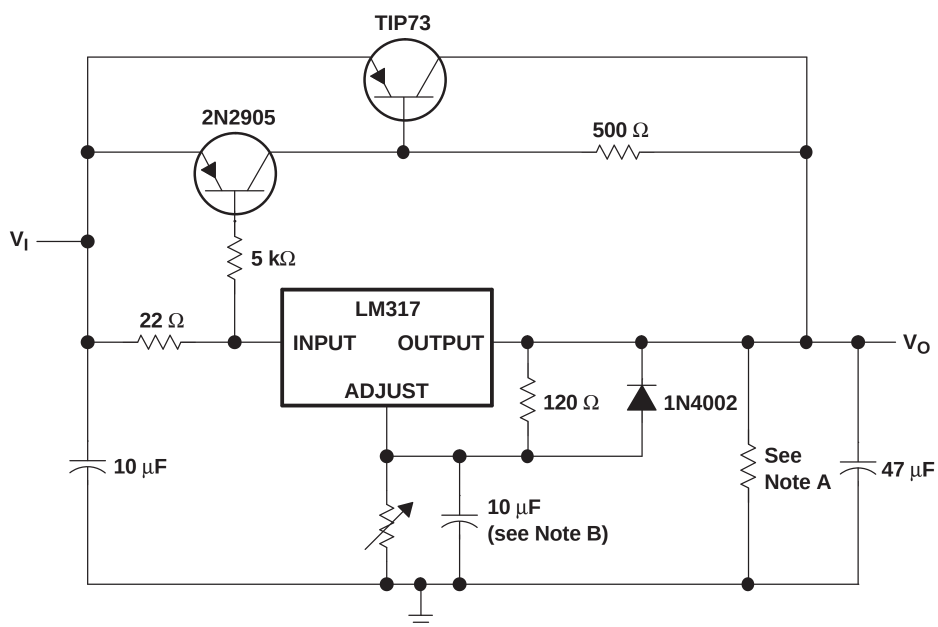


Figure 13. Adjustable 4-A Regulator Circuit



NOTES: A. The minimum load current is 30 mA.
B. This optional capacitor improves ripple rejection.

Figure 14. High-Current Adjustable Regulator Circuit

PACKAGING INFORMATION

Orderable Device	Status [1]	Package Type	Package Drawing	Pins	Package Qty	Eco Plan [2]	Lead/Ball Finish	MSL Peak Temp [3]
LM317DCY	ACTIVE	SOT-223	DCY	4	80	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1YEAR
LM317DCYG3	ACTIVE	SOT-223	DCY	4	80	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1YEAR
LM317DCYR	ACTIVE	SOT-223	DCY	4	2500	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1YEAR
LM317DCYRG3	ACTIVE	SOT-223	DCY	4	2500	Green (RoHS & no Sb/Br)	CU SN	Level-2-260C-1YEAR
LM317KC	NRND	TO-220	KC	3	50	Pb-Free (RoHS)	CU SN	N / A for Pkg Type
LM317KCE3	NRND	TO-220	KC	3	50	Pb-Free (RoHS)	CU SN	N / A for Pkg Type
LM317KCS	ACTIVE	TO-220	KCS	3	50	Pb-Free (RoHS)	CU SN	N / A for Pkg Type
LM317KTER	NRND	PFM	KTE	3	2000	TBD	CU SN	Level-3-240C-168 HR
LM317KTTR	ACTIVE	DDPAK/ TO-263	KTT	3	500	Green (RoHS & no Sb/Br)	CU SN	Level-3-245C-168 HR
LM317KTTRG3	ACTIVE	DDPAK/ TO-263	KTT	3	500	Green (RoHS & no Sb/Br)	CU SN	Level-3-245C-168 HR

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new design.
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.ti.com/productcontent for the latest availability information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all 6 substances, including the requirement that lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable for use in specified lead-free processes.
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package, or 2) lead-based die adhesive used between the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retardants (Br or Sb do not exceed 0.1% by weight in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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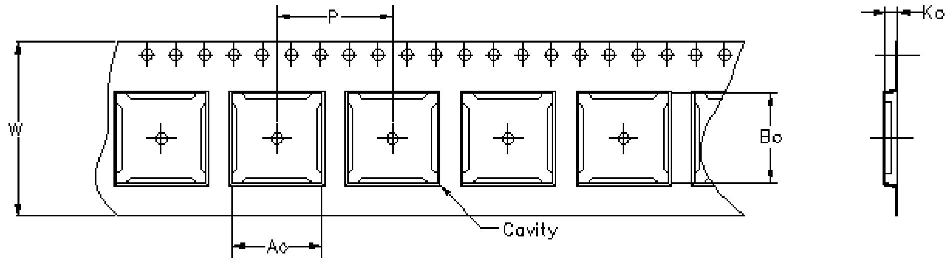
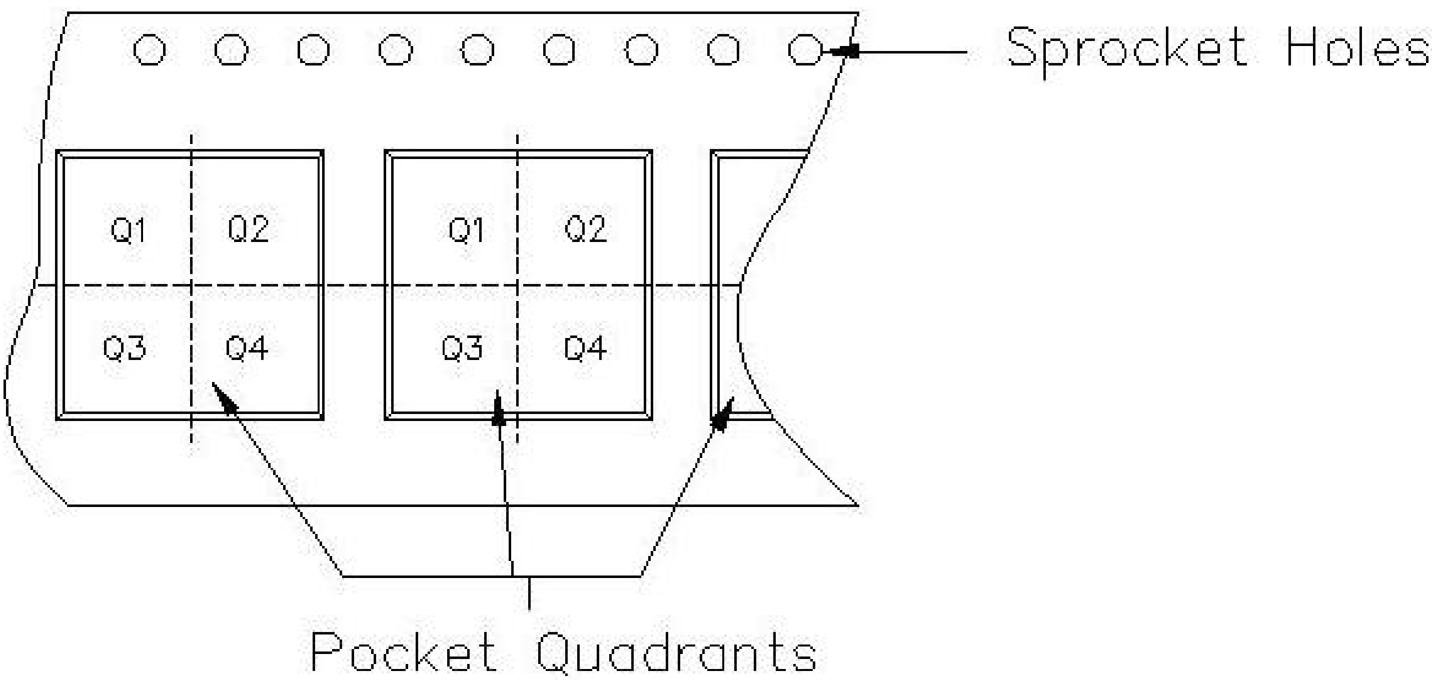
In no event shall TI's liability arising out of such information exceed the total purchase price of the TI part(s) at issue in this document sold by TI to Customer on an annual basis.



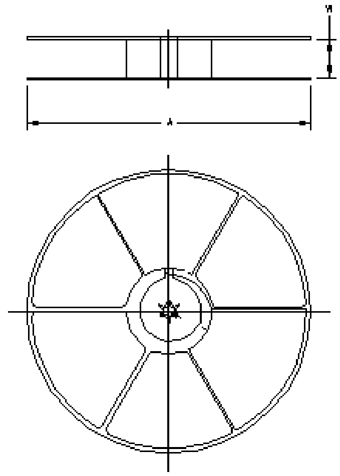
Carrier tape design is defined largely by the component lentgh, width, and thickness.

Ao =	Dimension designed to accommodate the component width.
Bo =	Dimension designed to accommodate the component length.
Ko =	Dimension designed to accommodate the component thickness.
W =	Overall width of the carrier tape.
P =	Pitch between successive cavity centers.



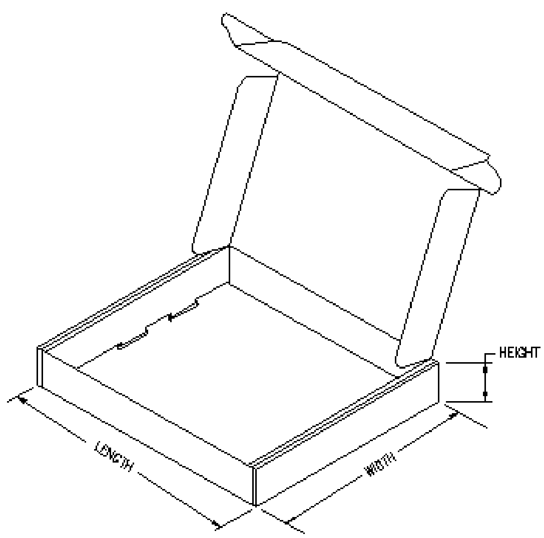
TAPE AND REEL INFORMATION

Device	Package	Pins	Site	Reel Diameter (mm)	Reel Width (mm)	A0 (mm)	B0 (mm)	K0 (mm)	P1 (mm)	W (mm)	Pin1 Quadrant
LM317KTER	KTE	3	SEM	0	0	9.8	11.0	2.45	12	24	NONE

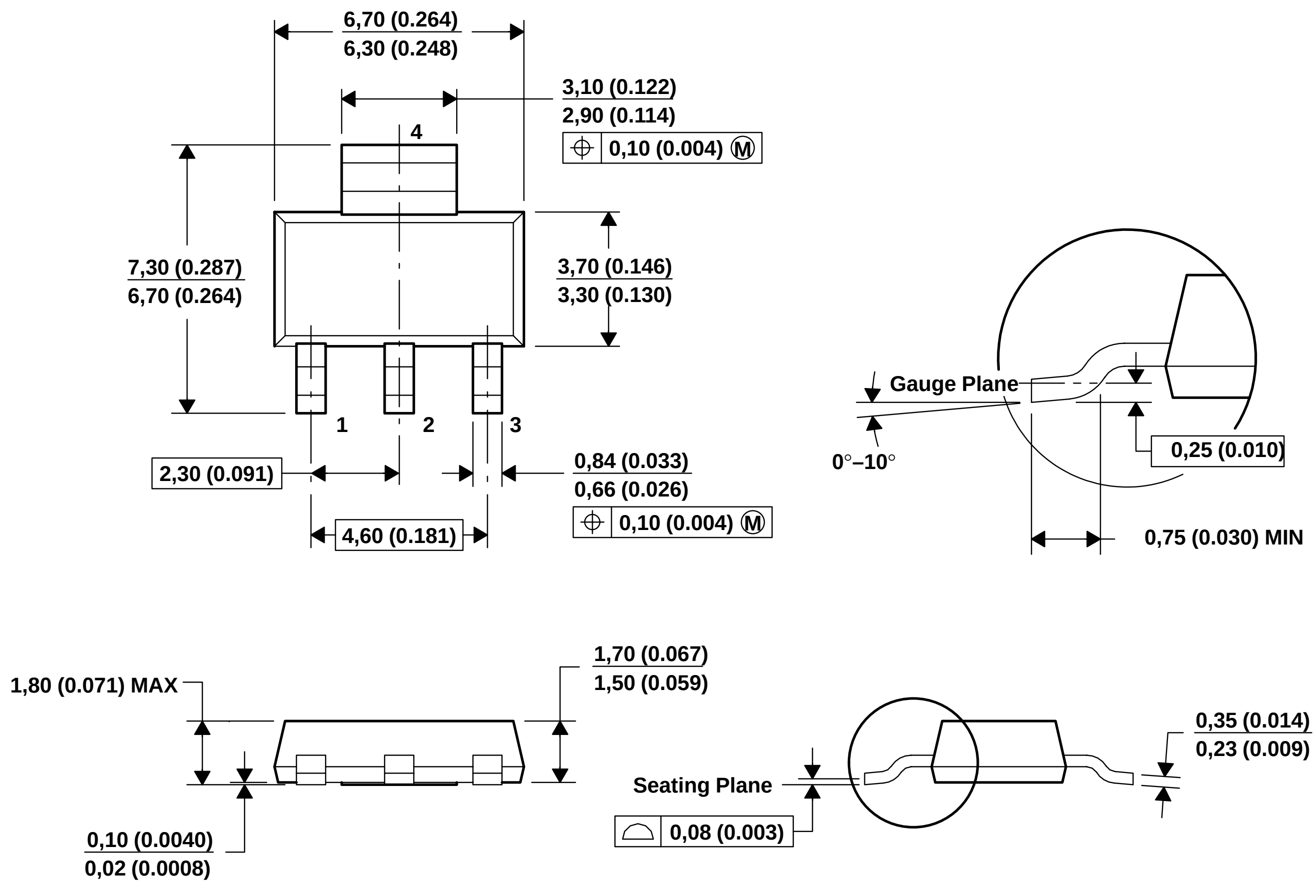


TAPE AND REEL BOX INFORMATION

Device	Package	Pins	Site	Length (mm)	Width (mm)	Height (mm)
LM317KTER	KTE	3	SEM	333.2	333.2	31.75



DCY (R-PDSO-G4) **PLASTIC SMALL-OUTLINE**

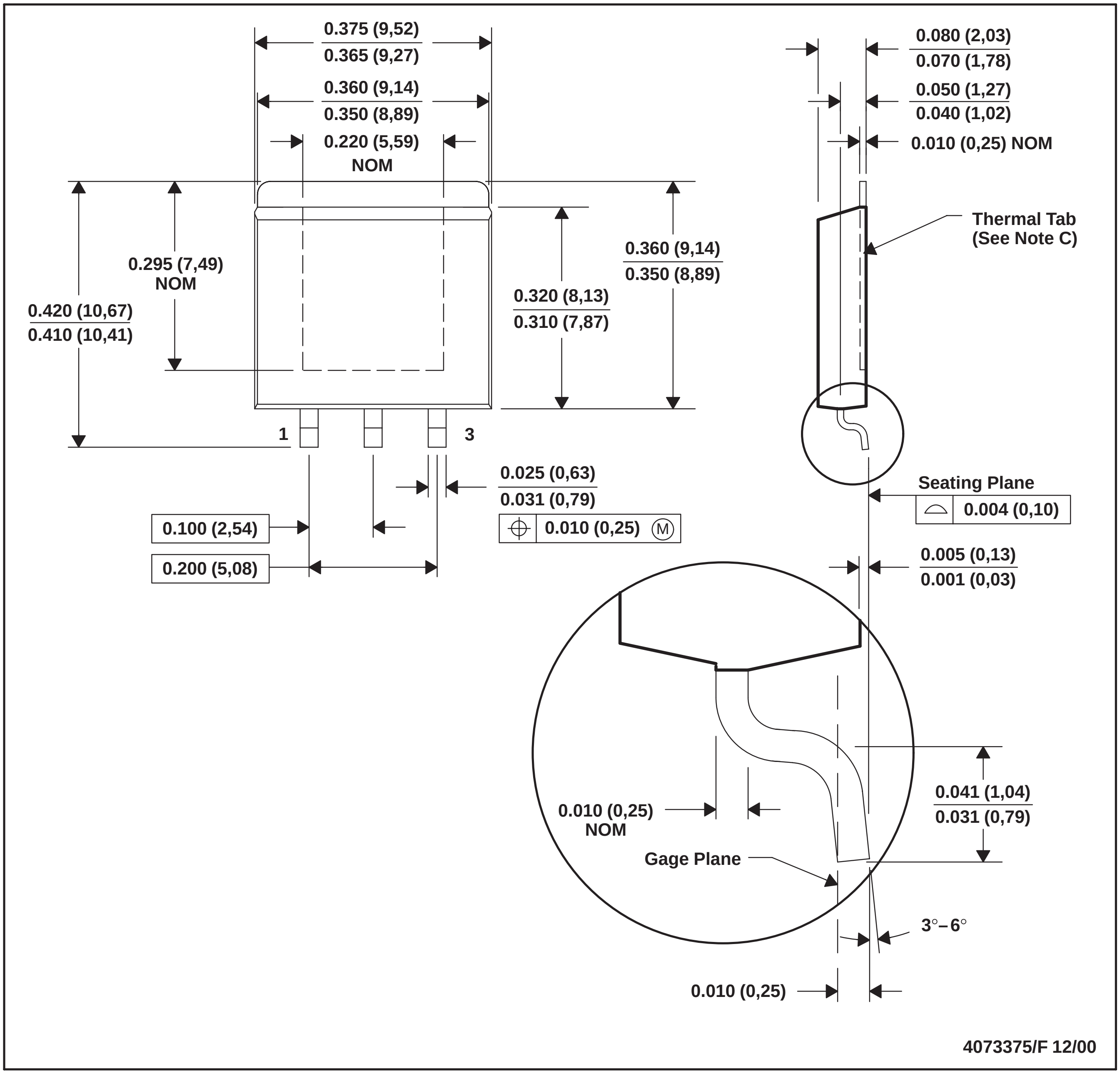


4202506/B 06/2002

NOTES: A. All linear dimensions are in millimeters (inches).
B. This drawing is subject to change without notice.
C. Body dimensions do not include mold flash or protrusion.
D. Falls within JEDEC TO-261 Variation AA.

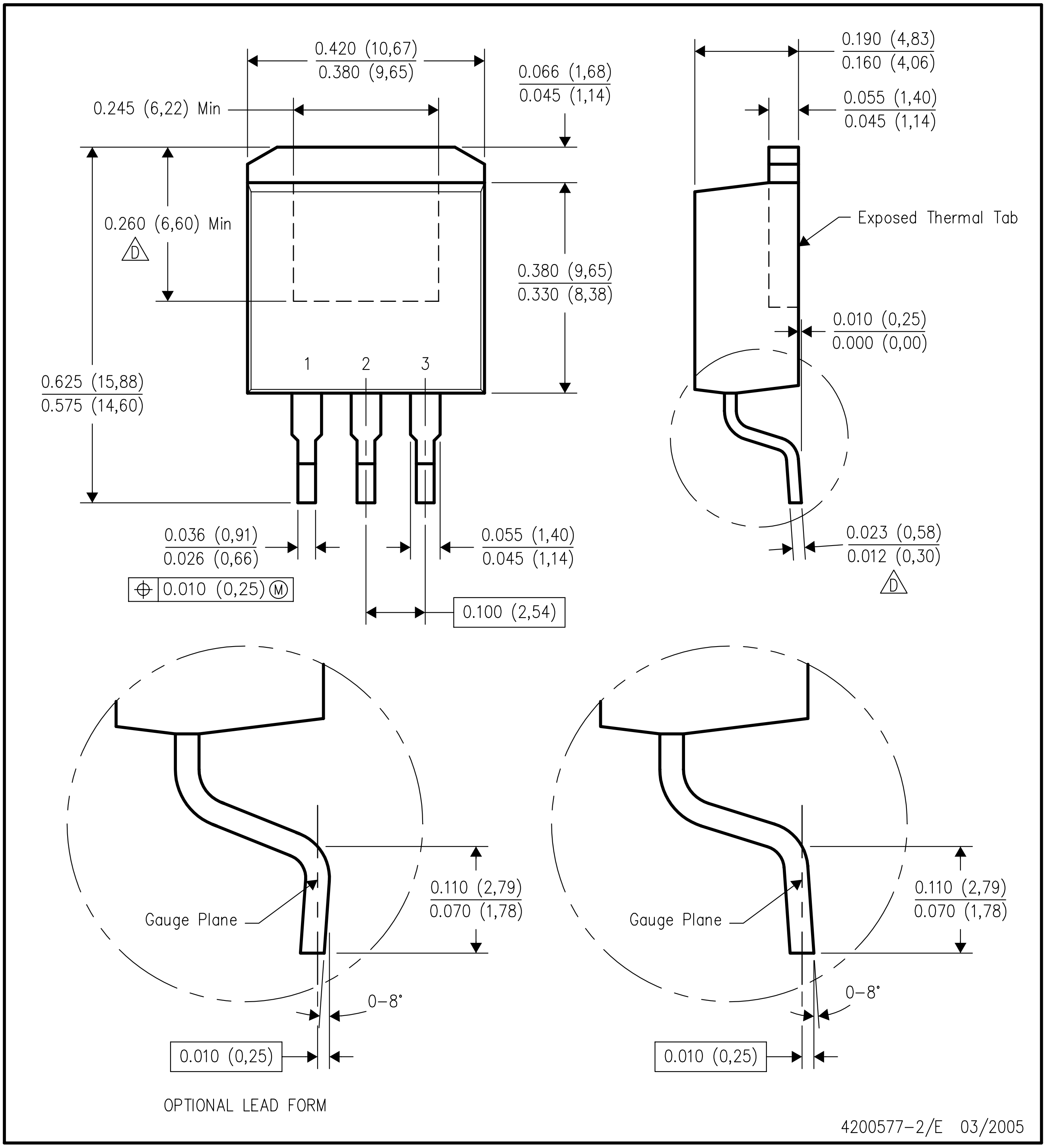
MPFM001E – OCTOBER 1994 – REVISED JANUARY 2001

KTE (R-PSFM-G3) **PowerFLEX™ PLASTIC FLANGE-MOUNT**



NOTES: A. All linear dimensions are in inches (millimeters).
B. This drawing is subject to change without notice.
C. The center lead is in electrical contact with the thermal tab.
D. Dimensions do not include mold protrusions, not to exceed 0.006 (0,15).
E. Falls within JEDEC MO-169

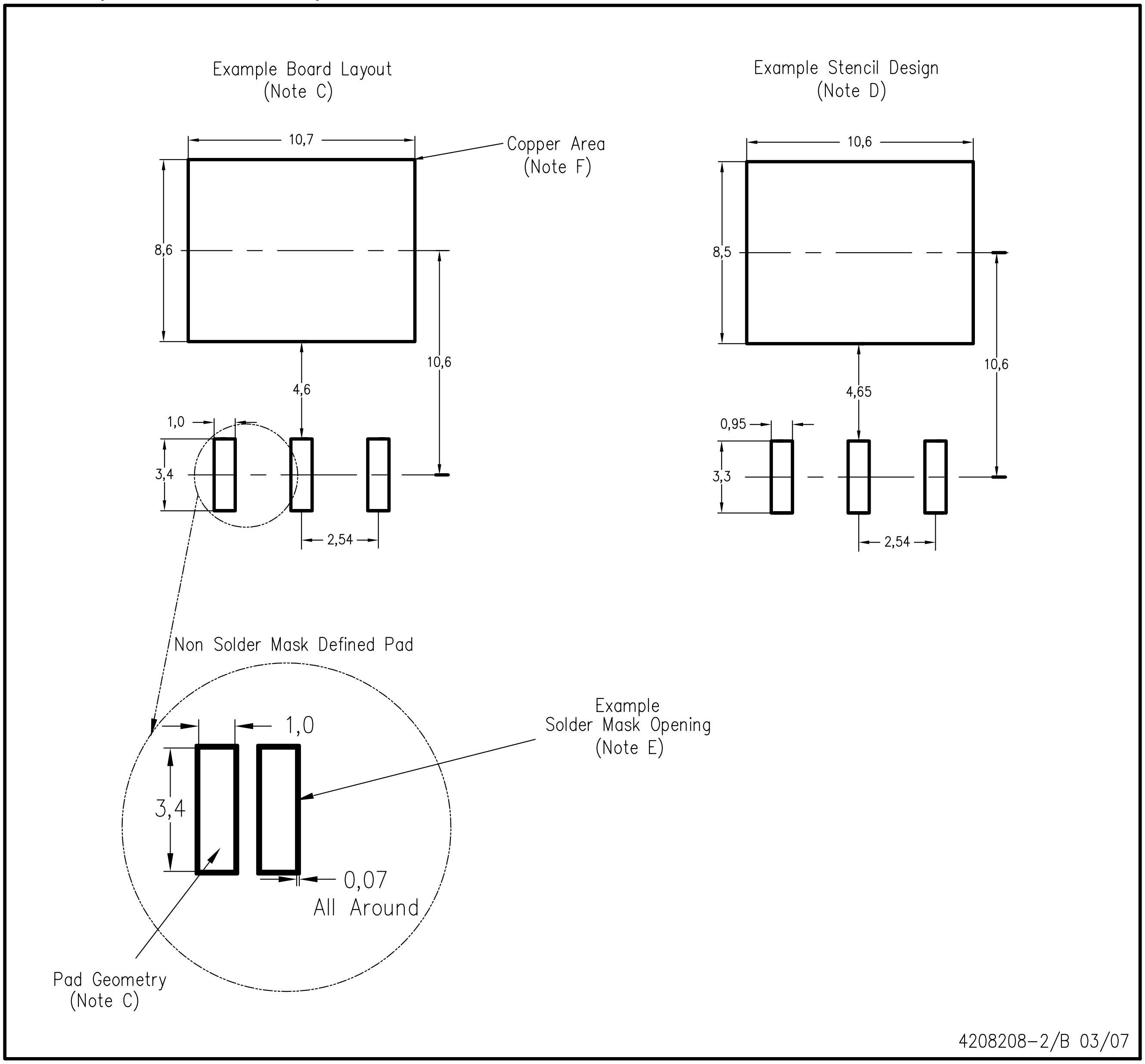
KTT (R–PSFM–G3) PLASTIC FLANGE–MOUNT PACKAGE



NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Body dimensions do not include mold flash or protrusion. Mold flash or protrusion not to exceed 0.005 (0,13) per side.
- D. Falls within JEDEC TO–263 variation AA, except minimum lead thickness and minimum exposed pad length.

查询"LM317DCYG3"供应商

KTT (R–PSFM–G3)



NOTES:
- A. All linear dimensions are in millimeters.
- B. This drawing is subject to change without notice.
- C. Publication IPC–SM–782 is recommended for alternate designs.
- D. Laser cutting apertures with trapezoidal walls and also rounding corners will offer better paste release. Customers should contact their board assembly site for stencil design recommendations. Refer to IPC–7525.
- E. Customers should contact their board fabrication site for solder mask tolerances between and around signal pads.
- F. This package is designed to be soldered to a thermal pad on the board. Refer to the Product Datasheet for specific thermal information, via requirements, and recommended thermal pad size. For thermal pad sizes larger than shown a solder mask defined pad is recommended in order to maintain the solderable pad geometry while increasing copper area.

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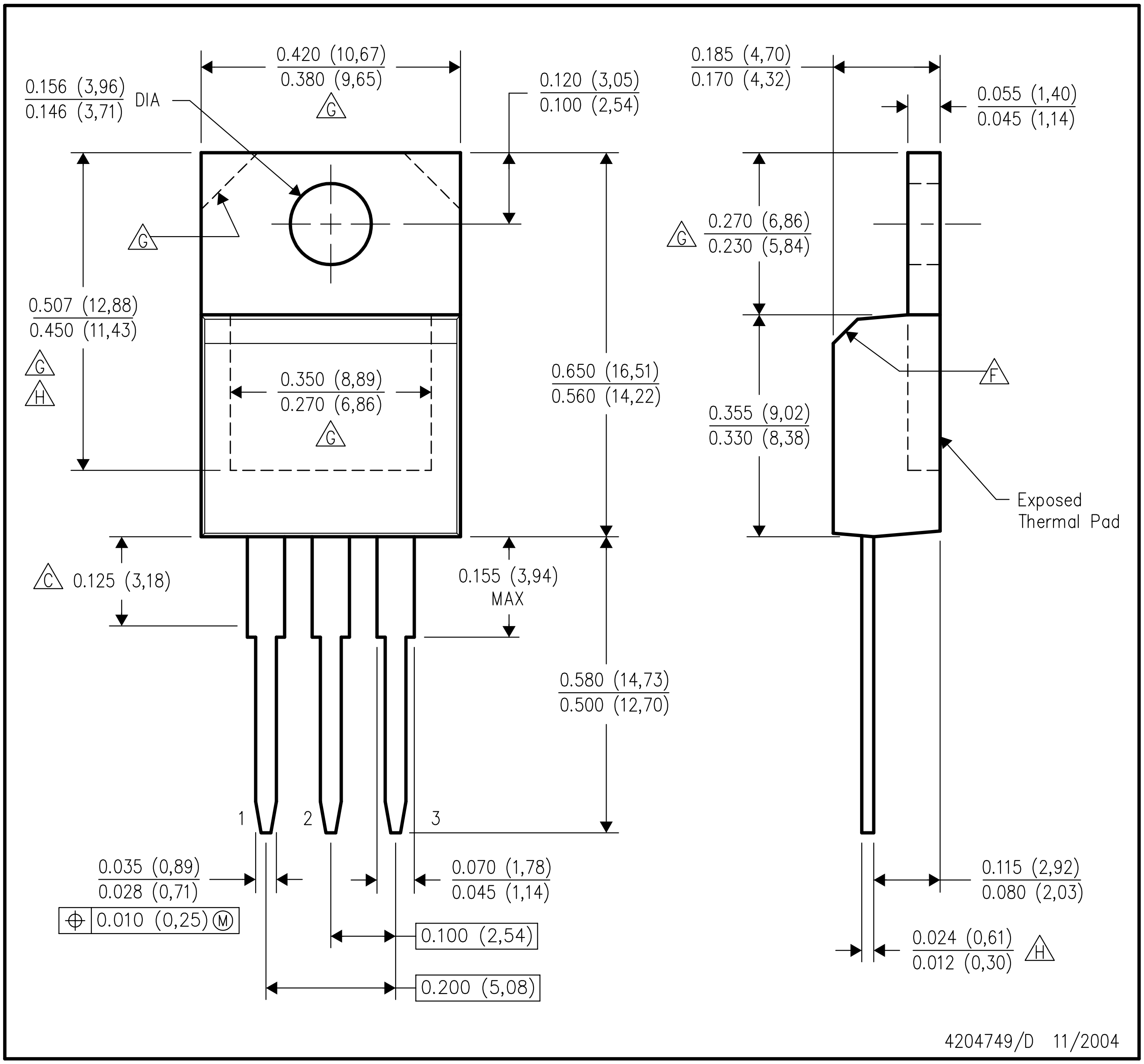
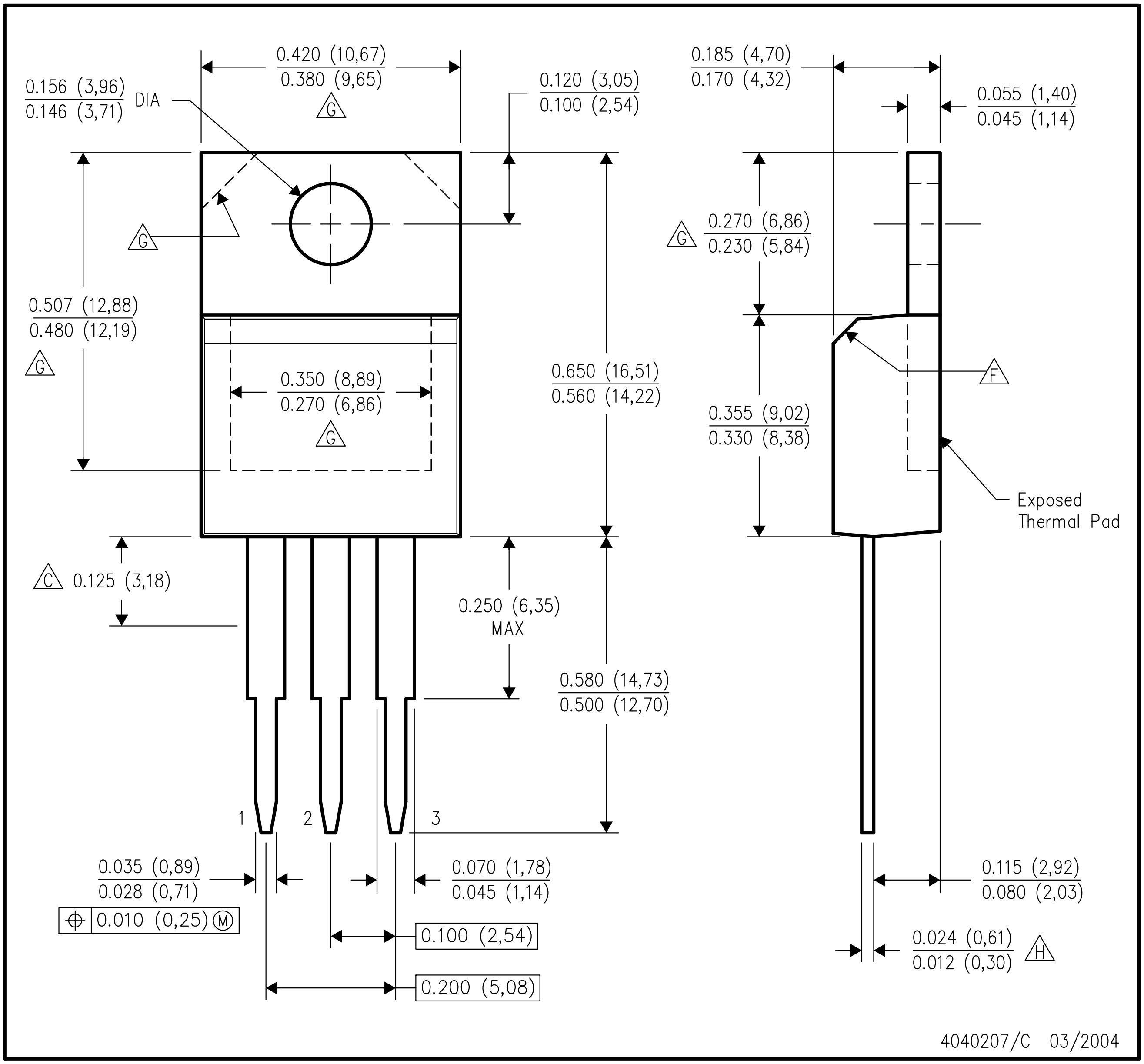
KCS (R–PSFM–T3) PLASTIC FLANGE–MOUNT PACKAGE



NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Lead dimensions are not controlled within this area.
- D. All lead dimensions apply before solder dip.
- E. The center lead is in electrical contact with the mounting tab.
- F. The chamfer is optional.
- G. Thermal pad contour optional within these dimensions.
- H. Falls within JEDEC TO–220 variation AB, except minimum lead thickness and minimum exposed pad length.

KC (R–PSFM–T3) PLASTIC FLANGE–MOUNT PACKAGE



NOTES:
- A. All linear dimensions are in inches (millimeters).
- B. This drawing is subject to change without notice.
- C. Lead dimensions are not controlled within this area.
- D. All lead dimensions apply before solder dip.
- E. The center lead is in electrical contact with the mounting tab.
- F. The chamfer is optional.
- G. Thermal pad contour optional within these dimensions.
- H. Falls within JEDEC TO–220 variation AB, except minimum lead thickness.

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