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SEMICONDUCTOR™

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74LCX541
Low Voltage Octal Buffer/Line Driver with 5V Tolerant Inputs and Outputs

General Description

The LCX541 is an octal buffer/line driver designed to be employed as memory and address drivers, clock drivers and bus oriented transmitter/receivers. The LCX541 is a non inverting option of the LCX540.

This device is similar in function to the LCX244 while providing flow-through architecture (inputs on opposite side from outputs). This pinout arrangement makes this device especially useful as an output port for microprocessors, allowing ease of layout and greater PC board density.

The LCX541 is designed for low voltage (2.5V or 3.3V) V_{CC} applications with capability of interfacing to a 5V signal environment. The LCX541 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining CMOS low power dissipation.

Features

- 5V tolerant input and outputs
- 2.3V–3.6V V_{CC} specifications provided
- 6.5 ns t_{PD} max (V_{CC} = 3.3V), 10 µA I_{CC} max
- Power-down high impedance inputs and outputs
- Supports live insertion/withdrawal (Note 1)
- ±24 mA output drive (V_{CC} = 3.0V)
- Implements patented noise/ EMI reduction circuitry
- Latch-up performance exceeds 500 mA
- ESD performance:
 - Human body model > 2000V
  - Machine model > 200V

Note 1: To ensure the high-impedance state during power up or down, $\overline{OE}$ should be tied to V_{CC} through a pull-up resistor: the minimum value or the resistor is determined by the current-sourcing capability of the driver.

Ordering Code:

Order Number	Package Number	Package Description
74LCX541WM	M20B	20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
74LCX541SJ	M20D	20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
74LCX541MSA	MSA20	20-Lead Shrink Small Outline Package (SSOP), EIAJ TYPE II, 5.3mm Wide
74LCX541MTC	MTC20	20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide

Devices also available in Tape and Reel. Specify by appending the suffix letter "X" to the ordering code.

Logic Symbol
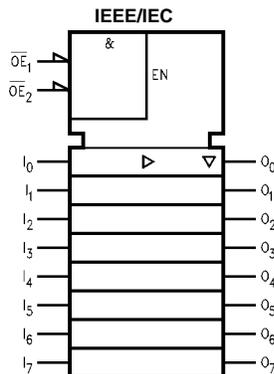
Connection Diagram
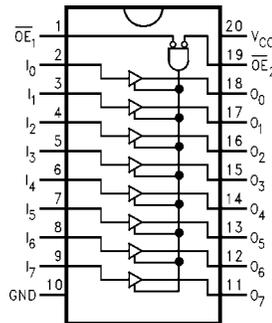
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Pin Descriptions

Pin Names	Description
$\overline{OE}_1$, $\overline{OE}_2$	3-STATE Output Enable Inputs
I_0, I_7	Inputs
O_0, O_7	Outputs

Truth Table

Inputs			Outputs
$\overline{OE}_1$	$\overline{OE}_2$	I	O_n
L	L	H	H
H	X	X	Z
X	H	X	Z
L	L	L	L

H = HIGH Voltage Level
L = LOW Voltage Level
X = Immaterial
Z = High Impedance

"74LCX541MSAX"

Absolute Maximum Ratings(Note 2)

Symbol	Parameter	Value	Conditions	Units
V_{CC}	Supply Voltage	−0.5 to +7.0		V
V_I	DC Input Voltage	−0.5 to +7.0		V
V_O	DC Output Voltage	−0.5 to +7.0	Output in 3-STATE	V
		−0.5 to V_{CC} + 0.5	Output in HIGH or LOW State (Note 3)	
I_{IK}	DC Input Diode Current	−50	V_I < GND	mA
I_{OK}	DC Output Diode Current	−50	V_O < GND	mA
		+50	V_O > V_{CC}	
I_O	DC Output Source/Sink Current	±50		mA
I_{CC}	DC Supply Current per Supply Pin	±100		mA
I_{GND}	DC Ground Current per Ground Pin	±100		mA
T_{STG}	Storage Temperature	−65 to +150		°C

Recommended Operating Conditions (Note 4)

Symbol	Parameter		Min	Max	Units
V_{CC}	Supply Voltage	Operating	2.0	3.6	V
		Data Retention	1.5	3.6	
V_I	Input Voltage		0	5.5	V
V_O	Output Voltage	HIGH or LOW State	0	V_{CC}	V
		3-STATE	0	5.5	
I_{OH}/I_{OL}	Output Current	V_{CC} = 3.0V – 3.6V		±24	mA
		V_{CC} = 2.7V – 3.0V		±12	
		V_{CC} = 2.3V – 2.7V		±8	
T_A	Free-Air Operating Temperature		−40	85	°C
Δt/ΔV	Input Edge Rate, V_{IN} = 0.8V–2.0V, V_{CC} = 3.0V		0	10	ns/V

Note 2: The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.

Note 3: I_O Absolute Maximum Rating must be observed.

Note 4: Unused inputs or I/O's must be held HIGH or LOW. They may not float.

DC Electrical Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	T_A = −40°C to +85°C		Units
				Min	Max	
V_{IH}	HIGH Level Input Voltage		2.3 – 2.7	1.7		V
			2.7 – 3.6	2.0		
V_{IL}	LOW Level Input Voltage		2.3 – 2.7		0.7	V
			2.7 – 3.6		0.8	
V_{OH}	HIGH Level Output Voltage	I_{OH} = −100μA	2.3 – 3.6	V_{CC} - 0.2		V
		I_{OH} = -8 mA	2.3	1.8		
		I_{OH} = −12 mA	2.7	2.2		
		I_{OH} = −18 mA	3.0	2.4		
		I_{OH} = −24 mA	3.0	2.2		
V_{OL}	LOW Level Output Voltage	I_{OL} = 100μA	2.3 – 3.6		0.2	V
		I_{OL} = 8mA	2.3		0.6	
		I_{OL} = 12 mA	2.7		0.4	
		I_{OL} = 16 mA	3.0		0.4	
		I_{OL} = 24 mA	3.0		0.55	
I_I	Input Leakage Current	0 ≤ V_I ≤ 5.5V	2.3 – 3.6		±5.0	μA
I_{OFF}	Power-Off Leakage Current	V_I or V_O = 5.5V	0		10	μA
I_{CC}	Quiescent Supply Current	V_I = V_{CC} or GND	2.3 – 3.6		10	μA
		3.6V ≤ V_I, V_O ≤ 5.5V (Note 5)	2.3 – 3.6		±10	
$ΔI_{CC}$	Increase in I_{CC} per Input	V_{IH} = V_{CC} 0.6V	2.3 – 3.6		500	μA

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DC Electrical Characteristics (Continued)

Note 5: Outputs disabled or 3-STATE only.

AC Electrical Characteristics

Symbol	Parameter	$T_A = -40°C$ to $+85°C$, $R_L = 500\Omega$						Units
		$V_{CC} = 3.3V \pm 0.3V$		$V_{CC} = 2.7V$		$V_{CC} = 2.5V \pm 0.2V$		
		$C_L = 50$ pF		$C_L = 50$ pF		$C_L = 30$ pF		
		Min	Max	Min	Max	Min	Max	
t_{PHL}	Propagation Delay	1.5	6.5	1.5	7.5	1.5	7.8	ns
t_{PLH}		1.5	6.5	1.5	7.5	1.5	7.8	
t_{PZL}	Output Enable Time	1.5	8.5	1.5	9.5	1.5	10.5	ns
t_{PZH}		1.5	8.5	1.5	9.5	1.5	10.5	
t_{PLZ}	Output Disable Time	1.5	7.5	1.5	8.5	1.5	9.0	ns
t_{PHZ}		1.5	7.5	1.5	8.5	1.5	9.0	
t_{OSHL}	Output to Output Skew (Note 6)		1.0					ns
t_{OSLH}			1.0					

Note 6: Skew is defined as the absolute value of the difference between the actual propagation delay for any two separate outputs of the same device. The specification applies to any outputs switching in the same direction, either HIGH-to-LOW (t_{OSHL}) or LOW-to-HIGH (t_{OSLH}).

Dynamic Switching Characteristics

Symbol	Parameter	Conditions	V_{CC} (V)	$T_A = 25°C$ Typical	Units
V_{OLP}	Quiet Output Dynamic Peak V_{OL}	$C_L = 50$ pF, $V_{IH} = 3.3V$, $V_{IL} = 0V$	3.3	0.8	V
		$C_L = 30$ pF, $V_{IH} = 2.5V$, $V_{IL} = 0V$	2.5	0.6	
V_{OLV}	Quiet Output Dynamic Valley V_{OL}	$C_L = 50$ pF, $V_{IH} = 3.3V$, $V_{IL} = 0V$	3.3	−0.8	V
		$C_L = 30$ pF, $V_{IH} = 2.5V$, $V_{IL} = 0V$	2.5	−0.6	

Capacitance

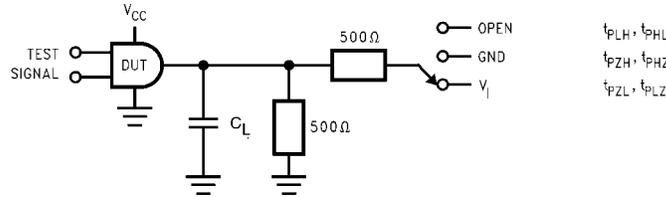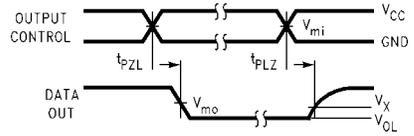| Symbol	Parameter	Conditions	Typical	Units
C_{IN}	Input Capacitance	$V_{CC} =$ Open, $V_I = 0V$ or V_{CC}	7	pF
C_{OUT}	Output Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}	8	pF
C_{PD}	Power Dissipation Capacitance	$V_{CC} = 3.3V$, $V_I = 0V$ or V_{CC}, f = 10 MHz	25	pF

AC Loading and Waveforms Generic for LCX Family

FIGURE 1. AC Test Circuit

(C$_L$ includes probe and jig capacitance)

Test	Switch
t$_{PLH}$, t$_{PHL}$	Open
t$_{PZL}$, t$_{PLZ}$	6V at V$_{CC}$ = 3.3 ± 0.3V V$_{CC}$ x 2 at V$_{CC}$ = 2.5 ± 0.2V
t$_{PZH}$, t$_{PHZ}$	GND
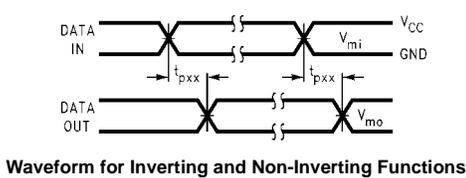
Waveform for Inverting and Non-Inverting Functions

Propagation Delay, Pulse Width and t$_{rec}$ Waveforms

3-STATE Output High Enable and Disable Times for Logic

3-STATE Output Low Enable and Disable Times for Logic

Setup Time, Hold TIme and Recovery TIme for Logic
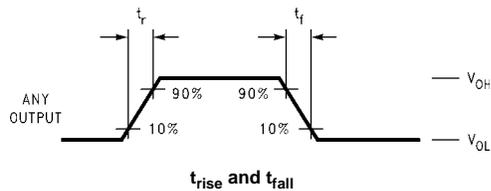

t$_{rise}$ and t$_{fall}$

FIGURE 2. Waveforms

(Input Pulse Characteristics; f = 1MHz, t$_r$ = t$_f$ = 3ns)

Symbol	V$_{CC}$		
	3.3V ± 0.3V	2.7V	2.5V ± 0.2V
V$_{mi}$	1.5V	1.5V	V$_{CC}$/2
V$_{mo}$	1.5V	1.5V	V$_{CC}$/2
V$_x$	V$_{OL}$ + 0.3V	V$_{OL}$ + 0.3V	V$_{OL}$ + 0.15V
V$_y$	V$_{OH}$ − 0.3V	V$_{OH}$ − 0.3V	V$_{OH}$ − 0.15V

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Schematic Diagram Generic for LCX Family

Physical Dimensions inches (millimeters) unless otherwise noted

0.496 – 0.512
(12.598 – 13.005)

20 19 18 17 16 15 14 13 12 11

0.394 – 0.419
(10.008 – 10.643)

LEAD NO 1
IDENT

30° TYP

1   2   3   4   5   6   7   8   9   10

0.010 MAX
(0.254)

0.291 – 0.299
(7.391 – 7.595)

0.010 – 0.029
(0.254 – 0.737) × 45°

0.093 – 0.104
(2.362 – 2.642)

0.004 – 0.012
(0.102 – 0.305)

8° MAX TYP
ALL LEADS

SEATING
PLANE

0.009 – 0.013
(0.229 – 0.330)
TYP ALL LEADS

0.004
(0.102)
ALL LEAD TIPS

0.016 – 0.050
(0.406 – 1.270)
TYP ALL LEADS

0.014
(0.356)

0.050
(1.270)
TYP

0.014 – 0.020 TYP
(0.356 – 0.508)

0.008 TYP
(0.203)

M20B (REV F)

20-Lead Small Outline Integrated Circuit (SOIC), JEDEC MS-013, 0.300" Wide
Package Number M20B

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Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

12.6±0.10
-A-
0.40 TYP
20
11
7.8
3.9
5.3±0.10
-B-
PIN #1 IDENT.
1
10
0.2 C B A
ALL LEAD TIPS

20 19   12 11
5.01 TYP
9.27 TYP
(2.13 TYP)
1   2   9   10
1.27 TYP   0.6 TYP
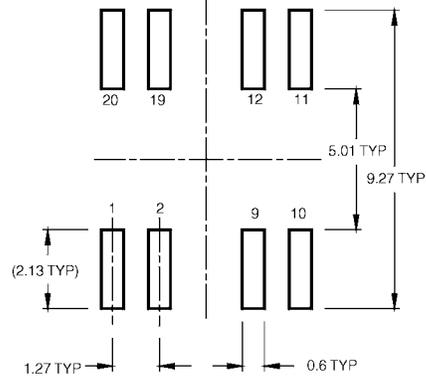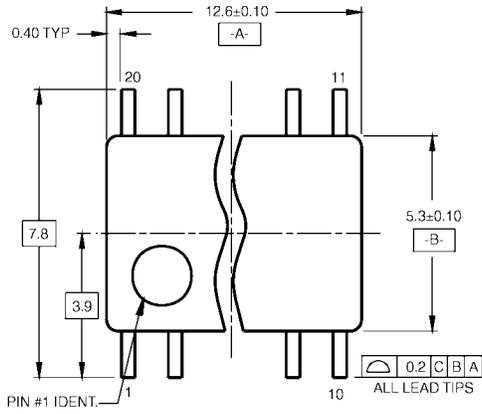
LAND PATTERN RECOMMENDATION

ALL LEAD TIPS
0.1 C
2.1 MAX.
1.8±0.1
-C-
0.15±0.05
1.27 TYP
0.35-0.51
0.12 M C A
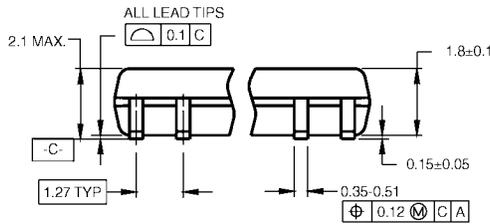
DIMENSIONS ARE IN MILLIMETERS
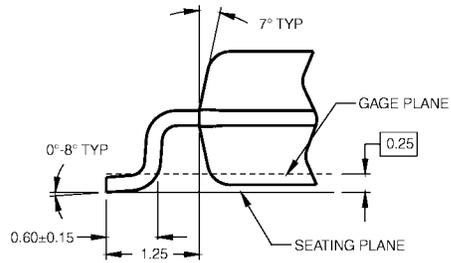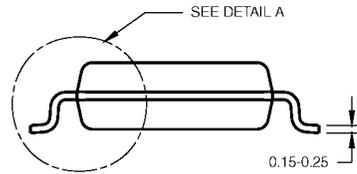
NOTES:
A. CONFORMS TO EIAJ EDR-7320 REGISTRATION,
   ESTABLISHED IN DECEMBER, 1998.
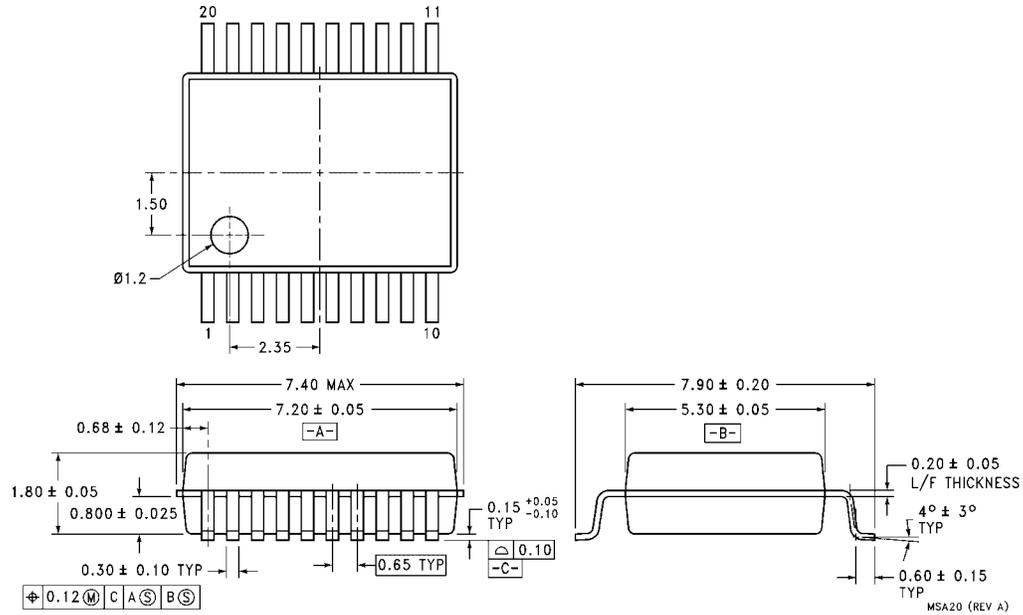B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD
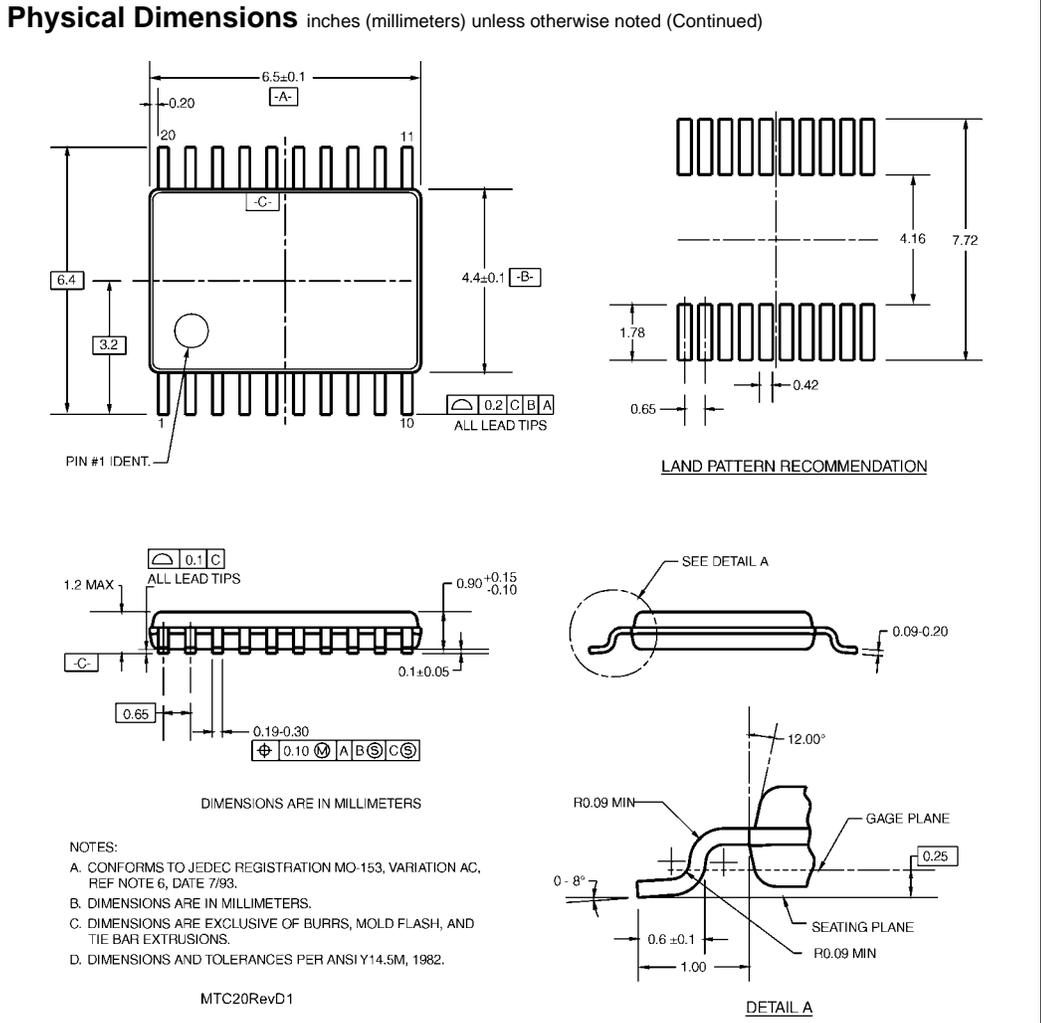   FLASH, AND TIE BAR EXTRUSIONS.

M20DRevB1

SEE DETAIL A
0.15-0.25

7° TYP
GAGE PLANE
0°-8° TYP
0.25
0.60±0.15
1.25
SEATING PLANE

DETAIL A

20-Lead Small Outline Package (SOP), EIAJ TYPE II, 5.3mm Wide
Package Number M20D

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

20   11

1.50

Ø1.2

1   2.35   10

7.40 MAX
7.20 ± 0.05
-A-

0.68 ± 0.12

1.80 ± 0.05
0.800 ± 0.025

0.30 ± 0.10 TYP

⊕ 0.12 Ⓜ C AⓈ BⓈ

0.15 +0.05 -0.10 TYP

0.65 TYP

⌂ 0.10
-C-

7.90 ± 0.20
5.30 ± 0.05
-B-

0.20 ± 0.05
L/F THICKNESS

4° ± 3°
TYP

0.60 ± 0.15
TYP

MSA20 (REV A)

20-Lead Shrink Small Outline Package (SSOP), EIAJ TYPE II, 5.3mm Wide
Package Number MSA20

74LCX541 Low Voltage Octal Buffer/Line Driver with 5V Tolerant Inputs and Outputs

Physical Dimensions inches (millimeters) unless otherwise noted (Continued)

NOTES:
A. CONFORMS TO JEDEC REGISTRATION MO-153, VARIATION AC, REF NOTE 6, DATE 7/93.
B. DIMENSIONS ARE IN MILLIMETERS.
C. DIMENSIONS ARE EXCLUSIVE OF BURRS, MOLD FLASH, AND TIE BAR EXTRUSIONS.
D. DIMENSIONS AND TOLERANCES PER ANSI Y14.5M, 1982.

MTC20RevD1

**20-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 4.4mm Wide
Package Number MTC20**

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