查询"2305B-1HDCG"供应商

# 3.3V ZERO DELAY CLOCK BUFFER

**IDT2305B**

## FEATURES:

- Phase-Lock Loop Clock Distribution
- 10MHz to 133MHz operating frequency
- Distributes one clock input to one bank of five outputs
- Zero Input-Output Delay
- Output Skew < 250ps
- Low jitter <175 ps cycle-to-cycle
- 50ps typical cycle-to-cycle jitter (15pF, 66MHz)
- IDT2305B-1 for Standard Drive
- IDT2305B-1H for High Drive
- No external RC network required
- Operates at 3.3V $V_{DD}$
- Power down mode
- Available in SOIC and TSSOP packages

***NOTE: EOL for non-green parts to occur on 5/13/10 per PDN U-09-01***

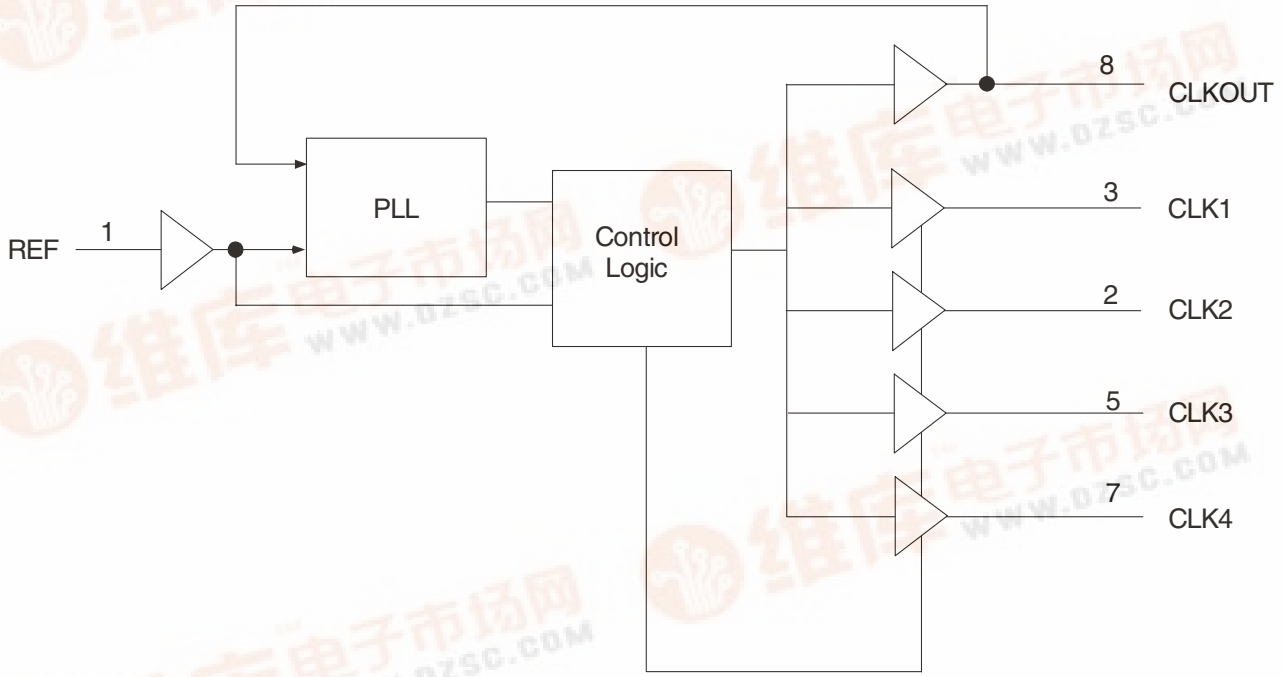
## DESCRIPTION:

The IDT2305B is a high-speed phase-lock loop (PLL) clock buffer, designed to address high-speed clock distribution applications. The zero delay is achieved by aligning the phase between the incoming clock and the output clock, operable within the range of 10 to 133MHz.

The IDT2305B is an 8-pin version of the IDT2309B. IDT2305B accepts one reference input, and drives out five low skew clocks. The -1H version of this device operates, up to 133MHz frequency and has a higher drive than the -1 device. All parts have on-chip PLLs which lock to an input clock on the REF pin. The PLL feedback is on-chip and is obtained from the CLKOUT pad. In the absence of an input clock, the IDT2305B enters power down. In this mode, the device will draw less than 25µA, the outputs are tri-stated, and the PLL is not running, resulting in a significant reduction of power.

The IDT2305B is characterized for both Industrial and Commercial operation.

## FUNCTIONAL BLOCK DIAGRAM

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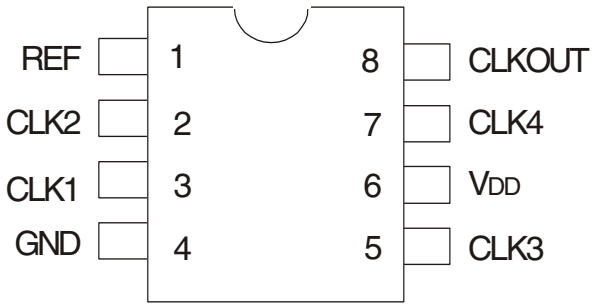
## PIN CONFIGURATION




SOIC/TSSOP
TOP VIEW

## ABSOLUTE MAXIMUM RATINGS(1)

| Symbol | Rating | Max. | Unit |
|---|---|---|---|
| $V_{DD}$ | Supply Voltage Range | –0.5 to +4.6 | V |
| $V_I$ (2) | Input Voltage Range (REF) | –0.5 to +5.5 | V |
| $V_I$ | Input Voltage Range (except REF) | –0.5 to $V_{DD}$+0.5 | V |
| $I_{IK}$ ($V_I$ < 0) | Input Clamp Current | –50 | mA |
| $I_O$ ($V_O$ = 0 to $V_{DD}$) | Continuous Output Current | ±50 | mA |
| $V_{DD}$ or GND | Continuous Current | ±100 | mA |
| $T_A$ = 55°C (in still air)(3) | Maximum Power Dissipation | 0.7 | W |
| $T_{STG}$ | Storage Temperature Range | –65 to +150 | °C |
| Operating Temperature | Commercial Temperature Range | 0 to +70 | °C |
| Operating Temperature | Industrial Temperature Range | -40 to +85 | °C |

NOTES:
1. Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
2. The input and output negative-voltage ratings may be exceeded if the input and output clamp-current ratings are observed.
3. The maximum package power dissipation is calculated using a junction temperature of 150°C and a board trace length of 750 mils.

## APPLICATIONS:

- SDRAM
- Telecom
- Datacom
- PC Motherboards/Workstations
- Critical Path Delay Designs

## PIN DESCRIPTION

| Pin Name | Pin Number | Type | Functional Description |
|---|---|---|---|
| REF(1) | 1 | IN | Input reference clock, 5 Volt tolerant input |
| CLK2(2) | 2 | Out | Output clock |
| CLK1(2) | 3 | Out | Output clock |
| GND | 4 | Ground | Ground |
| CLK3(2) | 5 | Out | Output clock |
| $V_{DD}$ | 6 | PWR | 3.3V Supply |
| CLK4(2) | 7 | Out | Output clock |
| CLKOUT(2) | 8 | Out | Output clock, internal feedback on this pin |

NOTES:
1. Weak pull down.
2. Weak pull down on all outputs.

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## OPERATING CONDITIONS - COMMERCIAL

| Symbol | Parameter | Min. | Max. | Unit |
|---|---|---|---|---|
| $V_{DD}$ | Supply Voltage | 3 | 3.6 | V |
| $T_A$ | Operating Temperature (Ambient Temperature) | 0 | 70 | °C |
| $C_L$ | Load Capacitance < 100MHz | — | 30 | pF |
| | Load Capacitance 100MHz - 133MHz | — | 10 | |
| $C_{IN}$ | Input Capacitance | — | 7 | pF |

## DC ELECTRICAL CHARACTERISTICS - COMMERCIAL

| Symbol | Parameter | Conditions | | Min. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{IL}$ | Input LOW Voltage Level | | | — | 0.8 | V |
| $V_{IH}$ | Input HIGH Voltage Level | | | 2 | — | V |
| $I_{IL}$ | Input LOW Current | $V_{IN}$ = 0V | | — | 50 | µA |
| $I_{IH}$ | Input HIGH Current | $V_{IN}$ = $V_{DD}$ | | — | 100 | µA |
| $V_{OL}$ | Output LOW Voltage | Standard Drive | $I_{OL}$ = 8mA | — | 0.4 | V |
| | | High Drive | $I_{OL}$ = 12mA (-1H) | | | |
| $V_{OH}$ | Output HIGH Voltage | Standard Drive | $I_{OH}$ = -8mA | 2.4 | — | V |
| | | High Drive | $I_{OH}$ = -12mA (-1H) | | | |
| $I_{DD_PD}$ | Power Down Current | REF = 0MHz | | — | 12 | µA |
| $I_{DD}$ | Supply Current | Unloaded Outputs at 66.66MHz | | — | 32 | mA |

## SWITCHING CHARACTERISTICS (2305B-1) - COMMERCIAL (1,2)

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $t_1$ | Output Frequency | 10pF Load | 10 | — | 133 | MHz |
| | | 30pF Load | 10 | — | 100 | |
| | Duty Cycle = $t_2 \div t_1$ | Measured at 1.4V, $F_{OUT}$ = 66.66MHz | 40 | 50 | 60 | % |
| $t_3$ | Rise Time | Measured between 0.8V and 2V | — | — | 2.5 | ns |
| $t_4$ | Fall Time | Measured between 0.8V and 2V | — | — | 2.5 | ns |
| $t_5$ | Output to Output Skew | All outputs equally loaded | — | — | 250 | ps |
| $t_6$ | Delay, REF Rising Edge to CLKOUT Rising Edge | Measured at $V_{DD}/2$ | — | 0 | ±350 | ps |
| $t_7$ | Device-to-Device Skew | Measured at $V_{DD}/2$ on the CLKOUT pins of devices | — | 0 | 700 | ps |
| $t_J$ | Cycle-to-Cycle Jitter | Measured at 66.66MHz, loaded outputs | — | 50 | 175 | ps |
| $t_{LOCK}$ | PLL Lock Time | Stable power supply, valid clock presented on REF pin | — | — | 1 | ms |

NOTES:
1. REF Input has a threshold voltage of $V_{DD}/2$.
2. All parameters specified with loaded outputs.

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## SWITCHING CHARACTERISTICS (2305B-1H) - COMMERCIAL[1,2]

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $t_1$ | Output Frequency | 10pF Load | 10 | — | 133 | MHz |
| | | 30pF Load | 10 | — | 100 | |
| | Duty Cycle = $t_2 \div t_1$ | Measured at 1.4V, $F_{OUT}$ = 66.66MHz | 40 | 50 | 60 | % |
| | Duty Cycle = $t_2 \div t_1$ | Measured at 1.4V, $F_{OUT}$ <50MHz | 45 | 50 | 55 | % |
| $t_3$ | Rise Time | Measured between 0.8V and 2V | — | — | 1.5 | ns |
| $t_4$ | Fall Time | Measured between 0.8V and 2V | — | — | 1.5 | ns |
| $t_5$ | Output to Output Skew | All outputs equally loaded | — | — | 250 | ps |
| $t_6$ | Delay, REF Rising Edge to CLKOUT Rising Edge | Measured at $V_{DD}/2$ | — | 0 | ±350 | ps |
| $t_7$ | Device-to-Device Skew | Measured at $V_{DD}/2$ on the CLKOUT pins of devices | — | 0 | 700 | ps |
| $t_8$ | Output Slew Rate | Measured between 0.8V and 2V using Test Circuit #2 | 1 | — | — | V/ns |
| $t_J$ | Cycle-to-Cycle Jitter | Measured at 66.66MHz, loaded outputs | — | — | 175 | ps |
| $t_{LOCK}$ | PLL Lock Time | Stable power supply, valid clock presented on REF pin | — | — | 1 | ms |

NOTES:
1. REF Input has a threshold voltage of $V_{DD}/2$.
2. All parameters specified with loaded outputs.

## OPERATING CONDITIONS - INDUSTRIAL

| Symbol | Parameter | Min. | Max. | Unit |
|---|---|---|---|---|
| $V_{DD}$ | Supply Voltage | 3 | 3.6 | V |
| $T_A$ | Operating Temperature (Ambient Temperature) | -40 | +85 | °C |
| $C_L$ | Load Capacitance < 100MHz | — | 30 | pF |
| | Load Capacitance 100MHz - 133MHz | — | 10 | |
| $C_{IN}$ | Input Capacitance | — | 7 | pF |

## DC ELECTRICAL CHARACTERISTICS - INDUSTRIAL

| Symbol | Parameter | Conditions | | Min. | Max. | Unit |
|---|---|---|---|---|---|---|
| $V_{IL}$ | Input LOW Voltage Level | | | — | 0.8 | V |
| $V_{IH}$ | Input HIGH Voltage Level | | | 2 | — | V |
| $I_{IL}$ | Input LOW Current | $V_{IN}$ = 0V | | — | 50 | µA |
| $I_{IH}$ | Input HIGH Current | $V_{IN}$ = $V_{DD}$ | | — | 100 | µA |
| $V_{OL}$ | Output LOW Voltage | Standard Drive | $I_{OL}$ = 8mA | — | 0.4 | V |
| | | High Drive | $I_{OL}$ = 12mA (-1H) | | | |
| $V_{OH}$ | Output HIGH Voltage | Standard Drive | $I_{OH}$ = -8mA | 2.4 | — | V |
| | | High Drive | $I_{OH}$ = -12mA (-1H) | | | |
| $I_{DD_PD}$ | Power Down Current | REF = 0MHz | | — | 25 | µA |
| $I_{DD}$ | Supply Current | Unloaded Outputs at 66.66MHz | | — | 35 | mA |

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## SWITCHING CHARACTERISTICS (2305B-1) - INDUSTRIAL (1,2)

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $t_1$ | Output Frequency | 10pF Load | 10 | — | 133 | MHz |
| | | 30pF Load | 10 | — | 100 | |
| | Duty Cycle = $t_2 \div t_1$ | Measured at 1.4V, $F_{OUT}$ = 66.66MHz | 40 | 50 | 60 | % |
| $t_3$ | Rise Time | Measured between 0.8V and 2V | — | — | 2.5 | ns |
| $t_4$ | Fall Time | Measured between 0.8V and 2V | — | — | 2.5 | ns |
| $t_5$ | Output to Output Skew | All outputs equally loaded | — | — | 250 | ps |
| $t_6$ | Delay, REF Rising Edge to CLKOUT Rising Edge | Measured at $V_{DD}/2$ | — | 0 | ±350 | ps |
| $t_7$ | Device-to-Device Skew | Measured at $V_{DD}/2$ on the CLKOUT pins of devices | — | 0 | 700 | ps |
| $t_J$ | Cycle-to-Cycle Jitter | Measured at 66.66MHz, loaded outputs | — | 50 | 175 | ps |
| $t_{LOCK}$ | PLL Lock Time | Stable power supply, valid clock presented on REF pin | — | — | 1 | ms |

NOTES:
1. REF Input has a threshold voltage of $V_{DD}/2$.
2. All parameters specified with loaded outputs.

## SWITCHING CHARACTERISTICS (2305B-1H) - INDUSTRIAL (1,2)

| Symbol | Parameter | Conditions | Min. | Typ. | Max. | Unit |
|---|---|---|---|---|---|---|
| $t_1$ | Output Frequency | 10pF Load | 10 | — | 133 | MHz |
| | | 30pF Load | 10 | — | 100 | |
| | Duty Cycle = $t_2 \div t_1$ | Measured at 1.4V, $F_{OUT}$ = 66.66MHz | 40 | 50 | 60 | % |
| | Duty Cycle = $t_2 \div t_1$ | Measured at 1.4V, $F_{OUT}$ <50MHz | 45 | 50 | 55 | % |
| $t_3$ | Rise Time | Measured between 0.8V and 2V | — | — | 1.5 | ns |
| $t_4$ | Fall Time | Measured between 0.8V and 2V | — | — | 1.5 | ns |
| $t_5$ | Output to Output Skew | All outputs equally loaded | — | — | 250 | ps |
| $t_6$ | Delay, REF Rising Edge to CLKOUT Rising Edge | Measured at $V_{DD}/2$ | — | 0 | ±350 | ps |
| $t_7$ | Device-to-Device Skew | Measured at $V_{DD}/2$ on the CLKOUT pins of devices | — | 0 | 700 | ps |
| $t_8$ | Output Slew Rate | Measured between 0.8V and 2V using Test Circuit #2 | 1 | — | — | V/ns |
| $t_J$ | Cycle-to-Cycle Jitter | Measured at 66.66MHz, loaded outputs | — | — | 175 | ps |
| $t_{LOCK}$ | PLL Lock Time | Stable power supply, valid clock presented on REF pin | — | — | 1 | ms |

NOTES:
1. REF Input has a threshold voltage of $V_{DD}/2$.
2. All parameters specified with loaded outputs.

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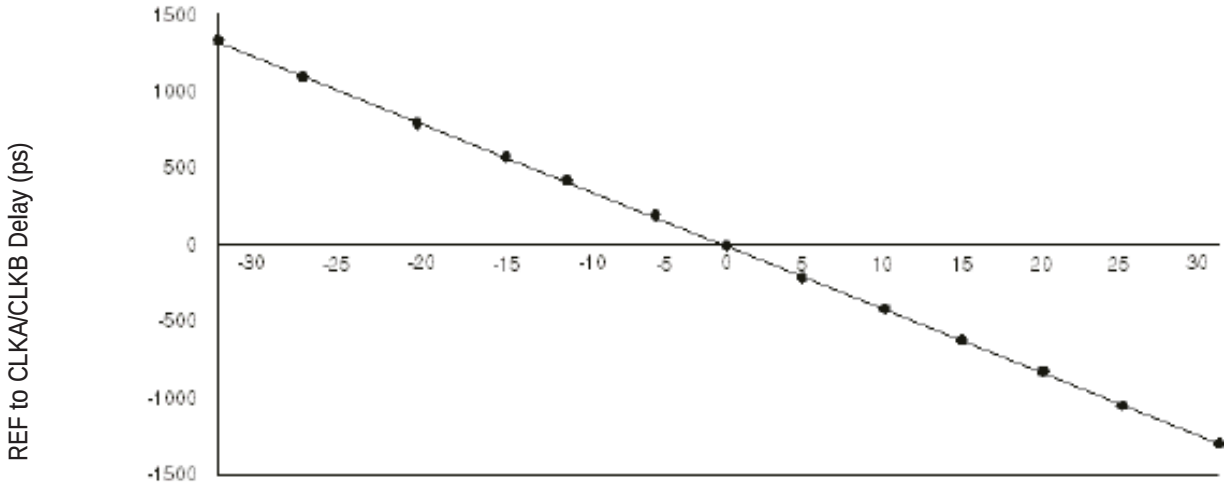
## ZERO DELAY AND SKEW CONTROL

All outputs should be uniformly loaded in order to achieve Zero I/O Delay. Since the CLKOUT pin is the internal feedback for the PLL, its relative loading can affect and adjust the input/output delay. The Output Load Difference diagram illustrates the PLL's relative loading with respect to the other outputs that can adjust the Input-Output (I/O) Delay.

For designs utilizing zero I/O Delay, all outputs including CLKOUT must be equally loaded. Even if the output is not used, it must have a capacitive load equal to that on the other outputs in order to obtain true zero I/O Delay. If I/O Delay adjustments are needed, use the Output Load Difference diagram to calculate loading differences between the CLKOUT pin and other outputs. For zero output-to-output skew, all outputs must be loaded equally.

REF TO CLKA/CLKB RELAY vs. OUTPUT LOAD DIFFERENCE BETWEEN CLKOUT PIN AND CLKA/CLKB PINS




OUTPUT LOAD DIFFERENCE BETWEEN CLKOUT PIN AND CLKA/CLKB PINS (pF)

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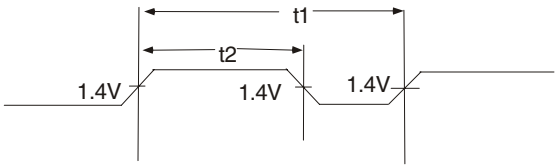
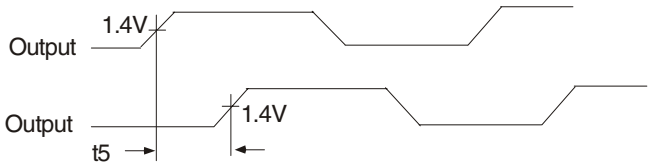
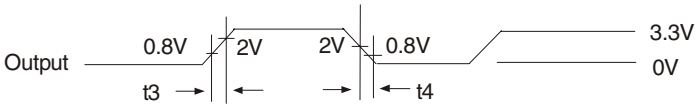
## SWITCHING WAVEFORMS



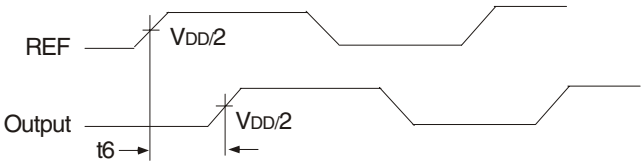

*Duty Cycle Timing*



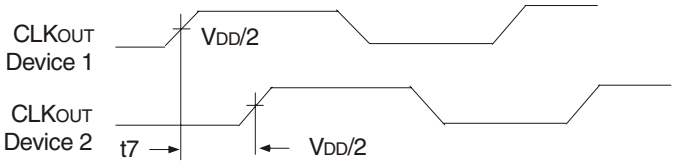

*Output to Output Skew*




*All Outputs Rise/Fall Time*

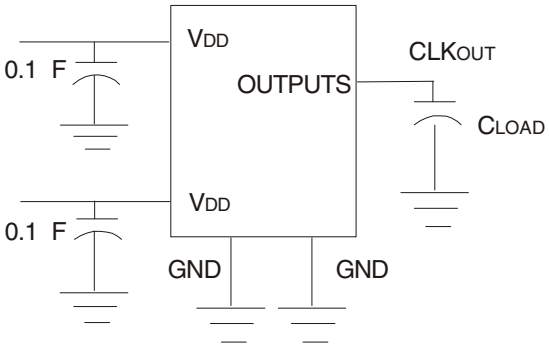



*Input to Output Propagation Delay*

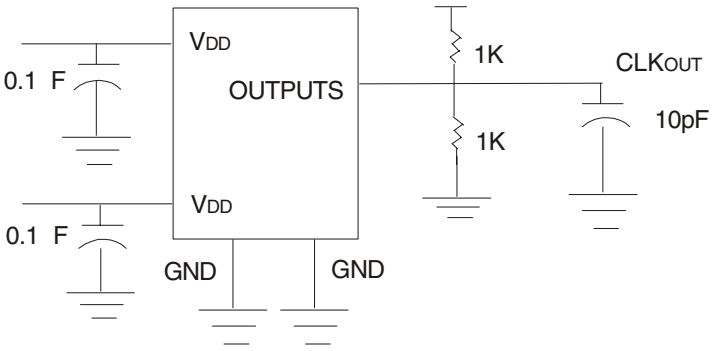



*Device to Device Skew*

## TEST CIRCUITS




*Test Circuit 1 (all Parameters Except t8)*




*Test Circuit 2 (t8, Output Slew Rate On -1H Devices)*

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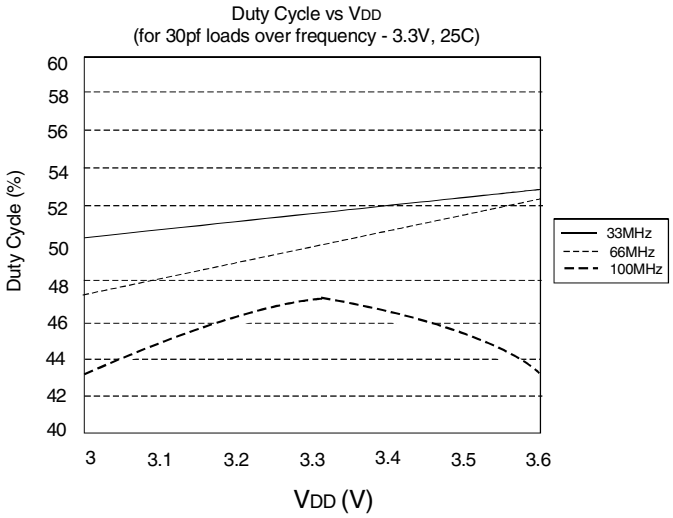
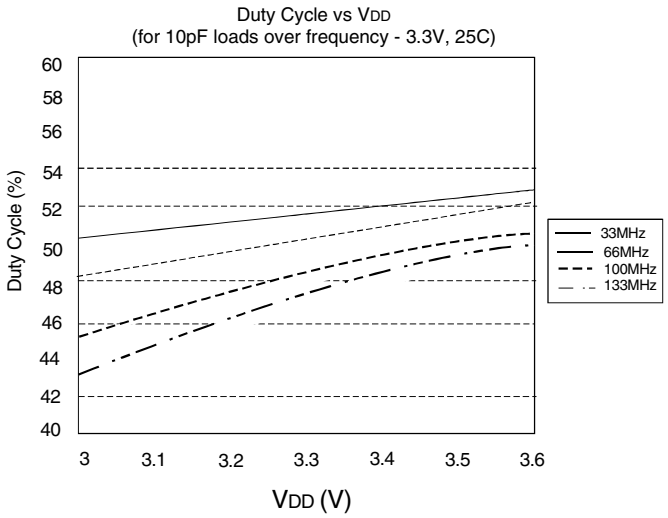
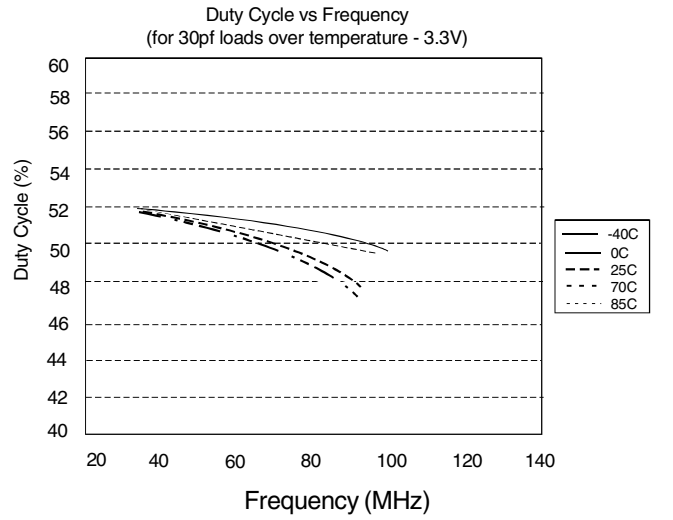
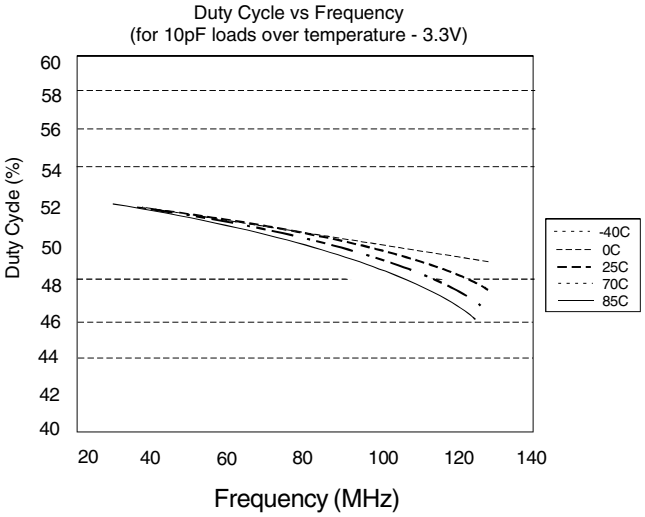
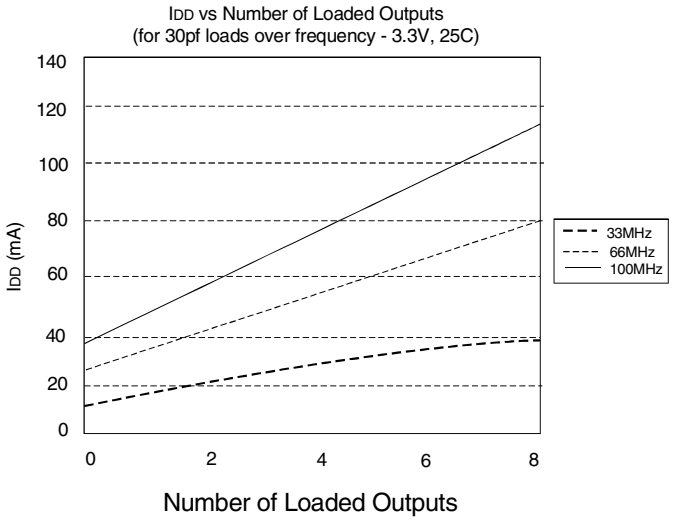
# TYPICAL DUTY CYCLE(1) AND IDD TRENDS(2) FOR IDT2305B-1

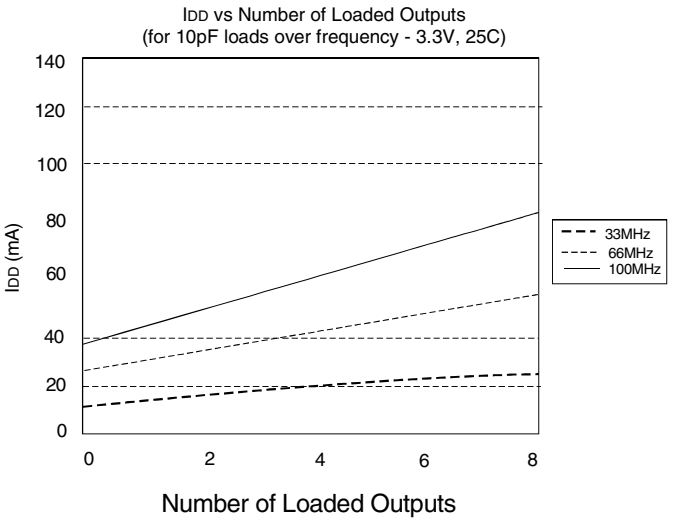



NOTES:
1. Duty Cycle is taken from typical chip measured at 1.4V.
2. IDD data is calculated from IDD = ICORE + nCVf, where ICORE is the unloaded current. (n = Number of outputs; C = Capacitance load per output (F); V = Supply Voltage (V); f = Frequency (Hz))

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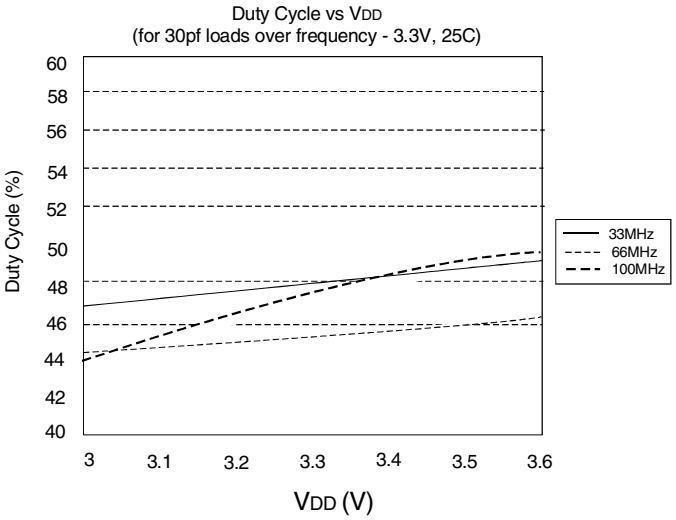
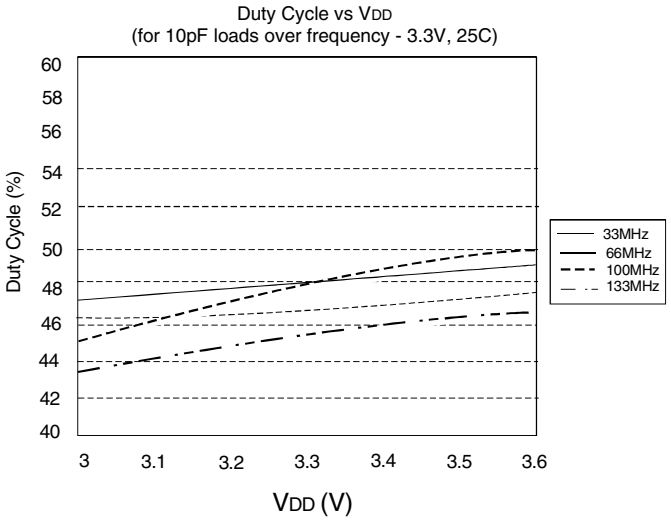
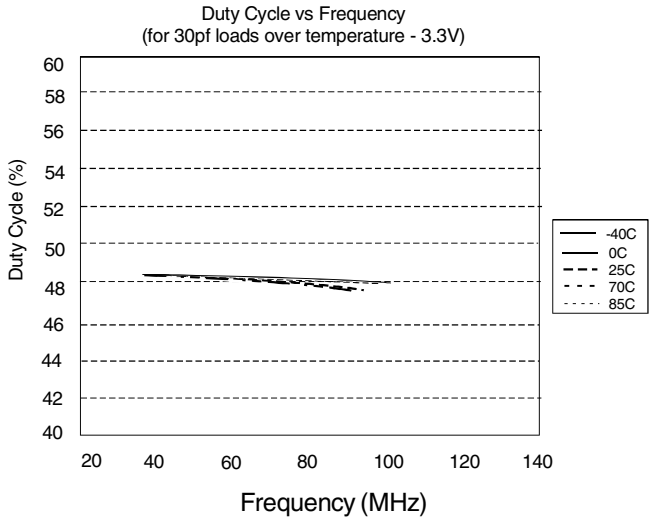
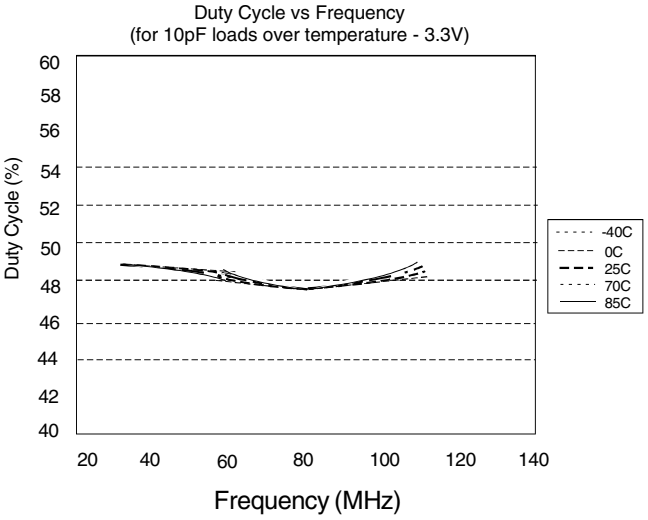
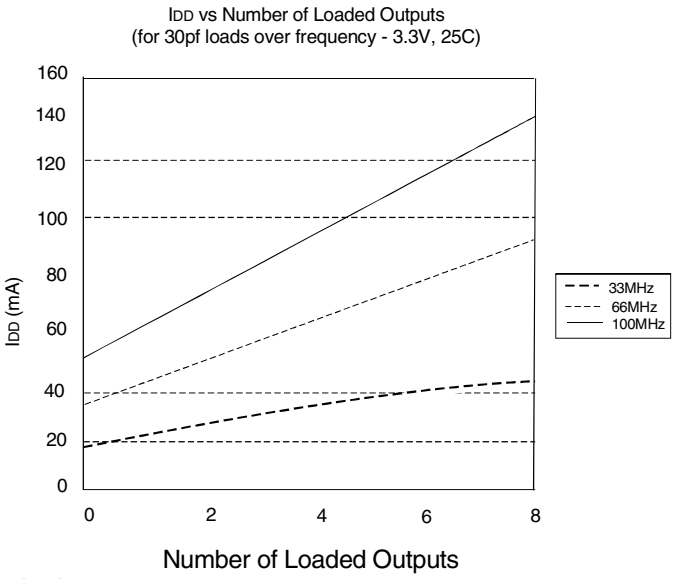
# TYPICAL DUTY CYCLE(1) AND IDD TRENDS(2) FOR IDT2305B-1H

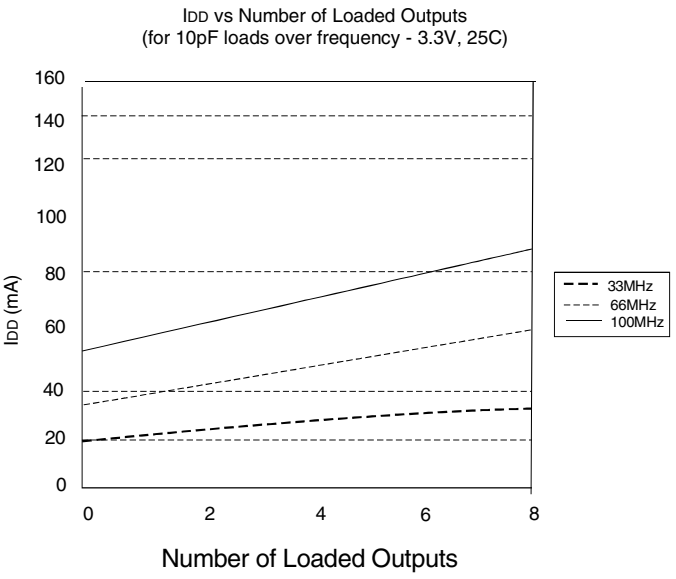



NOTES:
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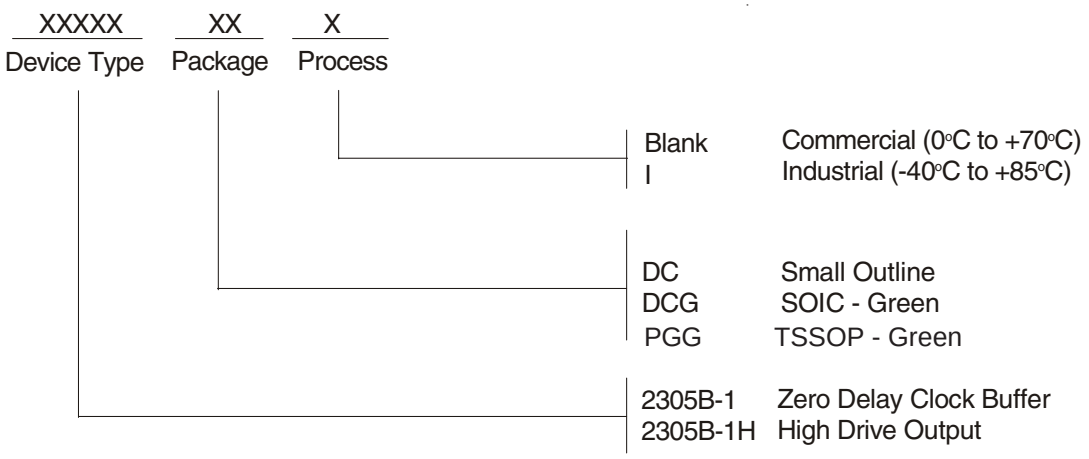
## ORDERING INFORMATION




***NOTE: EOL for non-green parts to occur on 5/13/10 per PDN U-09-01***

| Ordering Code | Package Type | Operating Range |
|---|---|---|
| 2305B-1DC* | 8-Pin SOIC | Commercial |
| 2305B-1DCG | 8-Pin SOIC | Commercial |
| 2305B-1HDC* | 8-Pin SOIC | Commercial |
| 2305B-1HDCG | 8-Pin SOIC | Commercial |
| 2305B-1HDCGI | 8-Pin SOIC | Industrial |
| 2305B-1HDCI* | 8-Pin SOIC | Industrial |
| 2305B-1PGG | 8-Pin TSSOP | Commercial |
| 2305B-1PGGI | 8-Pin TSSOP | Industrial |

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