Programmable Digital Vibration Sensor

ADIS16220

FEATURES

Digital ±70 *g* accelerometer/vibration sensing
22 kHz sensor resonance
100.2 kSPS sample rate
SPI-compatible serial interface
Programmable data capture function:
3 channels, 1024 samples each
1 accelerometer/2 auxiliary ADCs (AIN1, AIN2)
Manual trigger for user initiation
Automatic trigger for periodic data capture
Event trigger for condition-driven capture
Digital temperature sensor output
Digitally controlled sample rate
Digitally controlled frequency response
2 auxiliary digital I/Os
Digitally activated self-test
Digitally activated low power mode
Serial number and device ID
Single-supply operation: 3.15 V to 3.6 V
Operating temperature range: −40°C to +125°C
9.2 mm × 9.2 mm 16-terminal LGA

APPLICATIONS

Vibration analysis
Shock detection and event capture
Condition monitoring
Machine health
Instrumentation, diagnostics
Safety, shut-off sensing
Security sensing, tamper detection

GENERAL DESCRIPTION

The ADIS16220 *i*Sensor® is a digital vibration sensor that combines industry-leading *i*MEMS® sensing technology with signal processing, data capture, and a convenient serial peripheral interface (SPI). The SPI and data buffer structure provide convenient access to wide-bandwidth sensor data. The 22 kHz sensor resonance and 100.2 kSPS sample rate provide adequate response for most machine-health applications. The averaging/decimating filter provides optimization controls for lower bandwidth applications.

An internal clock drives the data sampling system, which fills the buffer memory for user access. The data capture function has three different trigger modes. The automatic data collection allows for periodic wake-up and capture, based on a programmable duty cycle. The manual data capture mode allows the user to initiate a data capture, providing power and read-rate optimization. The event capture mode continuously updates the buffers and monitors them for a preset trigger condition. This mode captures pre-event data and post-event data and produces an alarm indicator for driving an interrupt.

The ADIS16220 also offers a digital temperature sensor, digital power supply measurements, and peak output capture.

The ADIS16220 comes in a 9.2 mm × 9.2 mm × 3.9 mm LGA package that meets the Pb-free solder reflow profile requirements per JEDEC J-STD-020 and has an extended operating temperature range of −40°C to +125°C.

FUNCTION BLOCK DIAGRAM

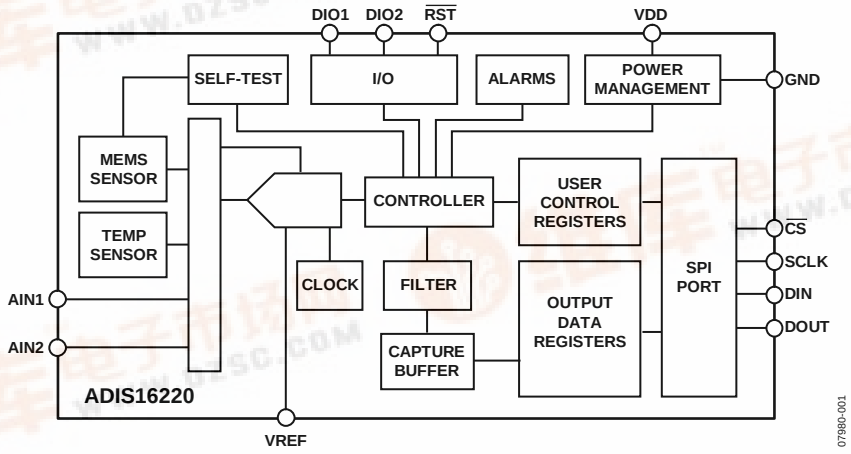


Figure 1.

Rev. 0

One Technology Way, P.O. Box 9106, Norwood, MA 02062-9106, U.S.A.
Tel: 781.329.4700 www.analog.com
Fax: 781.461.3113

TABLE OF CONTENTS

REVISION HISTORY

12/09—Revision 0: Initial Version

SPECIFICATIONS

T_A = −40°C to +125°C, VDD = 3.3 V, ±1 *g*, unless otherwise noted.

Table 1.

Parameter	Conditions	Min	Typ	Max	Unit
ACCELEROMETER					
Measurement Range	T_A = 25°C	−70		+70	*g*
Sensitivity	T_A = 25°C		19.073		mg/LSB
Sensitivity Error	T_A = 25°C		±5		%
Sensitivity Temperature Coefficient			±310		ppm/°C
Nonlinearity	With respect to full scale		±0.2	±2	%
Cross-Axis Sensitivity			±2		%
Alignment Error	With respect to package		±1		Degree
Offset Error	T_A = 25°C	−19.1		+19.1	g
Offset Temperature Coefficient			±5		mg/°C
Output Noise	T_A = 25°C, AVG_CNT = 0x0000		507		mg rms
Output Noise Density	T_A = 25°C, 10 Hz to 1 kHz		4		mg/√Hz
Sensor Resonant Frequency			22		kHz
Self-Test Response		917	1310	1703	LSB
AUXILIARY INPUTS (AIN1, AIN2)					
Resolution[1]			12		Bits
Sensitivity			305.18		µV/LSB
Integral Nonlinearity			2.4		LSB
Differential Nonlinearity			4		LSB
Offset			VDD/2		V
Offset Error			±20.4		LSB
Input Range		0		VDD	V
Input Capacitance			20		pF
ON-CHIP VOLTAGE REFEERENCE					
Output Level			2.5		V
Accuracy			±5		mV
Temperature Coefficient			±40		ppm/°C
Output Impedance			70		Ω
LOGIC INPUTS[2]					
Input High Voltage, V_{INH}		2.0			V
Input Low Voltage, V_{INL}				0.8	V
Logic 1 Input Current, I_{INH}	V_{IH} = 3.3 V		±0.2	±1	µA
Logic 0 Input Current, I_{INL}	V_{IL} = 0 V				
All Except $\overline{RST}$			−40	−60	µA
$\overline{RST}$			−1		mA
Input Capacitance, C_{IN}			10		pF
DIGITAL OUTPUTS[2]					
Output High Voltage, V_{OH}	I_{SOURCE} = 1.6 mA	2.4			V
Output Low Voltage, V_{OL}	I_{SINK} = 1.6 mA			0.4	V
FLASH MEMORY					
Endurance[3]		10,000			Cycles
Data Retention[4]	T_J = 85°C	20			Years
START-UP TIME[5]					
Initial Startup			160		ms
Reset Recovery ($\overline{RST}$)	$\overline{RST}$ or software (GLOB_CMD)		23		ms
Sleep Mode Recovery			2.3		ms

Parameter	Conditions	Min	Typ	Max	Unit
CONVERSION RATE	AVG_CNT = 0x0000		100.2		kSPS
Clock Accuracy			3		%
POWER SUPPLY	Operating voltage range, VDD	3.15	3.3	3.6	V
Power Supply Current	Capture mode, T_A = 25°C		38	46	mA
	Sleep mode, T_A = 25°C		230		µA
	Sleep mode, T_A = 85°C		250		µA
	Sleep mode, T_A = 125°C		600		µA

[1] A 12-bit analog-to-digital converter is used to create a 14-bit digital scale for the AIN1 and AIN2 inputs.
[2] The digital I/O signals are 5 V tolerant.
[3] Endurance is qualified as per JEDEC Standard 22, Method A117, and measured at −40°C, +25°C, +85°C, and +125°C.
[4] Retention lifetime equivalent at junction temperature (T_J) = 85°C as per JEDEC Standard 22, Method A117. Retention lifetime decreases with junction temperature. See Figure 16.
[5] The start-up times presented do not include the data capture time, which is dependent on the AVG_CNT register settings.

TIMING SPECIFICATIONS

T_A = 25°C, VDD = 3.3 V, unless otherwise noted.

Table 2.

Parameter	Description	Min[1]	Typ	Max	Unit
f_{SCLK}	SCLK frequency	0.01		2.25	MHz
t_{STALL}	Stall period between data, between 16th and 17th SCLK	15.4			µs
t_{CS}	Chip select to SCLK edge	48.8			ns
t_{DAV}	DOUT valid after SCLK edge			100	ns
t_{DSU}	DIN setup time before SCLK rising edge	24.4			ns
t_{DHD}	DIN hold time after SCLK rising edge	48.8			ns
t_{SCLKR}, t_{SCLKF}	SCLK rise/fall times		5	12.5	ns
t_{SR}	SCLK high pulse width			12.5	ns
t_{SF}	SCLK low pulse width			12.5	ns
t_{DF}, t_{DR}	DOUT rise/fall times		5	12.5	ns
t_{SFS}	$\overline{CS}$ high after SCLK edge	5			ns

[1] Guaranteed by design, not tested.

TIMING DIAGRAMS

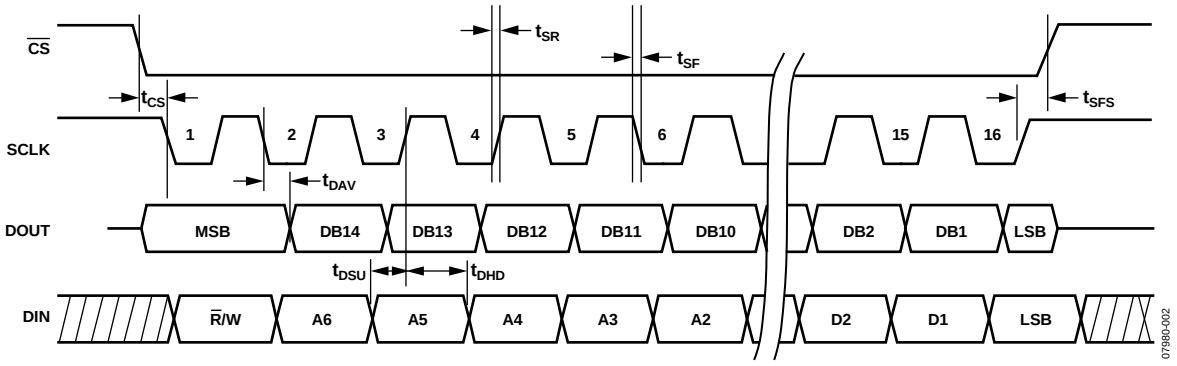


Figure 2. SPI Timing and Sequence

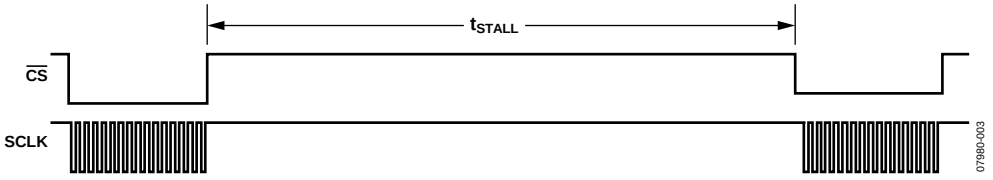


Figure 3. DIN Bit Sequence

ABSOLUTE MAXIMUM RATINGS

Table 3.

Parameter	Rating
Acceleration	
Any Axis, Unpowered	2000 *g*
Any Axis, Powered	2000 *g*
VDD to GND	−0.3 V to +6.0 V
Digital Input Voltage to GND	−0.3 V to +5.3 V
Digital Output Voltage to GND	−0.3 V to VDD + 0.3 V
Analog Inputs to GND	−0.3 V to +3.6 V
Operating Temperature Range	−40°C to +125°C
Storage Temperature Range	−65°C to +125°C

Stresses above those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only; functional operation of the device at these or any other conditions above those indicated in the operational section of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

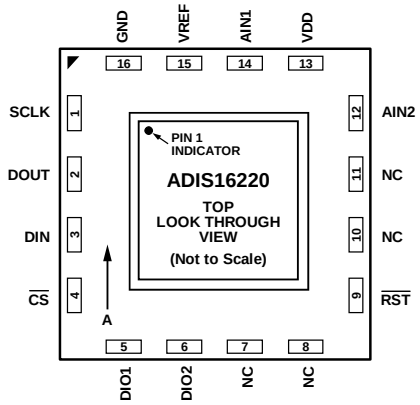
Table 4. Package Characteristics

Package Type	θ_{JA}	θ_{JC}	Device Weight
16-Terminal LGA	250°C/W	25°C/W	0.6 *g*

ESD CAUTION

ESD (electrostatic discharge) sensitive device. Charged devices and circuit boards can discharge without detection. Although this product features patented or proprietary protection circuitry, damage may occur on devices subjected to high energy ESD. Therefore, proper ESD precautions should be taken to avoid performance degradation or loss of functionality.

PIN CONFIGURATION AND FUNCTION DESCRIPTIONS



NOTES
1. NC = NO CONNECT.
2. THIS IS NOT AN ACTUAL TOP VIEW, BECAUSE THE PINS ARE NOT VISIBLE FROM THE TOP. THIS IS A LAYOUT VIEW THAT REPRESENTS THE PIN CONFIGURATION IF THE PACKAGE IS LOOKED THROUGH FROM THE TOP. THIS CONFIGURATION IS PROVIDED FOR PCB LAYOUT PURPOSES.

07980-005

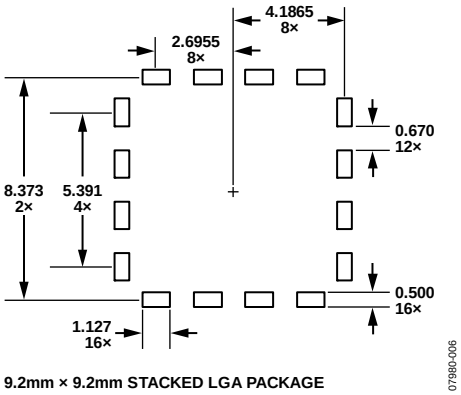
Figure 4. Pin Configuration

Table 5. Pin Function Descriptions

Pin No.	Mnemonic	Type[1]	Description
1	SCLK	I	SPI, Serial Clock.
2	DOUT	O[2]	SPI, Data Output.
3	DIN	I	SPI, Data Input.
4	$\overline{CS}$	I	SPI, Chip Select.
5	DIO1	I/O	Digital Input/Output.
6	DIO2	I/O	Digital Input/Output.
7, 8, 10, 11	NC	N/A	No Connect.
9	$\overline{RST}$	I	Reset, Active Low.
12	AIN2	I	Analog Input Channel 2.
13	VDD	S	Power Supply, 3.3 V.
14	AIN1	I	Analog Input Channel 1.
15	VREF	O	Voltage Reference for AIN1 and AIN2.
16	GND	S	Ground.

[1] S = supply; O = output; I = input; I/O = input/output.
[2] DOUT is an output when $\overline{CS}$ is low. When $\overline{CS}$ is high, DOUT is in a three-state, high impedance mode.

RECOMMENDED PAD LAYOUT



07980-006

Figure 5. Recommended of a Pad Layout

THEORY OF OPERATION

The ADIS16220 is a wide-bandwidth, digital acceleration sensor for vibration analysis. This sensing system collects data autonomously and makes it available to any processor system that supports a 4-wire serial peripheral interface (SPI).

SENSING ELEMENT

Digital vibration sensing in the ADIS16220 starts with a wide-bandwidth MEMS accelerometer core that provides a linear motion-to-electrical transducer function. Figure 6 provides a basic physical diagram of the sensing element and its response to linear acceleration. It uses a fixed frame and a moving frame to form a differential capacitance network that responds to linear acceleration. Tiny springs tether the moving frame to the fixed frame and govern the relationship between acceleration and physical displacement. A modulation signal on the moving plate feeds through each capacitive path into the fixed frame plates and into a demodulation circuit, which produces the electrical signal that is proportional to the acceleration acting on the device.

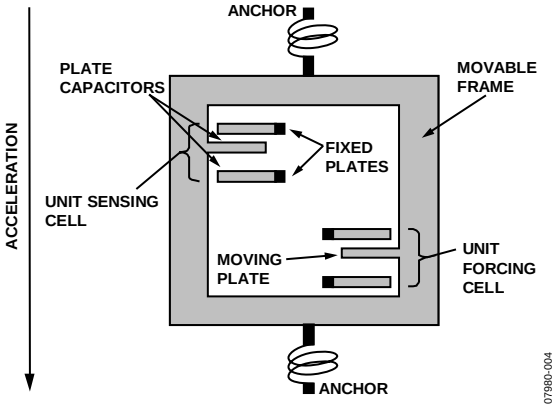


Figure 6. MEMS Sensor Diagram

DATA SAMPLING AND PROCESSING

The analog acceleration signal feeds into an analog-to-digital (ADC) converter stage, which passes digitized data into the controller. The controller processes the acceleration data, stores it in the capture buffer, and manages access to it using the SPI/register user interface. Processing options include offset adjustment, filtering, and checking for preset alarm conditions.

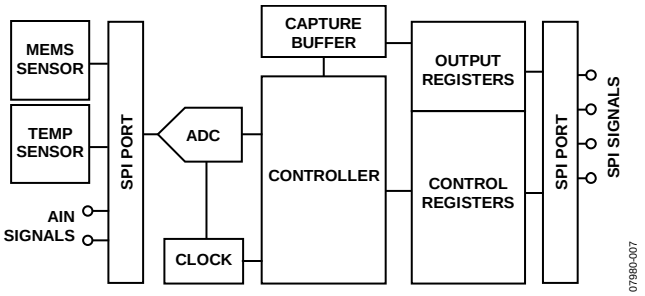


Figure 7. Simplified Sensor Signal Processing Diagram

USER INTERFACE

SPI Interface

The user registers control operation and manage user access to both sensor data and configuration inputs. Each 16-bit register has its own unique bit assignment and has two addresses: one for its upper byte and one for its lower byte. Table 8 provides a memory map for each register, along with their function and lower byte address. Each data collection and configuration commands both use the SPI, which consists of four wires. The chip select ($\overline{CS}$) signal activates the SPI interface and the serial clock (SCLK) synchronizes the serial data lines. Input commands clock into the DIN pin, one bit at a time, on the SCLK rising edge, and output data clocks out of the DOUT pin on the SCLK falling edge. As a SPI slave device, the DOUT contents reflect the information requested using a DIN command.

Dual Memory Structure

The user registers provide addressing for all input/output operations on the SPI interface. The control registers use a dual memory structure. The SRAM controls operation while the part is on, and facilitates all user configuration inputs. The flash memory provides nonvolatile storage for control registers that have flash backup (see Table 8). Storing configuration data in the flash memory requires a manual, flash update command (GLOB_CMD[12] = 1, DIN = 0xBF10). When the device powers on or resets, the flash memory contents load into the SRAM, and then the device starts producing data according to the configuration in the control registers.

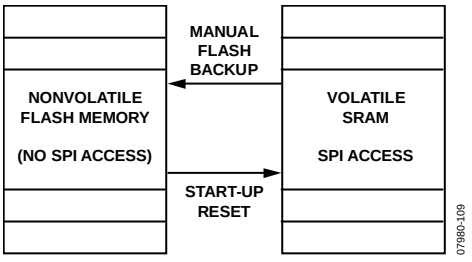


Figure 8. SRAM and Flash Memory Diagram

BASIC OPERATION

The ADIS16220 uses a serial peripheral interface (SPI) for communication, which enables a simple connection with a compatible, embedded processor platform, as shown in Figure 9. The two general-purpose lines provide options for a busy indicator, an alarm indicator, a general-purpose input/output function, and an external capture trigger input.

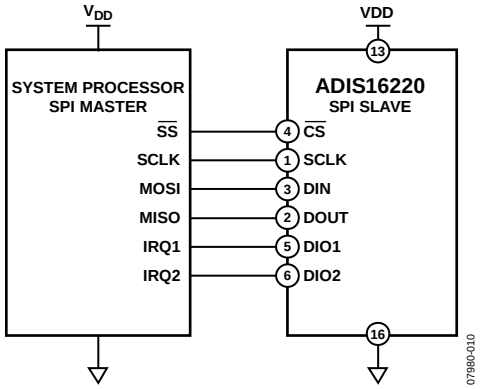


Figure 9. Electrical Hook-Up Diagram

Table 6. Generic Master Processor Pin Names and Functions

Pin Name	Function
$\overline{SS}$	Slave select
IRQ1, IRQ2	Interrupt request inputs
MOSI	Master output, slave input
MISO	Master input, slave output
SCLK	Serial clock

The ADIS16220 SPI interface supports full duplex serial communication (simultaneous transmit and receive) and uses the bit sequence shown in Figure 13. Table 7 provides a list of the most common settings that require attention to initialize a processor's serial port for the ADIS16220 SPI interface.

Table 7. Generic Master Processor SPI Settings

Processor Setting	Description
Master	ADIS16220 operates as a slave
SCLK Rate ≤ 2.25 MHz	Bit rate setting
SPI Mode 3 (1, 1)	Clock polarity/phase (CPOL = 1, CPHA = 1)
MSB-First	Bit sequence
16-Bit	Shift register/data length

The user registers in Table 8 govern all data collection and configuration. Figure 10 provides a generic bit assignment when referencing each registers' bit descriptions.

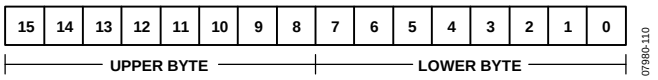


Figure 10. Generic Register Bit Definitions

SPI WRITE COMMANDS

The control registers in Table 8 provide configuration options for a variety of functions. A master processor writes to the registers, one byte at a time, using simple firmware commands and the bit assignments in Figure 13. Because each byte in a register is independent, some functions only require one write cycle. For example, set GLOB_CMD[11] = 1 (DIN = 0xBF08) to start a manual capture sequence. The manual capture starts immediately after the last bit clocks into DIN (16th SCLK rising edge).

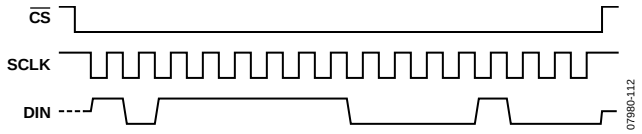


Figure 11. SPI Sequence for Manual Capture Start (DIN = 0xBF08)

SPI READ COMMANDS

A single register read requires two 16-bit SPI cycles, which also use the bit assignments in Figure 13. The first sequence sets $\overline{R}$/W = 0 and communicates the target address (A6:A0). For a read request, D7:D0 are don't care bits. For simplicity, set D7:D0 equal to zero during read request commands. DOUT clocks out during the second sequence. The second sequence can also use DIN to setup the next read. Figure 12 provides a signal diagram for all four SPI signals while reading the acceleration capture buffer (CAPT_BUFA) in a repeating pattern. In this diagram, DIN = 0x1400 and DOUT reflects the CAPT_BUFA register contents.

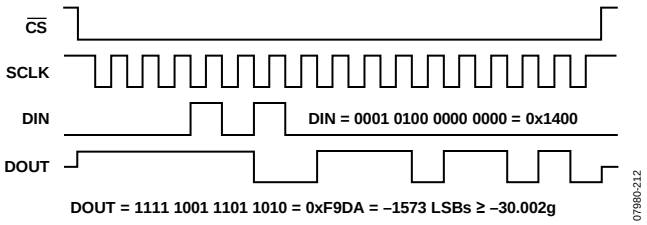


Figure 12. Example SPI Read, Second 16-Bit Sequence

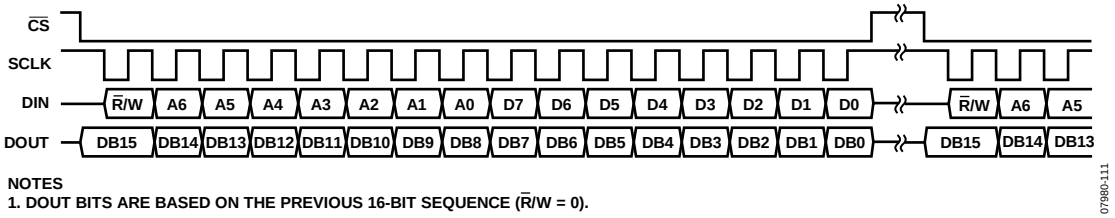


Figure 13. Example SPI Read Sequence

Note that all registers in Table 8 consist of two bytes. All unused memory locations are reserved for future use.

Table 8. User Register Memory Map

Name	Access	Flash Backup	Address[1]	Default	Function	Bit Assignments
FLASH_CNT	Read only	Yes	0x00	N/A	Status, flash memory write count	Table 35
ACCL_NULL	Read/write	Yes	0x02	0x0000	Control, acceleration offset adjustment control	Table 25
AIN1_NULL	Read/write	Yes	0x04	0x0000	Control, AIN1 offset adjustment control	Table 26
AIN2_NULL	Read/write	Yes	0x06	0x0000	Control, AIN2 offset adjustment control	Table 26
			0x08 to 0x09		Reserved	
CAPT_SUPPLY	Read only	Yes	0x0A	0x8000	Output, power supply during capture	Table 10
CAPT_TEMP	Read only	Yes	0x0C	0x8000	Output, temperature during capture	Table 10
CAPT_PEAKA	Read only	Yes	0x0E	0x8000	Output, peak acceleration during capture	Table 10
CAPT_PEAK1	Read only	Yes	0x10	0x8000	Output, peak AIN1 level during capture	Table 10
CAPT_PEAK2	Read only	Yes	0x12	0x8000	Output, peak AIN2 level during capture	Table 10
CAPT_BUFA	Read only	No	0x14	0x8000	Output, capture buffer for acceleration	Table 10
CAPT_BUF1	Read only	No	0x16	0x8000	Output, capture buffer for AIN1	Table 10
CAPT_BUF2	Read only	No	0x18	0x8000	Output, capture buffer for AIN2	Table 10
CAPT_PNTR	Read/write	No	0x1A	0x0000	Control, capture buffer address pointer	Table 9
CAPT_CTRL	Read/write	Yes	0x1C	0x0020	Control, capture control register	Table 15
CAPT_PRD	Read/write	Yes	0x1E	0x0000	Control, capture period (automatic mode)	Table 16
ALM_MAGA	Read/write	Yes	0x20	0x0000	Control, Alarm A, acceleration peak threshold	Table 19
ALM_MAG1	Read/write	Yes	0x22	0x0000	Control, Alarm 1, AIN1 peak threshold	Table 20
ALM_MAG2	Read/write	Yes	0x24	0x0000	Control, Alarm 2, AIN2 peak threshold	Table 20
ALM_MAGS	Read/write	Yes	0x26	0x0000	Control, Alarm S, peak threshold	Table 21
ALM_CTRL	Read/write	Yes	0x28	0x0000	Control, alarm configuration register	Table 18
			0x2A to 0x31		Reserved	
GPIO_CTRL	Read/write	Yes	0x32	0x0000	Control, general I/O configuration	Table 28
MSC_CTRL	Read/write	Yes	0x34	0x0003	Control, self-test control, AIN configuration	Table 30
DIO_CTRL	Read/write	Yes	0x36	0x000F	Control, digital I/O configuration	Table 27
AVG_CNT	Read/write	Yes	0x38	0x0000	Control, filter configuration	Table 24
			0x3A to 0x3B		Reserved	
DIAG_STAT	Read only	Yes	0x3C	0x0000	Status, system status	Table 29
GLOB_CMD	Write only	No	0x3E	N/A	Control, system commands	Table 23
ST_DELTA	Read only	Yes	0x40	N/A	Status, self-test response	Table 31
			0x42 to 0x51		Reserved	
LOT_ID1	Read only	Yes	0x52	N/A	Date code identification	Table 32
LOT_ID2	Read only	Yes	0x54	N/A	Date code identification	Table 33
PROD_ID	Read only	Yes	0x56	0x3F5C	Product identifier; convert to decimal = 16220	N/A
SERIAL_NUM	Read only	Yes	0x58	N/A	Serial number	Table 34

[1] Each register contains two bytes. The address of the lower byte is displayed. The address of the upper byte is equal to the address of the lower byte, plus 1.

DATA COLLECTION

The ADIS16220 samples and stores acceleration (vibration) and analog input signal data using capture events. A capture event involves several sampling/processing operations, as shown in Figure 14. First, the ADIS16220 produces and stores 1024 samples of acceleration and analog input channel data into the capture buffers. Second, the capture event takes a 5.12 ms record of power supply measurements at a sample rate of 50 kHz and loads the average of this record into the CAPT_SUPPLY register. Third, the capture event takes 64 samples of internal temperature data over a period of 1.7 ms and loads the average of this record into CAPT_TEMP.

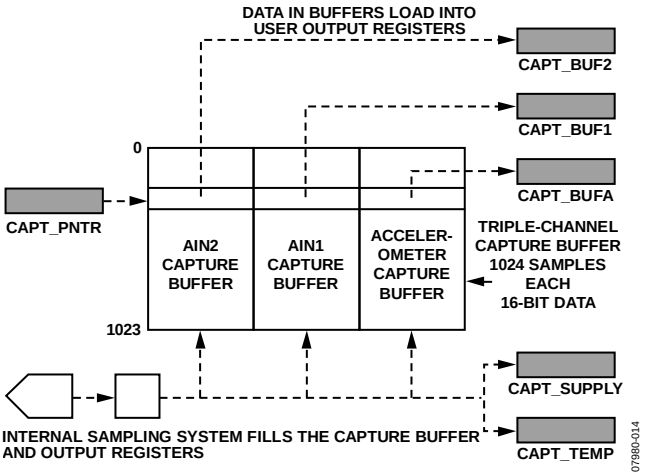


Figure 14. Acceleration Capture Buffer Structure and Operation; CAPT_BUF1 (AIN1) and CAPT_BUF2 (AIN2) Use Similar Structures

READING DATA FROM THE CAPTURE BUFFER

When a capture is complete, the first data samples load into the CAPT_BUFx registers and 0x0000 loads into the index pointer (CAPT_PNTR). The index pointer determines which data samples load into the CAPT_BUFx registers. For example, writing 0x0138 to the CAPT_PNTR register (DIN = 0x9A38, DIN = 0x9B01) causes the 313th sample in the buffer memory to load into the CAPT_BUFx registers.

Table 9. CAPT_PNTR Bits Descriptions

Bit	Description (Default = 0x0000)
[15:10]	Reserved
[9:0]	Data bits

The index pointer automatically increments with a CAPT_BUFA, CAPT_BUF1, or CAPT_BUF2 read command, which causes the next set of capture data to load into each capture buffer register.

Output Data Format

Table 10 offers a summary of the data format used by each output registers. Table 11, Table 12, Table 13, and Table 14 provide example output coding for each register.

Table 10. Capture Output Register Formats

Register	Format[1]	Reference
CAPT_SUPPLY	12-bit binary, 0 V = 0 LSB, 1.2207 mV/LSB	Table 13
CAPT_TEMP	12-bit binary, +25°C = 1278 LSB, −0.47°C/LSB	Table 14
CAPT_BUFA, CAPT_PEAKA	16-bit twos complement 19.073 mg/LSB	Table 11
CAPT_BUF1, CAPT_BUF2, CAPT_PEAK1, CAPT_PEAK2	16-bit twos complement 305.18 µV/LSB	Table 12

[1] 12-bit data formats are LSB justified. Upper four bits are not used in these cases.

Table 11. CAPT_BUFA[1] Data Format Examples

Acceleration (*g*)	LSB	Hex	Output (Binary)
+70	+3670	0x0E56	0000 1110 0101 0111
+0.019073	+1	0x0001	0000 0000 0000 0001
0	0	0x0000	0000 0000 0000 0000
−0.019073	−1	0xFFFF	1111 1111 1111 1111
−70	−3670	0xF1AA	1111 0001 1010 1010

[1] This table also applies to the CAPT_PEAKA register.

Table 12. CAPT_BUF1[1] Data Format Examples

Level (mV)[2]	LSB	Hex	Output (Binary)
VDD/2+1000	+3277	0x0CCD	0000 1100 1100 1101
VDD/2+0.305	+1	0x0001	0000 0000 0000 0001
VDD/2	0	0x0000	0000 0000 0000 0000
VDD/2−0.305	−1	0xFFFF	1111 1111 1111 1111
VDD/2−1000	−3277	0xF333	1111 0011 0011 0011

[1] This table also applies to CAPT_BUF2, CAPT_PEAK1, and CAPT_PEAK2 registers.
[2] This applies for MSC_CTRL = 0x0003. When MSC_CTRL = 0x0000, substitute 3300 mV for VDD.

Table 13. CAPT_SUPPLY Data Format Examples

Supply Level (V)	LSB	Hex	Binary Output
3.6	2949	0xB85	1011 1000 0101
3.3 + 0.0012207	2704	0xA90	1010 1001 0000
3.3	2703	0xA8F	1010 1000 1111
3.3 – 0.0012207	2702	0xA8E	1010 1000 1110
3.15	2580	0xA14	1010 0001 0100

Table 14. CAPT_TEMP Data Format Examples

Temperature (°C)	LSB	Hex	Binary Output
+125	1065	0x429	0100 0100 1001
+25.47	1277	0x4FD	0100 1111 1101
+25	1278	0x4FE	0100 1111 1110
+24.53	1279	0x4FF	0100 1111 1111
−40	1416	0x588	0101 1000 1000

CAPTURE MODE CONFIGURATION

The CAPT_CTRL register (see Table 15) offers three modes of capture operation (manual, automatic, and event), along with a number of configuration features for supporting these modes. All three modes use the start/stop bit, located in GLOB_CMD[11] (see Table 23) to manage the capture operation.

Table 15. CAPT_CTRL Bit Descriptions

Bit	Description (Default = 0x0020)
[15:7]	Reserved
[6]	Automatically store capture buffers to flash upon alarm trigger (1 = enabled)
[5:4]	Pre-event capture length for event mode
	00 = 64 samples
	01 = 128 samples
	10 = 256 samples
	11 = 512 samples
[3:2]	Capture mode
	00 = manual: use GLOB_CMD[11] to start capture
	01 = automatic: use CAPT_PRD[9:0] to set capture period
	10 = event: continuously monitor data for the conditions set in ALM_CTRL, ALM_MAGA, ALM_MAG1, and ALM_MAG2.
	11 = not used
[1]	Power-down between capture events
	1 = enabled, which requires $\overline{CS}$ toggle to wake up
[0]	Reserved

Manual Capture Mode

The factory default configuration for capture mode is the manual mode. In the manual mode, the ADIS16220 waits for a start command to execute the capture event. Set GLOB_CMD[11] = 1 (DIN = 0xBF08) to start a capture in this mode. Once the capture process begins, GLOB_CMD[11] resets to zero and serves as a stop bit, until the capture event completes. Set GLOB_CMD[11] = 1 to stop a capture event that is in progress.

Automatic Capture Mode

In the automatic mode, the ADIS16220 executes capture events periodically, according to the time in CAPT_PRD (see Table 16). Table 17 provides an example for configuring and starting the automatic mode. When the device receives the start command, it executes a capture event, and then starts the countdown for executing the next capture event. Once the automatic mode starts, GLOB_CMD[11] becomes a stop bit.

Table 16. CAPT_PRD Register Bit Descriptions

Bit	Description (Default = 0x0000)
[15:10]	Reserved
[9:8]	Scale
	00 = 1 second/LSB
	01 = 1 minute/LSB
	10 = 1 hour/LSB
[7:0]	Data bits, binary format

Table 17. Example Automatic Mode Configuration Sequence

DIN	Description
0x9F02, 0x9E18	CAPT_PRD[15:8] = 0x02, set time scale to hours CAPT_PRD[7:0] = 0x18, set the capture period to 24 hours
0x9C06	Set the device for trigger mode and enable shutdown
0xBF08	Start: device executes a capture and shuts down

Event Capture Mode

The event mode functions in a manner similar to a single-event trigger on a digital oscilloscope. This mode is useful for capturing shock events and for preshock motion/vibration analysis. Once started, it monitors a continuous stream of real-time data for a preset, event trigger condition. The event trigger settings are in the following registers: ALM_CTRL (see Table 18), ALM_MAGA (see Table 19), and ALM_MAG1/ALM_MAG2 (see Table 20). When the acceleration or analog input signals trip the alarm trigger settings, the device fills the capture buffers with pre-trigger and post-trigger data, according to the pre-trigger configuration in CAPT_CTRL[5:4].

Configuring the device in the event capture mode requires four steps:

1. Select which data channels to enable using ALM_CTRL.
2. Set each threshold using the ALM_MAGx registers.
3. Select event capture mode by setting CAPT_CTRL[3:2] = 10.
4. Start the sampling by setting GLOB_CMD[11] = 1. Table 22 provides an example for configuring the device in this mode. After the continuously sampling starts, setting GLOB_CMD[11] = 1 stops the sampling process.

Table 18. ALM_CTRL Bit Descriptions

Bit	Description (Default = 0x0000)
[15:6]	Reserved
[5]	System alarm comparison polarity
	1 = trigger when less than ALM_MAGS[11:0]
	0 = trigger when greater than ALM_MAGS[11:0]
[4]	System alarm trigger source
	1 = temperature, 0 = power supply
[3]	System alarm enable (ALM_MAGS)
	1 = enabled, 0 = disabled
[2]	AIN2 alarm enable (ALM_MAG2)
	1 = enabled, 0 = disabled
[1]	AIN1 alarm enable (ALM_MAG1)
	1 = enabled, 0 = disabled
[0]	Acceleration alarm enable (ALM_MAGA)
	1 = enabled, 0 = disabled

Table 19. ALM_MAGA Bit Descriptions

Bit	Description (Default = 0x0000)
[15:0]	Data bits for acceleration threshold setting; twos complement, 19.073 mg/LSB. Range = +8191 LSBs/−8192 LSBs.

Table 20. ALM_MAG1 and ALM_MAG2 Bit Descriptions

Bit	Description (Default = 0x0000)
[15:0]	Data bits for AIN1, AIN2 signal threshold setting; twos complement, 305.18 µV/LSB. Range = +8191 LSBs/−8192 LSBs.

Table 21. ALM_MAGS Bit Descriptions

Bit	Description (Default = 0x0000)
[15:12]	Reserved.
[11:0]	Data bits for temperature or supply threshold setting. Binary format matches CAPT_TEMP or CAPT_SUPPLY format, depending on the ALM_CTRL[4] setting.

Each ALM_MAGx register has a corresponding error flag in the DIAG_STAT register for software monitoring of alarm conditions. Note that the system alarm in the ALM_MAGS register (see Table 21) has an error flag in DIAG_STAT[11] but cannot trigger a data capture.

Table 22. Example Event Mode Configuration Sequence

DIN	Description
0xA00C, 0xA102	Set acceleration trigger point at >+10 *g* and <−10 *g* by setting ALM_MAGA = 0x020C.
0xA809	Set the system alarm as a greater-than-temperature configuration and enable both acceleration and system alarms by setting ALM_CTRL[7:0] = 0x09.
0xB61F	Keep DIO1 as a busy indicator and set DIO2 as a positive alarm indicator by setting DIO_CTRL[7:0] = 0x1F.
0x9C5A	Set capture into event mode, enable automatic capture store to flash, enable power-down between captures, and set pre-event capture length to 128 samples by setting CAPT_CTRL[7:0] = 0x5A.
0xBF08	Start the event capture mode by setting GLOB_CMD[11] = 1

Power-Down Control

CAPT_CTRL[1] provides an option to automatically power down the device after a capture event to reduce power consumption. Wake the device from power-down by lowering $\overline{CS}$. The timer in automatic mode can wake the device up as well. Allow for a 2 ms wake-up time after lowering $\overline{CS}$ to wake the device up. Communication with the device while in sleep mode wakes up the device. The device remains awake until after the next capture or until the device is manually put back to sleep. When data is extracted after a capture, the user can command the device to go back to sleep by setting GLOB_CMD[1] = 1 (DIN = 0xBE02). When waking multiple devices, $\overline{CS}$ must occur at different times to avoid conflicts on the DOUT line.

Automatic Flash Back-Up Control

CAPT_CTRL[6] provides an option for automatically storing capture buffer data to a mirror location in the nonvolatile flash memory at the end of a capture. When an alarm condition has been met, the device also performs a system backup, which stores the registers and capture buffers in flash memory. Set GLOB_CMD[13] = 1 (DIN = 0xBF40) to recover these settings from the flash memory.

Use the following equations to estimate capture times:

$$T_C = 0.014 + \frac{1}{97{,}184} \times 1024 \times 2^{AVG\_CNT} \text{ (no flash)}$$

$$T_C = 0.516 + \frac{1}{97{,}184} \times 1024 \times 2^{AVG\_CNT} \text{ (with flash)}$$

See Table 24 for the AVG_CNT setting.

GLOBAL COMMANDS

The GLOB_CMD register provides an array of single-write commands for convenience. Setting the assigned bit in Table 23 to 1 activates each function. When the function completes, the bit restores itself to 0. For example, clear the capture buffers using a single DIN write sequence, DIN = 0xBF01. All of the commands in the GLOB_CMD register require the power supply to be within normal limits for the execution times listed in Table 23. The execution times reflect the factory default configuration where applicable and describe the time required to return to normal operation.

Table 23. GLOB_CMD Bit Descriptions

Bit	Description	Execution Time[1]
[15:14]	Reserved	N/A
[13]	Restore capture data and settings from flash memory	0.88 ms (no capture) 6.91 ms (with capture)
[12]	Copy capture data and settings to flash memory	350 ms (no capture) 502 (with capture)
[11]	Capture mode start/stop	N/A
[10]	Set CAPT_PNTR = 0x0000	0.037 ms
[9]	Reserved	N/A
[8]	Clear capture buffers	0.84 ms
[7]	Software reset	22.7 ms
[6]	Reserved	N/A
[5]	Flash test, compare sum of flash memory with the sum of SRAM	10.5 ms
[4]	Clear DIAG_STAT register	0.035 ms
[3]	Factory setting restore	335 ms
[2]	Self-test	12 ms
[1]	Power-down, requires toggling $\overline{CS}$ low to wake up	N/A
[0]	Autonull	678 ms

[1] This indicates the typical duration of time between the command write and the device returning to normal operation.

FILTERING

The ADIS16220 provides an averaging/decimation filter for lower bandwidth applications that may value finer frequency resolution using the 1024-sample capture buffer.

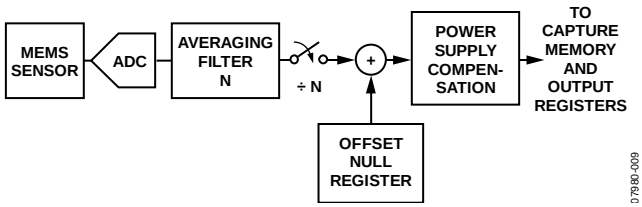


Figure 15. Simplified Signal Processing Flowchart

AVG_CNT[3:0] controls the averaging/decimating filter structure in binomial steps, starting with 1 and ending with 1024. For example, set AVG_CNT[7:0] = 0x08 (DIN = 0xB608) to select 256 averages and a decimation rate of 1/256. Note that the decrease in sample time impacts the total capture time (T_C):

$$AVG\_CNT[7:0] = 0x08 = 8,\ N = 2^8 = 256 \text{ averages}$$

Table 24. AVG_CNT Bit Descriptions

Bit	Description (Default = 0x0000)
[15:4]	Reserved
[3:0]	Power-of-two setting for number of averages, binary

OFFSET ADJUSTMENT

The ACCL_NULL, AIN1_NULL, and AIN2_NULL registers provide a bias adjustment function. For example, setting ACCL_NULL = 0x009D (DIN = 0x829D) increases the acceleration bias by 157 LSB (3 *g*). Set GLOB_CMD[0] = 1 (DIN = 0x3E01) to execute the autonull function, which loads the offset registers with a value derived from a 678 ms average of the acceleration data.

Table 25. ACCL_NULL Bit Descriptions

Bit	Description (Default = 0x0000)
[15:0]	Data bits, twos complement, 19.073 mg/LSB sensitivity. See Figure 15 for impact on output. Range = +8191 LSBs/−8192 LSBs

Table 26. AIN1_NULL and AIN2_NULL Bit Descriptions

Bit	Description (Default = 0x0000)
[15:0]	Data bits, twos complement, 305.18 µV/LSB sensitivity. Signal path is similar to Figure 15. Range = +8191 LSBs/−8192 LSBs

INPUT/OUTPUT FUNCTIONS

DIO1 and DIO2 are configurable as I/O lines that serve multiple purposes. The following register priority governs their operation: DIO_CTRL, then GPIO_CTRL. The DIO_CTRL register has four application-specific configuration options for each signal. The capture trigger input option works in conjunction with the manual capture mode and provides a hardware option for driving a data capture event. When enabled, this function searches for a positive pulse and the capture starts on the falling edge of this pulse. The busy indicator output is active during capture events and can help prevent undesirable interruptions. For example, set DIO_CTRL[5:0] = 101111 (DIN = 0xB62F) to establish DIO2 as a capture trigger input and keep DIO1 as a positive polarity, busy indicator output. Using the busy indicator as an interrupt driver enables the master processor to gather capture data as soon as it is available, without having to poll inputs or estimate execution times. The alarm indicator output is active when the trigger set by ALM_CTRL and ALM_MAGx activates. When configured as general-purpose lines, the GPIO_CTRL register configures DIO1 and DIO2. For example, set GPIO_CTRL = 0x0103 (DIN = 0xB203, then 0xB301) to set DIO1 and DIO2 as outputs, with DIO1 in a 1 state and DIO2 in a 0 state.

Table 27. DIO_CTRL Bit Descriptions

Bit	Description (Default = 0x000F)
[15:6]	Reserved
[5:4]	DIO2 function selection 00 = general-purpose I/O (use GPIO_CTRL) 01 = alarm indicator output (per ALM_CTRL) 10 = capture trigger inputs 11 = busy indicator output
[3:2]	DIO1 function selection 00 = general-purpose I/O (use GPIO_CTRL) 01 = alarm indicator output (per ALM_CTRL) 10 = capture trigger inputs 11 = busy indicator output
[1]	DIO2 line polarity; if [5:4] = 00, see GPIO_CTRL 1 = active high 0 = active low
[0]	DIO1 line polarity; if [3:2] = 00, see GPIO_CTRL 1 = active high 0 = active low

Table 28. GPIO_CTRL Bit Descriptions

Bit	Description (Default = 0x0000)
[15:10]	Reserved
[9]	General-purpose I/O output level, DIO2
[8]	General-purpose I/O output level, DIO1
[7:2]	Reserved
[1]	General-purpose I/O Line, data direction control, DIO2 1 = output, 0 = input
[0]	General-purpose I/O Line, data direction control, DIO1 1 = output, 0 = input

DIAGNOSTICS

In all of the error flags in DIAG_STAT, a 1 identifies an error condition, whereas a 0 signals normal operation. All of the flags remain until the next capture or reset command (GLOB_CMD[4] = 1). DIAG_STAT[1:0] returns to 1 after the next sample (or capture) if the error conditions still exist. DIAG_STAT[14:12] provide flags to check the source of an event capture, prior to reading the entire capture buffer. DIAG_STAT[10:8] offers flags that check the peak values in the capture against the conditions in the ALM_CTRL and ALM_MAGx registers. The flash test produces an error flag in DIAG_STAT[6] to check if the sum of the internal operating memory matches the sum of the same flash memory locations. The capture period violation flag (DIAG_STAT[4]) rises to 1 when the user attempts to use the SPI while a capture sequence is in progress. Using the DIO1 line in the factory default configuration as a busy indicator can help prevent this violation. The SPI communication flag in DIAG_STAT[3] raises to a Logic 1 when the total number of SCLK clocks is not a multiple of 16 during a SPI transfer.

Table 29. DIAG_STAT Bit Descriptions

Bit	Description (Default = 0x0000)
[15]	Reserved
[14]	AIN2 sample > ALM_MAG2
[13]	AIN1 sample > ALM_MAG1
[12]	Acceleration sample > ALM_MAGA
[11]	Error condition programmed into ALM_MAGS[11:0] and ALM_CTRL[5:4] is true
[10]	|Peak value in AIN2 data capture| > ALM_MAG2
[9]	|Peak value in AIN1 data capture| > ALM_MAG1
[8]	|Peak value in acceleration data capture| > ALM_MAGA
[7]	Data ready, capture complete
[6]	Flash test result, checksum flag
[5]	Self-test diagnostic error flag
[4]	Capture period violation/interruption
[3]	SPI communications failure
[2]	Flash update failure
[1]	Power supply above 3.625 V
[0]	Power supply below 3.15 V

Self-Test

The internal MEMS sensing element has an electrostatic self-test function that simulates the physical displacement associated with an acceleration event. There are two options for using this feature to verify the integrity of the accelerometer sensor and signal chain. Set GLOB_CMD[2] = 1 to execute an automatic self-test sequence, which exercises the sensing element, observes the change in output, records it into ST_DELTA, compares it with pre-set minimum/maximum values, and reports the pass/fail result in DIAG_STAT[5].

Another option is to set MSC_CTRL[8] = 1 (see Table 30) to manually activate the sensing element. Then execute a manual capture, which reflects the response associated with the self-test setting.

Table 30. MSC_CTRL Bit Descriptions

Bit	Description (Default = 0x0003)
[15:9]	Reserved
[8]	Self-test enable, set to 1 to activate, (returns to 0 when complete)
[7:2]	Reserved
[1]	Power supply compensation, AIN2 1 = enable, 0 = disable
[0]	Power supply compensation, AIN1 1 = enable, 0 = disable

MSC_CTRL[1:0] provides an option for reducing the sensitivity dependence on power supply for ratiometric sensors, such as the ADXL001.

Table 31. ST_DELTA Bit Descriptions

Bit	Description
[15:0]	Acceleration data, twos complement, 19.073 mg/LSB

SERIALIZATION

LOT_ID1 and LOT_ID2 combine to provide a unique lot code that is 24 bits in length. SERIAL_NUM provides a unique serial number for each device within a given lot.

Table 32. LOT_ID1 Bit Descriptions

Bit	Description
[15:8]	Lot identification code, least significant byte
[7:0]	Reserved for internal use, do not use

Table 33. LOT_ID2 Bit Descriptions

Bit	Description
[15:0]	Lot identification code, most significant bytes

Table 34. SERIAL_NUM Bit Descriptions

Bit	Description
[15:0]	Serial number, lot-specific

FLASH MEMORY MANAGEMENT

The FLASH_CNT register (see Table 35) provides a tool for managing the flash memory's endurance. The FLASH_CNT register increments every time there is a write to the flash memory. Figure 16 quantifies the relationship between data retention and junction temperature.

Table 35. FLASH_CNT Bit Descriptions

Bit	Description
[15:0]	Binary counter for writing to flash memory

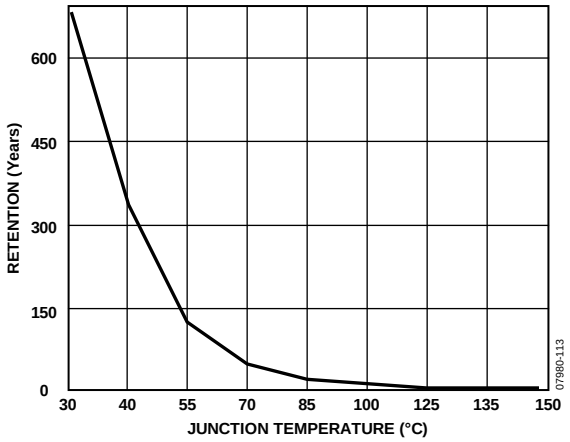


Figure 16. Flash/EE Memory Data Retention

APPLICATIONS INFORMATION

ASSEMBLY

When developing a process flow for installing ADIS16220 devices on PCBs, see the JEDEC standard document J-STD-020C for reflow temperature profile and processing information. The ADIS16220 can use the Sn-Pb eutectic process and the Pb-free eutectic process from this standard. See JEDEC J-STD-033 for moisture sensitivity level (MSL) handling requirements. The MSL rating for these devices is marked on the antistatic bags, which protect these devices from ESD during shipping and handling. Prior to assembly, review the process flow for information about introducing shock levels that exceed the absolute maximum ratings for the ADIS16220. PCB separation and ultrasonic cleaning processes can introduce high levels of shock and can damage the MEMS element. Bowing or flexing the PCB after solder reflow can also place large pealing stress on the pad structure and can damage the device. If this is unavoidable, consider using an underfill material to help distribute these forces across the bottom of the package. Tasca

GETTING STARTED QUICKLY

Once the ADIS16220 has a power supply voltage that reaches 3.15 V, it executes a start-up sequence that places the device in manual capture mode. The following code example initiates a manual data capture by setting GLOB_CMD[11] = 1 (DIN = 0xBF08) and reads all 1024 samples in the acceleration capture buffer, using DIN = 0x1400. The data from the first spi_reg_ read is not valid because this command is starting the process. The second spi_reg_read command (first read inside the embedded For loop) produces the first valid data. This code sequence produces $\overline{CS}$, SCLK, and DIN signals similar to the ones found in Figure 12.

```
spi_write(BF08h);
delay 30ms;
Data(0) = spi_reg_read(14h);
For n = 0 to 1023
  Data(n) = spi_reg_read(14h);
  n = n + 1;
end
```

INTERFACE BOARD

The ADIS16220/PCBZ provides the ADIS16220 function on a 1.2 inch × 1.3 inch printed circuit board (PCB), which simplifies the connection to an existing processor system. The four mounting holes accommodate either M2 (2mm) or Type 2-56 machine screws. These boards are made of IS410 material and are 0.063 inches thick. The second level assembly uses a SAC305-compatible solder composition (Pb-free), which has a presolder reflow thickness of approximately 0.005 inches. The pad pattern on the ADIS16220/PCBZ matches that shown in Figure 5. J1 and J2 are dual-row, 2 mm (pitch) connectors that work with a number of ribbon cable systems, including 3M Part Number 152212-0100-GB (ribbon-crimp connector) and 3M Part Number 3625/12 (ribbon cable).

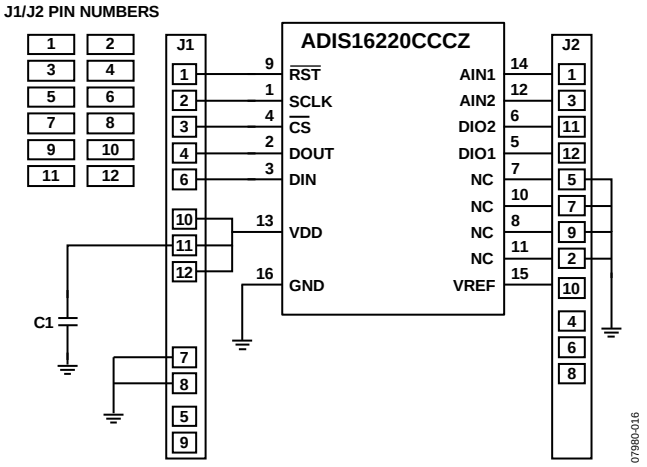


Figure 17. Electrical Schematic

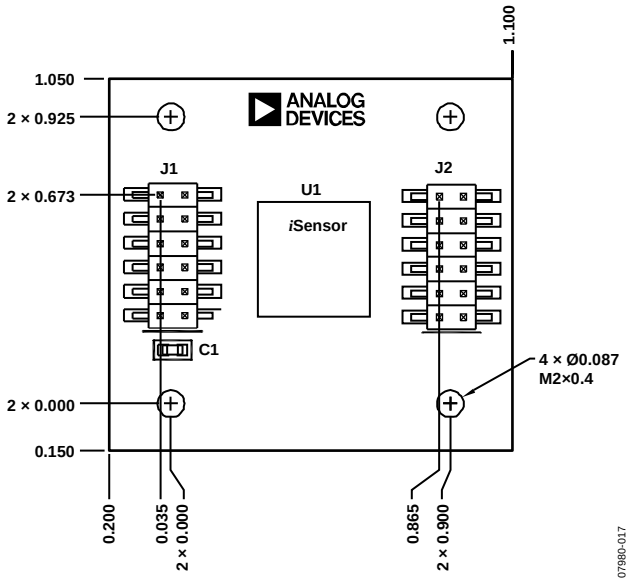


Figure 18. PCB Assembly View and Dimensions

OUTLINE DIMENSIONS

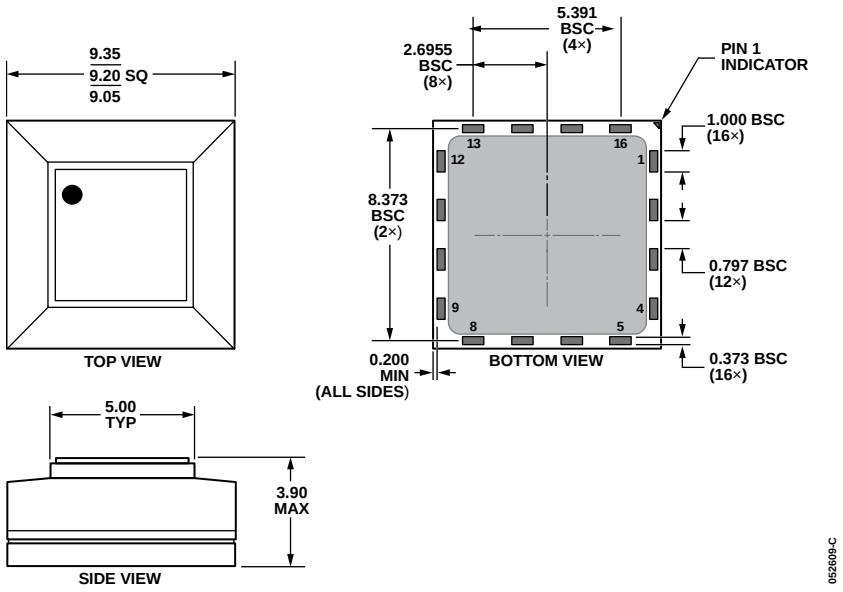


Figure 19. 16-Terminal Stacked Land Grid Array [LGA]
(CC-16-2)
Dimensions shown in millimeters

ORDERING GUIDE

Model[1]	Temperature Range	Package Description	Package Option
ADIS16220CCCZ	–40°C to +125°C	16-Terminal Stacked Land Grid Array [LGA]	CC-16-2
ADIS16220/PCBZ		Evaluation Board	

[1] Z = RoHS Compliant Part.

NOTES

NOTES

NOTES