

OCTAL BUS TRANSCEIVER, 3-STATE INVERTING

查询74HC640, 74HCT640 供应商

FEATURES

- Octal bidirectional bus interface
- Inverting 3-state outputs
- Output capability: bus driver
- ICC category: MSI

GENERAL DESCRIPTION

The 74HC/HCT640 are high-speed Si-gate CMOS devices and are pin compatible with low power Schottky TTL (LSTTL). They are specified in compliance with JEDEC standard no. 7A.

The 74HC/HCT640 are octal transceivers featuring inverting 3-state bus compatible outputs in both send and receive directions.

The "640" features an output enable (OE) input for easy cascading and a send/receive (DIR) for direction control. OE controls the outputs so that the buses are effectively isolated.

The "640" is similar to the "245" but has inverting outputs.

| SYMBOL | PARAMETER | CONDITIONS | TYPICAL | | UNIT |
|-------------------|---|---|---------|-----|------|
| | | | HC | HCT | |
| t_{PHL}/t_{PLH} | propagation delay A_n to B_n ; B_n to A_n | $C_L = 15 \text{ pF}$ $V_{CC} = 5 \text{ V}$ | 9 | 9 | ns |
| C_i | input capacitance | | 3.5 | 3.5 | pF |
| $C_{i/O}$ | input/output capacitance | | 10 | 10 | pF |
| C_{PD} | power dissipation capacitance per transceiver | notes 1 and 2 | 35 | 35 | pF |

$GND = 0 \text{ V}$; $T_{amb} = 25 \text{ }^\circ\text{C}$; $t_r = t_f = 6 \text{ ns}$

Notes

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):

$$P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o) \text{ where:}$$

f_i = input frequency in MHz C_L = output load capacitance in pF

f_o = output frequency in MHz V_{CC} = supply voltage in V

$\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs

2. For HC the condition is $V_I = GND$ to V_{CC}
For HCT the condition is $V_I = GND$ to $V_{CC} - 1.5 \text{ V}$

ORDERING INFORMATION/PACKAGE OUTLINES

20-lead DIL; plastic (SOT146).

20-lead mini-pack; plastic (SO20; SOT163A).

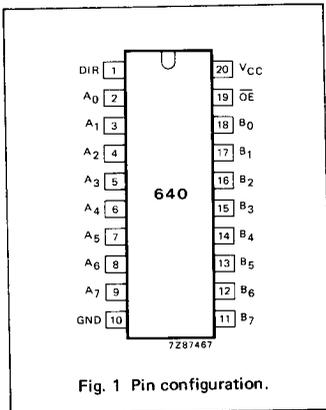


Fig. 1 Pin configuration.

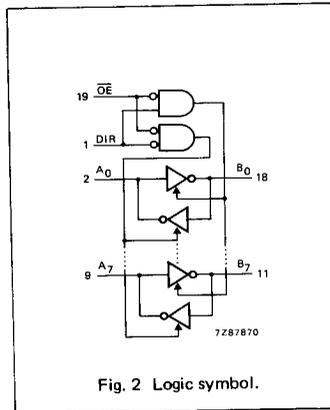


Fig. 2 Logic symbol.

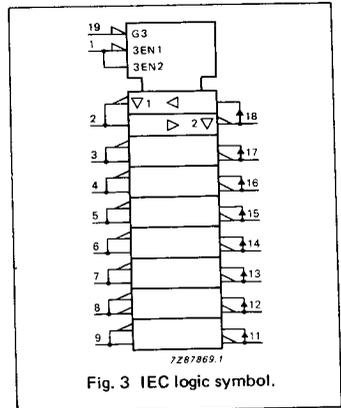


Fig. 3 IEC logic symbol.

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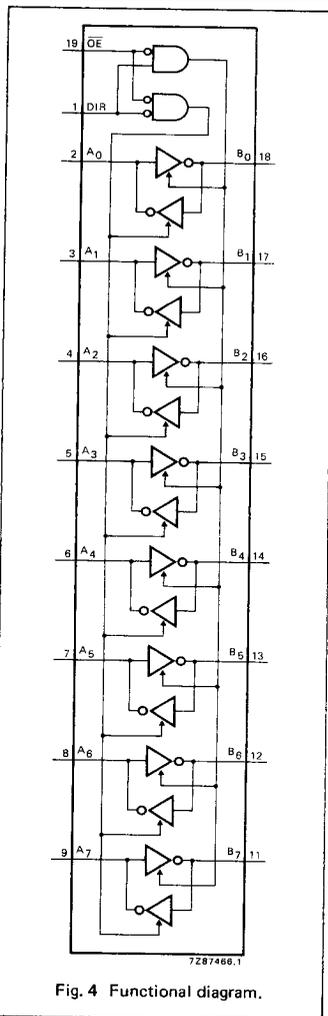


Fig. 4 Functional diagram.

PIN DESCRIPTION

| PIN NO. | SYMBOL | NAME AND FUNCTION |
|--------------------------------|----------------------------------|----------------------------------|
| 1 | DIR | direction control |
| 2, 3, 4, 5, 6, 7, 8, 9 | A ₀ to A ₇ | data inputs/outputs |
| 10 | GND | ground (0 V) |
| 18, 17, 16, 15, 14, 13, 12, 11 | B ₀ to B ₇ | data inputs/outputs |
| 19 | \overline{OE} | output enable input (active LOW) |
| 20 | VCC | positive supply voltage |

FUNCTION TABLE

| inputs | | inputs/outputs | |
|-----------------|-----|--------------------|--------------------|
| \overline{OE} | DIR | A _n | B _n |
| L | L | A = \overline{B} | inputs |
| L | H | inputs | B = \overline{A} |
| H | X | Z | Z |

H = HIGH voltage level
L = LOW voltage level
X = don't care
Z = high impedance OFF-state

[查询"74HC640D-T"供应商](#)**DC CHARACTERISTICS FOR 74HC**

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver

I_{CC} category: MSI**AC CHARACTERISTICS FOR 74HC**GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF

| SYMBOL | PARAMETER | T _{amb} (°C) | | | | | | UNIT | TEST CONDITIONS | | |
|--|---|-----------------------|----------------|-----------------|------------|-----------------|-------------|-----------------|----------------------|-------------------|--------|
| | | 74HC | | | | | | | V _{CC} V | WAVEFORMS | |
| | | +25 | | | -40 to +85 | | -40 to +125 | | | | |
| | | min. | typ. | max. | min. | max. | min. | | max. | | |
| t _{PHL} / t _{PLH} | propagation delay A _n to B _n ; B _n to A _n | | 30 11 9 | 90 18 15 | | 115 23 20 | | 135 27 23 | ns | 2.0 4.5 6.0 | Fig. 5 |
| t _{PZH} / t _{PZL} | 3-state output enable time OE, DIR to A _n ; OE, DIR to B _n | | 44 16 13 | 150 30 26 | | 190 38 33 | | 225 45 38 | ns | 2.0 4.5 6.0 | Fig. 6 |
| t _{PHZ} / t _{PLZ} | 3-state output disable time OE, DIR to A _n ; OE, DIR to B _n | | 50 18 14 | 150 30 26 | | 190 38 33 | | 225 45 38 | ns | 2.0 4.5 6.0 | Fig. 6 |
| t _{THL} / t _{TLH} | output transition time | | 14 5 4 | 60 12 10 | | 75 15 13 | | 90 18 15 | ns | 2.0 4.5 6.0 | Fig. 5 |

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DC CHARACTERISTICS FOR 74HCT

For the DC characteristics see chapter "HCMOS family characteristics", section "Family specifications".

Output capability: bus driver
I_{CC} category: MSI

Note to HCT types

The value of additional quiescent supply current (ΔI_{CC}) for a unit load of 1 is given in the family specifications. To determine ΔI_{CC} per input, multiply this value by the unit load coefficient shown in the table below.

| INPUT | UNIT LOAD COEFFICIENT |
|----------------|-----------------------|
| A _n | 1.50 |
| B _n | 1.50 |
| OE | 1.50 |
| DIR | 0.90 |

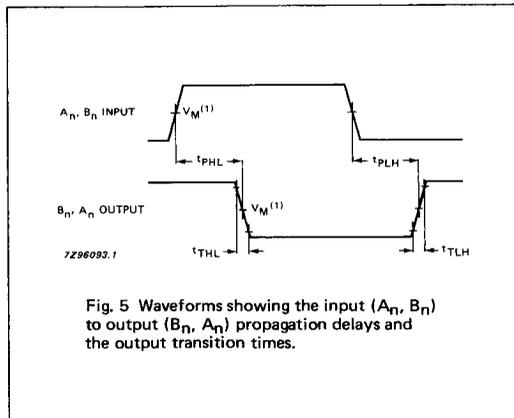
AC CHARACTERISTICS FOR 74HCT

GND = 0 V; t_r = t_f = 6 ns; C_L = 50 pF

| SYMBOL | PARAMETER | T _{amb} (°C) | | | | | | UNIT | TEST CONDITIONS | | |
|--|---|-----------------------|------|------|------------|------|-------------|------|----------------------|-----------|--------|
| | | 74HCT | | | | | | | V _{CC} V | WAVEFORMS | |
| | | +25 | | | -40 to +85 | | -40 to +125 | | | | |
| | | min. | typ. | max. | min. | max. | min. | | | | max. |
| t _{PHL} / t _{PLH} | propagation delay A _n to B _n ; B _n to A _n | | 11 | 22 | | 28 | | 33 | ns | 4.5 | Fig. 5 |
| t _{PZH} / t _{PZL} | 3-state output enable time OE, DIR to A _n ; OE, DIR to B _n | | 18 | 30 | | 38 | | 45 | ns | 4.5 | Fig. 6 |
| t _{PHZ} / t _{PLZ} | 3-state output disable time OE, DIR to A _n ; OE, DIR to B _n | | 19 | 30 | | 38 | | 45 | ns | 4.5 | Fig. 6 |
| t _{THL} / t _{TLH} | output transition time | | 5 | 12 | | 15 | | 18 | ns | 4.5 | Fig. 5 |

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AC WAVEFORMS



Note to AC waveforms

- (1) HC : $V_M = 50\%$; $V_I = \text{GND to } V_{CC}$.
HCT: $V_M = 1.3 \text{ V}$; $V_I = \text{GND to } 3 \text{ V}$.

