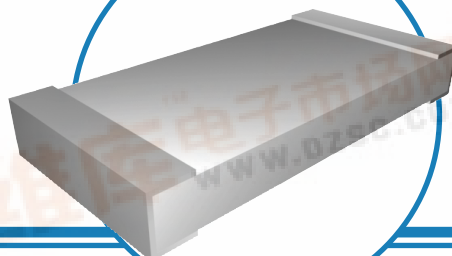


Pulse Withstanding Chip Resistors



PWC Series

- Higher power ratings
- Improved working voltage ratings
- Excellent pulse withstanding performance
- Sn/Pb or Pb-free wrap-around terminations
- Standard chip sizes available from 0805 to 2512



Electrical Data

Characteristic	0805	1206	2010	2512
Resistance Range	1.0Ω to 10MΩ			
±1%, ±5%	10Ω to 1MΩ			
±0.5%				
Power @ 70°C	125mW	500mW	1.0W	2.0W
Max Voltage Rating	150V	200V	400V	500V
Absolute TCR	<6Ω = 0 – 350ppm; ≥6Ω = ±100ppm/°C			
Operating Temperature	-55°C to +155°C			
Thermal Impedance	220°C/W	160°C/W	80°C/W	40°C/W
Pad/Trace Area	40mm ² *	125mm ² *	250mm ² *	500mm ² *
Termination	Wrap-around Sn/Pb or Pb-free with leach resistant Ni barrier			

*Recommended minimum pad and adjacent trace area for each termination for rated power on FR4 PCB.

Environmental Data

Test	Maximum ¹ ΔR	Typical ΔR
Load life at rated power (1000 hours @ 70°C)	1.00%	0.25%
Overload (5.0 X rated power for 2512, 6.25 X rated power for other sizes, 5 secs)	1.00%	0.10%
High temperature storage (1000 hours @ 155°C)	1.00%	0.20%
Moisture resistance	1.00%	0.25%
Thermal shock	0.25%	0.05%
Resistance to soldering heat	0.25%	0.05%

Note 1: 0.01Ω added for all resistance values <10Ω.

General Note

IRC reserves the right to make changes in product specification without notice or liability. All information is subject to IRC's own data and is considered accurate at time of going to print.

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PWC Series Issue January 2009



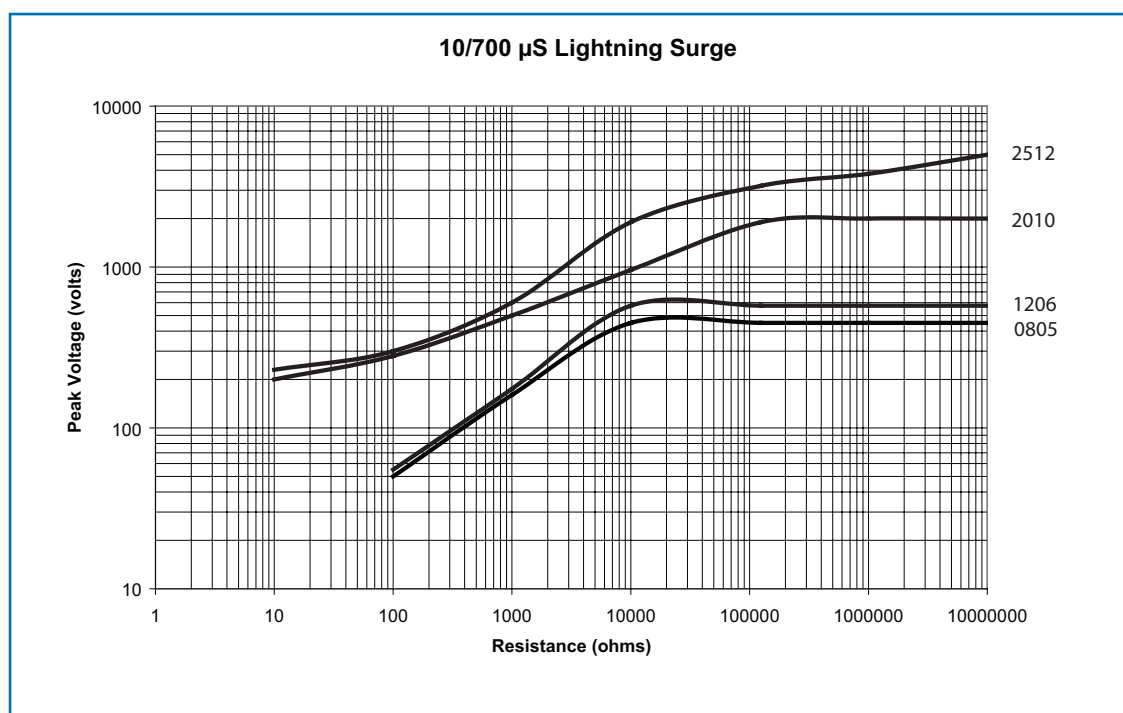
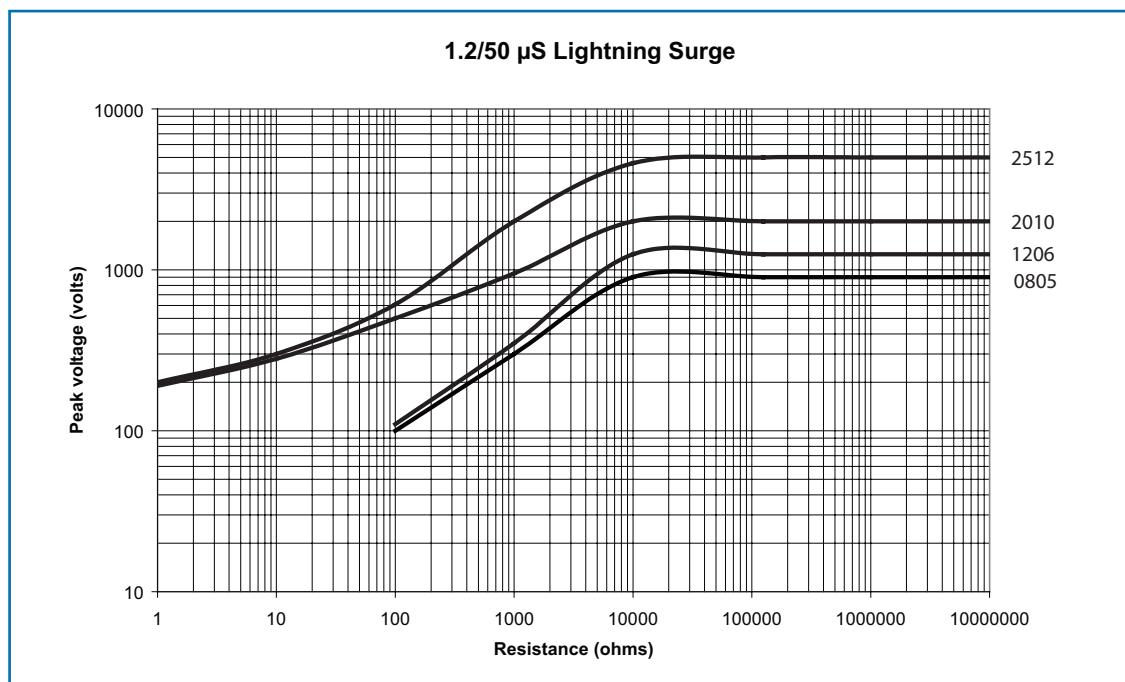
Pulse Withstanding Chip Resistors



Pulse Performance Data

Lighting Surge

Resistors are tested in accordance with IEC 60 115-1 using both 1.2/50 μ s and 10/700 μ s pulse shapes. The limit of acceptance is a shift in resistance of less than 1% from the initial value.



Pulse Withstanding Chip Resistors



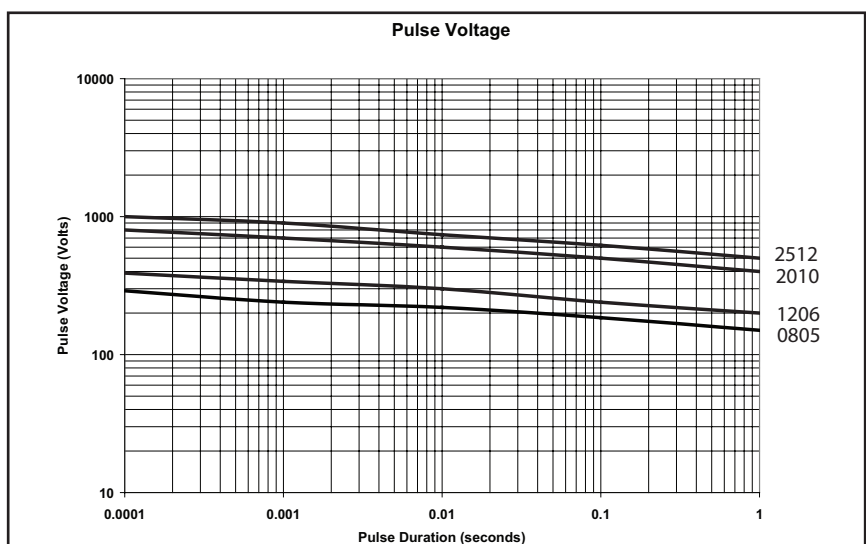
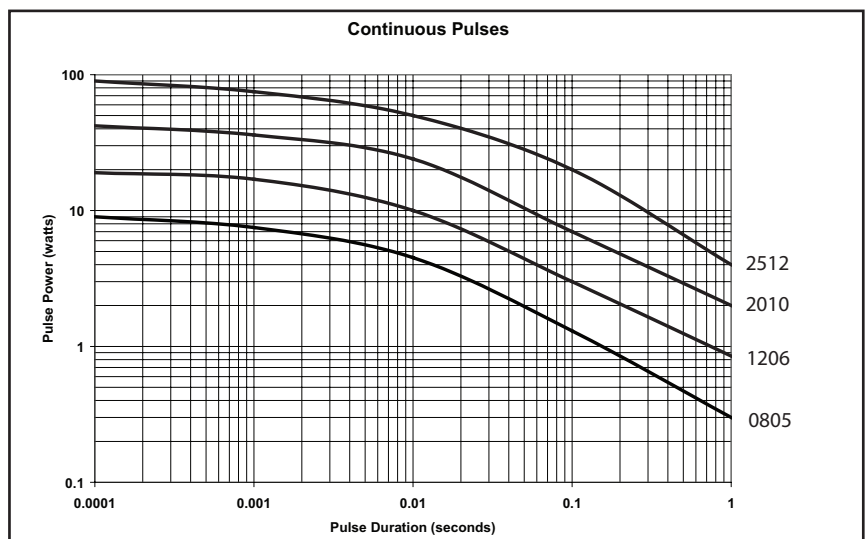
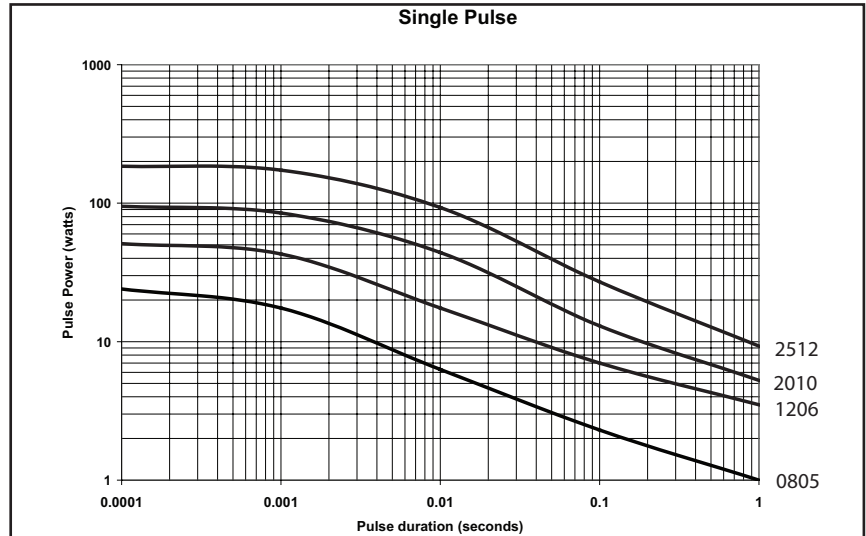
Pulse Performance Data

Single impulse:

The single impulse graph is the result of 50 impulses of rectangular shape applied at one minute intervals. The limit of acceptance was a shift in resistance of less than 1% from the initial value. The power applied was subject to the restrictions of the maximum permissible impulse voltage graph shown.

Continuous load due to repetitive pulses:

The continuous load graph was obtained by applying repetitive rectangular pulses where the pulse period was adjusted so that the average power dissipated in the resistor was equal to its rated power at 70°C. Again the limit of acceptance was a shift in resistance of less than 1% from the initial value.



Pulse Withstanding Chip Resistors



Physical Data

	L (mm)	W (mm)	T max (mm)	A (mm)	B min (mm)	C (mm)	Weight (grams)	
0805	2.0±0.3	1.25±0.2	0.6	0.3±0.15	0.9	0.3±0.1	0.009	
1206	3.2±0.4	1.6±0.2	0.7	0.4±0.2	1.7	0.4±0.15	0.020	
2010	5.1±0.3	2.5±0.2	0.8	0.6±0.3	3.0	0.6±0.25	0.036	
2512	6.5±0.3	3.2±0.2	0.8	0.6±0.3	4.4	0.6±0.25	0.055	

Construction:

Thick film resistor material, overglaze and organic protection are screen printed on a 96% alumina substrate. Wrap-around terminations have an electroplated nickel barrier and tin-lead solder or matte-tin finish, ensuring excellent 'leach' resistance properties and solderability.

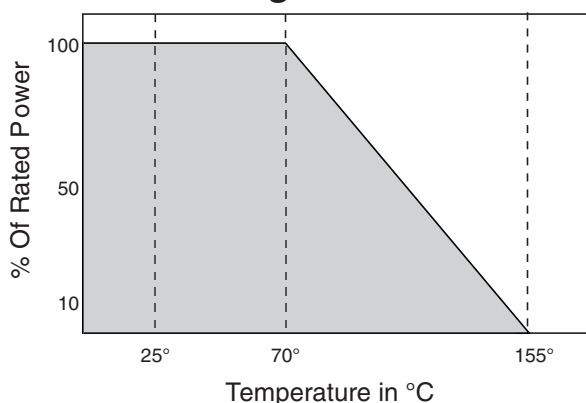
Marking:

Components are not marked. Reels are marked with type, value, tolerance, date code and quantity.

Solvent resistance:

The body protection is resistance to all normal industrial cleaning solvents suitable for printed circuits.

Power Derating Data



Ordering Data

Prefix **PWC** - **PWC** **2512LF** - **100R** - **F**

Chip Type
PWC

Chip Size and Termination

0805 = Sn/Pb solder termination
0805LF = 100% Tin (pb-free) termination
1206 = Sn/Pb solder termination
1206LF = 100% Tin (pb-free) termination
2010 = Sn/Pb solder termination
2010LF = 100% Tin (pb-free) termination
2512 = Sn/Pb solder termination
2512LF = 100% Tin (pb-free) termination

Resistance Value (Use IEC62 code)

Tolerance Code
J = ±5%; F = ±1%; D = ±0.5%

For additional information or to discuss your specific requirements, please contact our Applications Team using the contact details below.

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