



December 2001  
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## 74ALVC16839

### Low Voltage 20-Bit Selectable Register/Buffer with 3.6V Tolerant Inputs and Outputs

#### General Description

The ALVC16839 contains twenty non-inverting selectable buffered or registered paths. The device can be configured to operate in a registered, or flow through buffer mode by utilizing the register enable (REGE) and Clock (CLK) signals. The device operates in a 20-bit word wide mode. All outputs can be placed into 3-STATE through use of the  $\overline{OE}$  pin. These devices are ideally suited for buffered or registered 168 pin and 200 pin SDRAM DIMM memory modules.

The 74ALVC16839 is designed for low voltage (1.65V to 3.6V)  $V_{CC}$  applications with I/O compatibility up to 3.6V.

The 74ALVC16839 is fabricated with an advanced CMOS technology to achieve high speed operation while maintaining low CMOS power dissipation.

#### Features

- Compatible with PC100 and PC133 DIMM module specifications
- 1.65V to 3.6V  $V_{CC}$  supply operation
- 3.6V tolerant inputs and outputs
- $t_{PD}$  (CLK to  $O_n$ )
  - 3.7 ns max for 3.0V to 3.6V  $V_{CC}$
  - 4.9 ns max for 2.3V to 2.7V  $V_{CC}$
  - 8.8 ns max for 1.65V to 1.95V  $V_{CC}$
- Power-off high impedance inputs and outputs
- Supports live insertion and withdrawal (Note 1)
- Uses patented noise/EMI reduction circuitry
- Latchup conforms to JEDEC JED78
- ESD performance:
  - Human body model > 2000V
  - Machine model > 200V

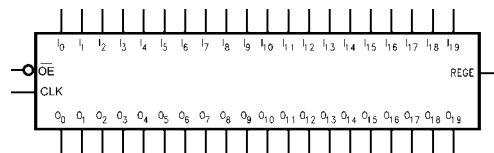
**Note 1:** To ensure the high-impedance state during power up or power down,  $\overline{OE}$  should be tied to  $V_{CC}$  through a pull-up resistor; the minimum value of the resistor is determined by the current-sourcing capability of the driver.

#### Ordering Code:

Order Number	Package Number	Package Descriptions
74ALVC16839MTD	MTD56	56-Lead Thin Shrink Small Outline Package (TSSOP), JEDEC MO-153, 6.1mm Wide

Devices also available in Tape and Reel. Specify by appending suffix letter "X" to the ordering code.

#### Logic Symbol



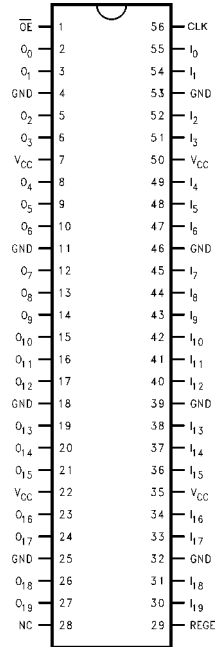
#### Pin Descriptions

Pin Names	Description
$\overline{OE}$	Output Enable Input (Active LOW)
$I_0-I_{19}$	Inputs
$O_0-O_{19}$	Outputs
CLK	Clock Input
REGE	Register Enable Input

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**Connection Diagram**



**Truth Table**

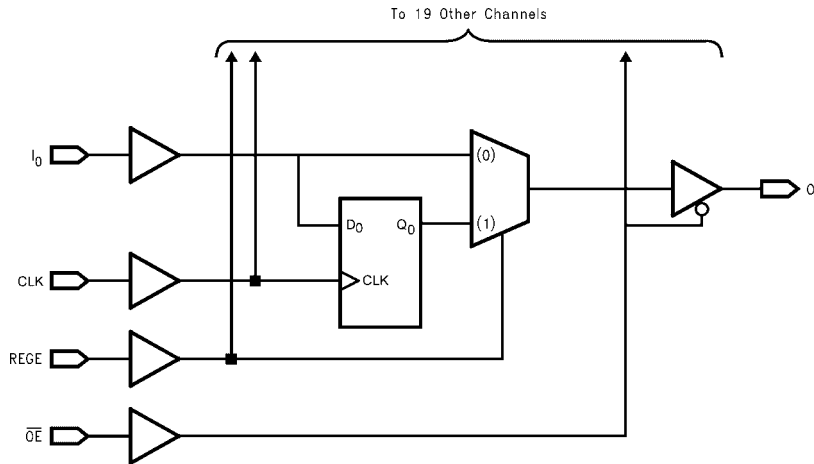
Inputs				Outputs
CLK	REGE	I <sub>n</sub>	OE	O <sub>n</sub>
↑	H	H	L	H
↑	H	L	L	L
X	L	H	L	H
X	L	L	L	L
X	X	X	H	Z

H = Logic HIGH  
 L = Logic LOW  
 X = Don't Care, but not floating  
 Z = High Impedance  
 ↑ = LOW-to-HIGH Clock Transition

**Functional Description**

The 74ALVC16839 consists of twenty selectable non-inverting buffers or registers with word wide modes. Mode functionality is selected through operation of the CLK and REGE pin as shown by the truth table. When REGE is held at a logic HIGH the device operates as a 20-bit register. Data is transferred from I<sub>n</sub> to O<sub>n</sub> on the rising edge of the CLK input. When the REGE pin is held at a logic LOW the device operates in a flow through mode and data propagates directly from the I<sub>n</sub> to the O<sub>n</sub> outputs. All outputs can be 3-stated by holding the OE pin at a logic HIGH.

**Logic Diagram**



Absolute Maximum Ratings (Note 2)		Recommended Operating Conditions (Note 4)				
Supply Voltage ( $V_{CC}$ )	-0.5V to +4.6V	Power Supply	Operating 1.65V to 3.6V			
DC Input Voltage ( $V_I$ )	-0.5V to 4.6V	Input Voltage ( $V_I$ )	0V to $V_{CC}$			
Output Voltage ( $V_O$ ) (Note 3)	-0.5V to $V_{CC} + 0.5V$	Output Voltage ( $V_O$ )	0V to $V_{CC}$			
DC Input Diode Current ( $I_{IK}$ )		Free Air Operating Temperature ( $T_A$ )	-40°C to +85°C			
$V_I < 0V$	-50 mA	Minimum Input Edge Rate ( $\Delta t/\Delta V$ )				
DC Output Diode Current ( $I_{OK}$ )		$V_{IN} = 0.8V$ to $2.0V$ , $V_{CC} = 3.0V$	10 ns/V			
$V_O < 0V$	-50 mA	<b>Note 2:</b> The Absolute Maximum Ratings are those values beyond which the safety of the device cannot be guaranteed. The device should not be operated at these limits. The parametric values defined in the Electrical Characteristics tables are not guaranteed at the Absolute Maximum Ratings. The "Recommended Operating Conditions" table will define the conditions for actual device operation.				
DC Output Source/Sink Current ( $I_{OH}/I_{OL}$ )	$\pm 50$ mA	<b>Note 3:</b> $I_O$ Absolute Maximum Rating must be observed.				
DC $V_{CC}$ or GND Current per Supply Pin ( $I_{CC}$ or GND)	$\pm 100$ mA	<b>Note 4:</b> Floating or unused inputs must be held HIGH or LOW.				
Storage Temperature Range ( $T_{STG}$ )	-65°C to +150°C					
<b>DC Electrical Characteristics</b>						
Symbol	Parameter	Conditions	$V_{CC}$ (V)	Min	Max	Units
$V_{IH}$	HIGH Level Input Voltage		1.65 - 1.95 2.3 - 2.7 2.7 - 3.6	0.65 x $V_{CC}$ 1.7 2.0		V
$V_{IL}$	LOW Level Input Voltage		1.65 - 1.95 2.3 - 2.7 2.7 - 3.6		0.35 x $V_{CC}$ 0.7 0.8	V
$V_{OH}$	HIGH Level Output Voltage	$I_{OH} = -100 \mu A$	1.65 - 3.6	$V_{CC} - 0.2$		V
		$I_{OH} = -4$ mA	1.65	1.2		
		$I_{OH} = -6$ mA	2.3	2		
		$I_{OH} = -12$ mA	2.3 2.7 3.0	1.7 2.2 2.4		
		$I_{OH} = -24$ mA	3.0	2		
$V_{OL}$	LOW Level Output Voltage	$I_{OL} = 100 \mu A$	1.65 - 3.6		0.2	V
		$I_{OL} = 4$ mA	1.65		0.45	
		$I_{OL} = 6$ mA	2.3		0.4	
		$I_{OL} = 12$ mA	2.3 2.7		0.7 0.4	
		$I_{OL} = 24$ mA	3		0.55	
$I_I$	Input Leakage Current	$0 \leq V_I \leq 3.6V$	3.6		$\pm 5.0$	$\mu A$
$I_{OZ}$	3-STATE Output Leakage	$0 \leq V_O \leq 3.6V$	3.6		$\pm 10$	$\mu A$
$I_{CC}$	Quiescent Supply Current	$V_I = V_{CC}$ or GND, $I_O = 0$	3.6		40	$\mu A$
$\Delta I_{CC}$	Increase in $I_{CC}$ per Input	$V_{IH} = V_{CC} - 0.6V$	3 - 3.6		750	$\mu A$

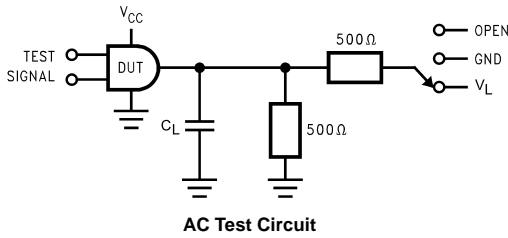
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AC Electrical Characteristics										
Symbol	Parameter	T <sub>A</sub> = -40°C to +85°C, R <sub>L</sub> = 500Ω								Units
		C <sub>L</sub> = 50 pF				C <sub>L</sub> = 30 pF				
		V <sub>CC</sub> = 3.3V ± 0.3V		V <sub>CC</sub> = 2.7V		V <sub>CC</sub> = 2.5V ± 0.2V		V <sub>CC</sub> = 1.8V ± 0.15V		
		Min	Max	Min	Max	Min	Max	Min	Max	
t <sub>MAX</sub>	Maximum Clock Frequency	250		200		200		100		ns
t <sub>PHL</sub> , t <sub>PLH</sub>	Propagation Delay Bus to Bus (REGE = 0)	1.3	3.0	1.5	4.0	1.0	3.5	1.5	7.0	ns
t <sub>PHL</sub> , t <sub>PLH</sub>	Propagation Delay CLK to Bus (REGE = 1)	1.3	3.7	1.5	4.9	1.0	4.4	1.5	8.8	ns
t <sub>PHL</sub> , t <sub>PLH</sub>	Propagation Delay REGE to Bus	1.3	4.5	1.5	5.5	1.0	5.0	1.5	8.8	ns
t <sub>PZL</sub> , t <sub>PZH</sub>	Output Enable Time	1.3	4.3	1.5	5.4	1.0	4.9	1.5	9.8	ns
t <sub>PLZ</sub> , t <sub>PHZ</sub>	Output Disable Time	1.3	4.2	1.5	4.7	1.0	4.2	1.5	7.6	ns
t <sub>W</sub>	Pulse Width	1.5		1.5		1.5		4.0		ns
t <sub>S</sub>	Setup Time	1.0		1.0		1.0		2.5		ns
t <sub>H</sub>	Hold Time	0.7		0.7		0.7		1.0		ns

Capacitance						
Symbol	Parameter	Conditions	T <sub>A</sub> = +25°C		Units	
			V <sub>CC</sub>	Typical		
C <sub>IN</sub>	Input Capacitance	V <sub>I</sub> = 0V or V <sub>CC</sub>	3.3	6	pF	
C <sub>OUT</sub>	Output Capacitance	V <sub>I</sub> = 0V or V <sub>CC</sub>	3.3	7	pF	
C <sub>PD</sub>	Power Dissipation Capacitance	Outputs Enabled	f = 10 MHz, C <sub>L</sub> = 50 pF	3.3	20	pF
				2.5	20	

**AC Loading and Waveforms**

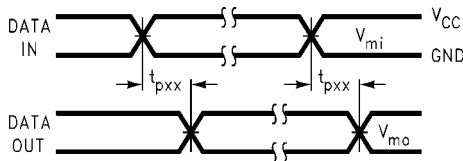


**TABLE 1. Values for Figure**

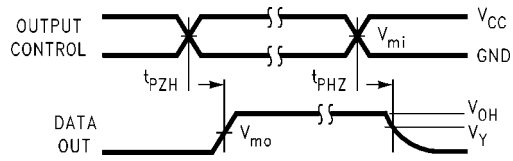
TEST	SWITCH
$t_{PLH}$ , $t_{PHL}$	Open
$t_{PZL}$ , $t_{PLZ}$	$V_L$
$t_{PZH}$ , $t_{PHZ}$	GND

**TABLE 2. Variable Matrix**  
(Input Characteristics:  $f = 1\text{MHz}$ ;  $t_r = t_f = 2\text{ns}$ ;  $Z_0 = 50\Omega$ )

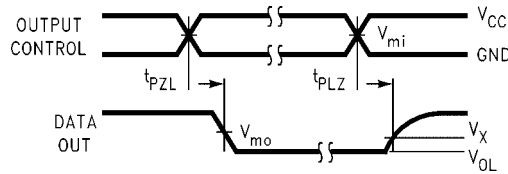
Symbol	$V_{CC}$			
	$3.3\text{V} \pm 0.3\text{V}$	$2.7\text{V}$	$2.5\text{V} \pm 0.2\text{V}$	$1.8\text{V} \pm 0.15\text{V}$
$V_{mi}$	1.5V	1.5V	$V_{CC}/2$	$V_{CC}/2$
$V_{mo}$	1.5V	1.5V	$V_{CC}/2$	$V_{CC}/2$
$V_X$	$V_{OL} + 0.3\text{V}$	$V_{OL} + 0.3\text{V}$	$V_{OL} + 0.15\text{V}$	$V_{OL} + 0.15\text{V}$
$V_Y$	$V_{OH} - 0.3\text{V}$	$V_{OH} - 0.3\text{V}$	$V_{OH} - 0.15\text{V}$	$V_{OH} - 0.15\text{V}$
$V_L$	6V	6V	$V_{CC} * 2$	$V_{CC} * 2$



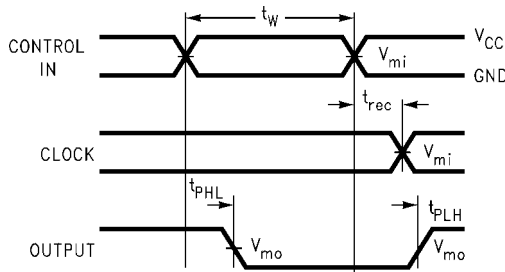
**FIGURE 1. Waveform for Inverting and Non-Inverting Functions**



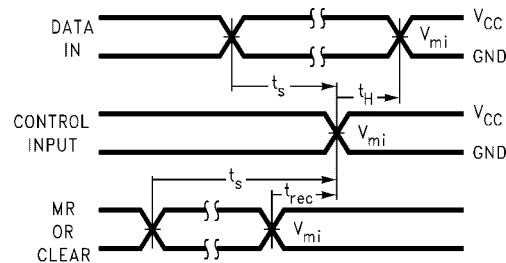
**FIGURE 2. 3-STATE Output High Enable and Disable Times for Low Voltage Logic**



**FIGURE 3. 3-STATE Output Low Enable and Disable Times for Low Voltage Logic**



**FIGURE 4. Propagation Delay, Pulse Width and  $t_{rec}$  Waveforms**



**FIGURE 5. Setup Time, Hold Time and Recovery Time for Low Voltage Logic**

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