

B-Suffix Series CMOS Gates

The B Series logic gates are constructed with P-Channel and N-Channel enhancement mode devices in a single monolithic structure (Complementary MOS). Their primary use is where low power dissipation and/or high noise immunity is desired.

Features

- Supply Voltage Range = 3.0 Vdc to 18 Vdc
- All Outputs Buffered
- Capable of Driving Two Low-Power TTL Loads or One Low-Power Schottky TTL Load Over the Rated Temperature Range
- Double Diode Protection on All Inputs
- Pin-for-Pin Replacements for Corresponding CD4000 Series B Suffix Devices
- Pb-Free Packages are Available

MAXIMUM RATINGS (Voltages Referenced to V_{SS})

Symbol	Parameter	Value	Unit
V_{DD}	DC Supply Voltage Range	-0.5 to +18.0	V
V_{in}, V_{out}	Input or Output Voltage Range (DC or Transient)	-0.5 to $V_{DD} + 0.5$	V
I_{in}, I_{out}	Input or Output Current (DC or Transient) per Pin	± 10	mA
P_D	Power Dissipation, per Package (Note 1)	500	mW
T_A	Ambient Temperature Range	-55 to +125	°C
T_{stg}	Storage Temperature Range	-65 to +150	°C
T_L	Lead Temperature (8-Second Soldering)	260	°C

Stresses exceeding Maximum Ratings may damage the device. Maximum Ratings are stress ratings only. Functional operation above the Recommended Operating Conditions is not implied. Extended exposure to stresses above the Recommended Operating Conditions may affect device reliability.

1. Temperature Derating:

Plastic "P and D/DW" Packages: - 7.0 mW/°C From 65°C To 125°C

This device contains protection circuitry to guard against damage due to high static voltages or electric fields. However, precautions must be taken to avoid applications of any voltage higher than maximum rated voltages to this high-impedance circuit. For proper operation, V_{in} and V_{out} should be constrained to the range $V_{SS} \leq (V_{in} \text{ or } V_{out}) \leq V_{DD}$.

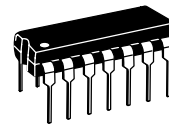
Unused inputs must always be tied to an appropriate logic voltage level (e.g., either V_{SS} or V_{DD}). Unused outputs must be left open.



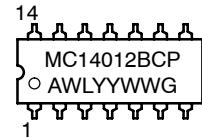
ON Semiconductor®

<http://onsemi.com>

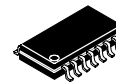
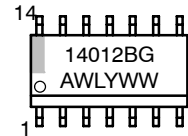
MARKING DIAGRAMS



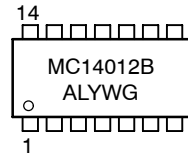
PDIP-14
P SUFFIX
CASE 646



SOIC-14
D SUFFIX
CASE 751A



SOEIAJ-14
F SUFFIX
CASE 965



A = Assembly Location
WL, L = Wafer Lot
YY, Y = Year
WW, W = Work Week
G = Pb-Free Package

ORDERING INFORMATION

See detailed ordering and shipping information in the package dimensions section on page 2 of this data sheet.

MC14012B

[查询"MC14012BCP"供应商](#)

MC14012B
Dual 4-Input NAND Gate

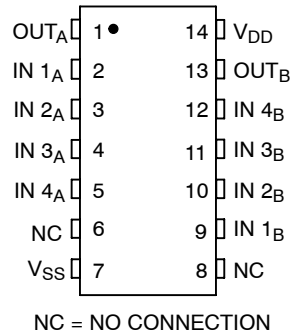


Figure 1. Pin Assignment

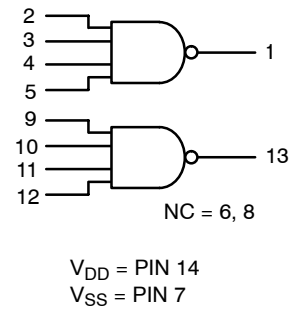


Figure 2. Logic Diagram

ORDERING INFORMATION

Device	Package	Shipping [†]
MC14012BCP	PDIP-14	25 Units / Rail
MC14012BCPG	PDIP-14 (Pb-Free)	
MC14012BD	SOIC-14	55 Units / Rail
MC14012BDG	SOIC-14 (Pb-Free)	
MC14012BDR2	SOIC-14	2500 Units / Tape & Reel
MC14012BDR2G	SOIC-14 (Pb-Free)	
MC14012BFEL	SOEIAJ-14	2000 Units / Tape & Reel
MC14012BFELG	SOEIAJ-14 (Pb-Free)	

[†]For information on tape and reel specifications, including part orientation and tape sizes, please refer to our Tape and Reel Packaging Specifications Brochure, BRD8011/D.

MC14012B

ELECTRICAL CHARACTERISTICS (Voltages Referenced to V_{SS})

查询"MC14012BCP"供应商

Characteristic	Symbol	V _{DD} Vdc	- 55° C		25° C			125° C		Unit
			Min	Max	Min	Typ (Note 2)	Max	Min	Max	
Output Voltage V _{in} = V _{DD} or 0	“0” Level V _{OL}	5.0	–	0.05	–	0	0.05	–	0.05	Vdc
		10	–	0.05	–	0	0.05	–	0.05	
		15	–	0.05	–	0	0.05	–	0.05	
	“1” Level V _{OH}	5.0	4.95	–	4.95	5.0	–	4.95	–	Vdc
		10	9.95	–	9.95	10	–	9.95	–	
		15	14.95	–	14.95	15	–	14.95	–	
Input Voltage (V _O = 4.5 or 0.5 Vdc) (V _O = 9.0 or 1.0 Vdc) (V _O = 13.5 or 1.5 Vdc)	“0” Level V _{IL}	5.0	–	1.5	–	2.25	1.5	–	1.5	Vdc
		10	–	3.0	–	4.50	3.0	–	3.0	
		15	–	4.0	–	6.75	4.0	–	4.0	
	“1” Level V _{IH}	5.0	3.5	–	3.5	2.75	–	3.5	–	Vdc
		10	7.0	–	7.0	5.50	–	7.0	–	
		15	11	–	11	8.25	–	11	–	
Output Drive Current (V _{OH} = 2.5 Vdc) (V _{OH} = 4.6 Vdc) (V _{OH} = 9.5 Vdc) (V _{OH} = 13.5 Vdc)	Source I _{OH}	5.0	– 3.0	–	– 2.4	– 4.2	–	– 1.7	–	mAdc
		5.0	– 0.64	–	– 0.51	– 0.88	–	– 0.36	–	
		10	– 1.6	–	– 1.3	– 2.25	–	– 0.9	–	
		15	– 4.2	–	– 3.4	– 8.8	–	– 2.4	–	
	Sink I _{OL}	5.0	0.64	–	0.51	0.88	–	0.36	–	mAdc
		10	1.6	–	1.3	2.25	–	0.9	–	
		15	4.2	–	3.4	8.8	–	2.4	–	
Input Current	I _{in}	15	–	± 0.1	–	± 0.00001	± 0.1	–	± 1.0	μAdc
Input Capacitance (V _{in} = 0)	C _{in}	–	–	–	–	5.0	7.5	–	–	pF
Quiescent Current (Per Package)	I _{DD}	5.0	–	0.25	–	0.0005	0.25	–	7.5	μAdc
		10	–	0.5	–	0.0010	0.5	–	15	
		15	–	1.0	–	0.0015	1.0	–	30	
Total Supply Current (Notes 3, 4) (Dynamic plus Quiescent, Per Gate, C _L = 50 pF)	I _T	5.0 10 15	I _T = (0.3 μA/kHz) f + I _{DD} /N I _T = (0.6 μA/kHz) f + I _{DD} /N I _T = (0.9 μA/kHz) f + I _{DD} /N							μAdc

2. Data labelled “Typ” is not to be used for design purposes but is intended as an indication of the IC’s potential performance.
3. The formulas given are for the typical characteristics only at 25° C.
4. To calculate total supply current at loads other than 50 pF:

$$I_T(C_L) = I_T(50 \text{ pF}) + (C_L - 50) \text{ Vfk}$$

where: I_T is in μA (per package), C_L in pF, V = (V_{DD} – V_{SS}) in volts, f in kHz is input frequency, and k = 0.001 x the number of exercised gates per package.

MC14012B

SWITCHING CHARACTERISTICS (Note 5) ($C_L = 50 \text{ pF}$, $T_A = 25^\circ\text{C}$)

Characteristic	Symbol	V_{DD} Vdc	Min	Typ (Note 6)	Max	Unit
Output Rise Time $t_{TLH} = (1.35 \text{ ns/pF}) C_L + 33 \text{ ns}$ $t_{TLH} = (0.60 \text{ ns/pF}) C_L + 20 \text{ ns}$ $t_{TLH} = (0.40 \text{ ns/pF}) C_L + 20 \text{ ns}$	t_{TLH}	5.0 10 15	– – –	100 50 40	200 100 80	ns
Output Fall Time $t_{THL} = (1.35 \text{ ns/pF}) C_L + 33 \text{ ns}$ $t_{THL} = (0.60 \text{ ns/pF}) C_L + 20 \text{ ns}$ $t_{THL} = (0.40 \text{ ns/pF}) C_L + 20 \text{ ns}$	t_{THL}	5.0 10 15	– – –	100 50 40	200 100 80	ns
Propagation Delay Time $t_{PLH}, t_{PHL} = (0.90 \text{ ns/pF}) C_L + 115 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.36 \text{ ns/pF}) C_L + 47 \text{ ns}$ $t_{PLH}, t_{PHL} = (0.26 \text{ ns/pF}) C_L + 37 \text{ ns}$	t_{PLH}, t_{PHL}	5.0 10 15	– – –	160 65 50	300 130 100	ns

5. The formulas given are for the typical characteristics only at 25°C .

6. Data labelled "Typ" is not to be used for design purposes but is intended as an indication of the IC's potential performance.

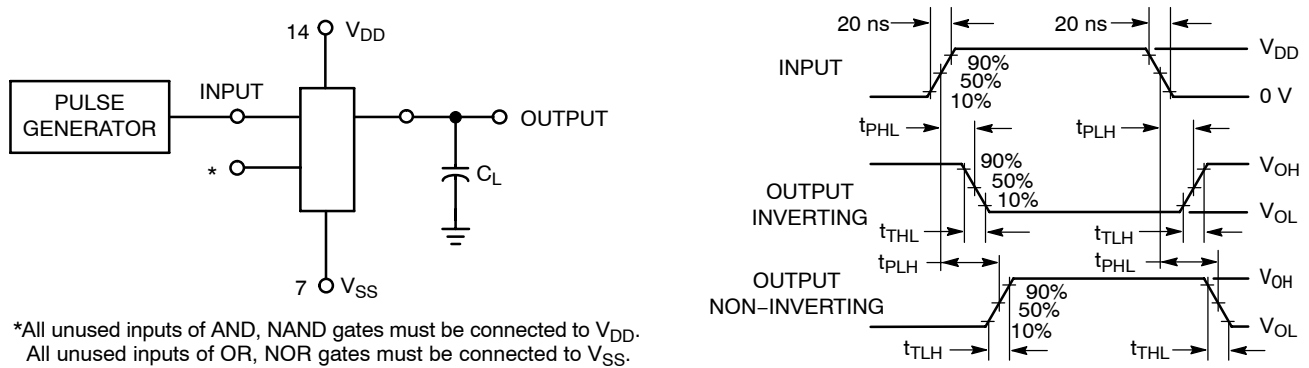


Figure 3. Switching Time Test Circuit and Waveforms

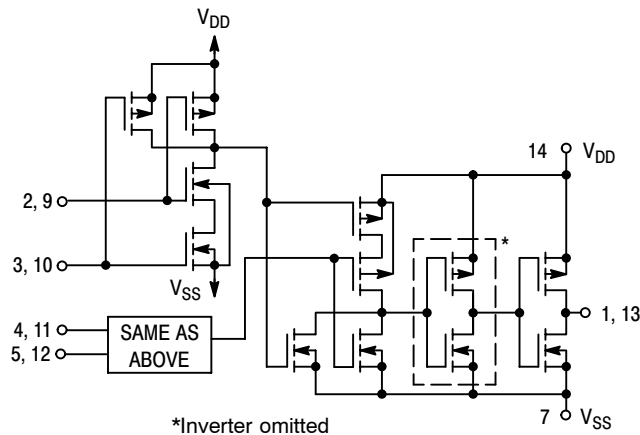
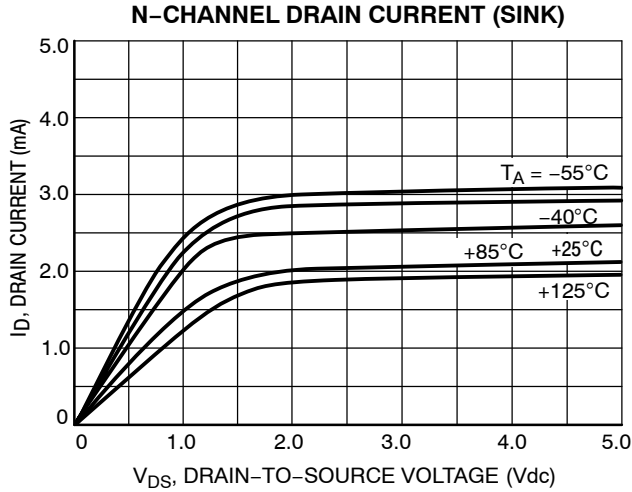
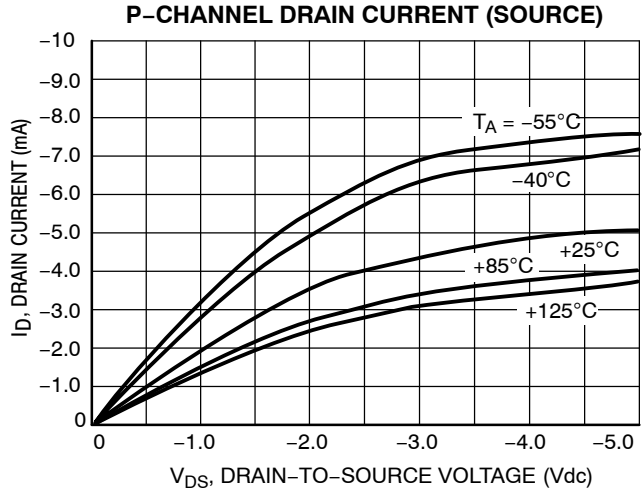
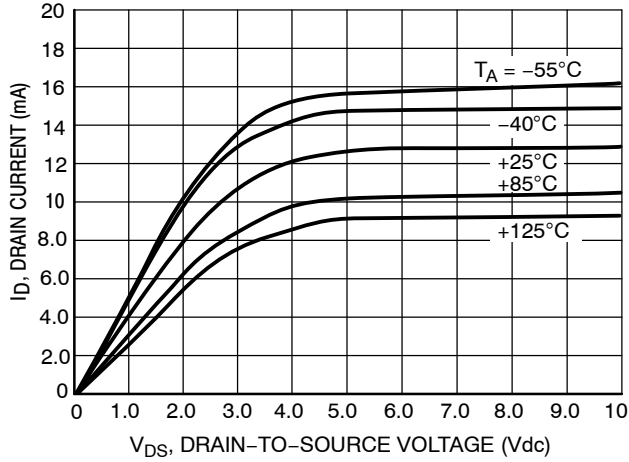
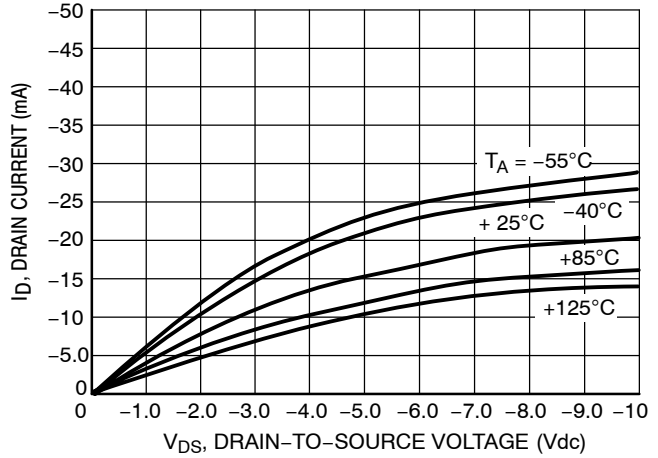
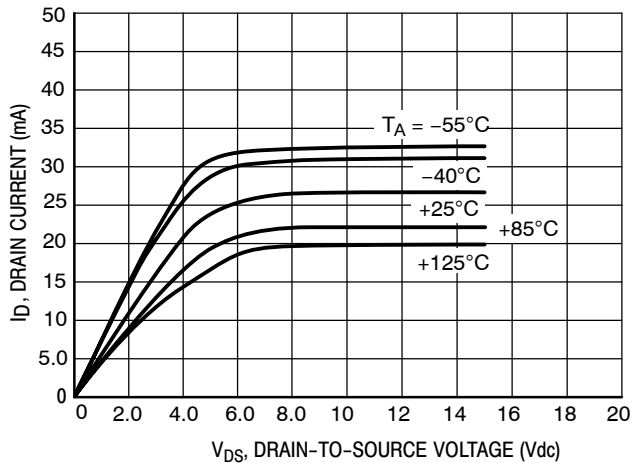
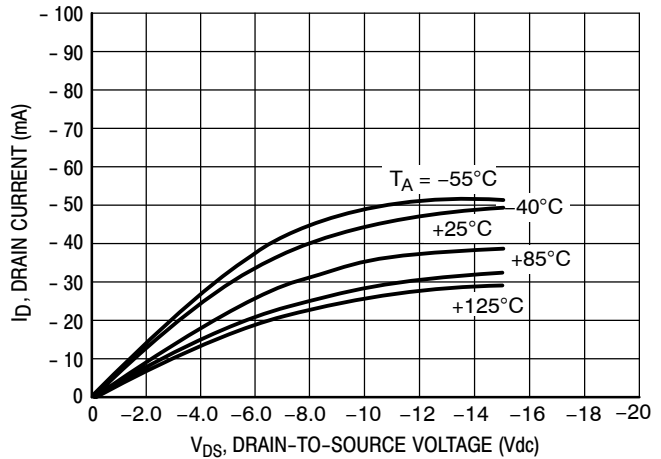


Figure 4. Circuit Schematic – One of Two Gates Shown

查询"MC14012BCP"供应商

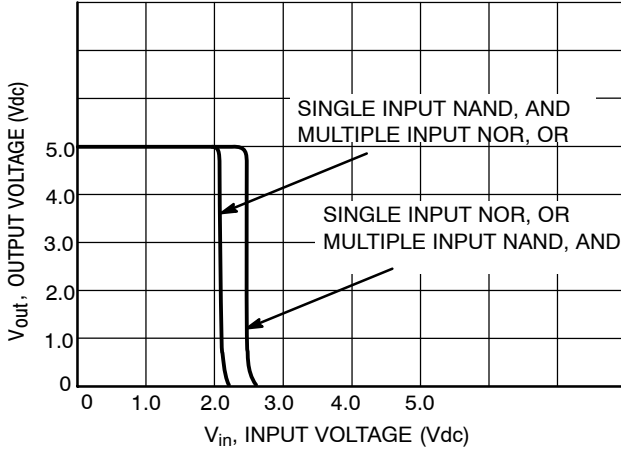
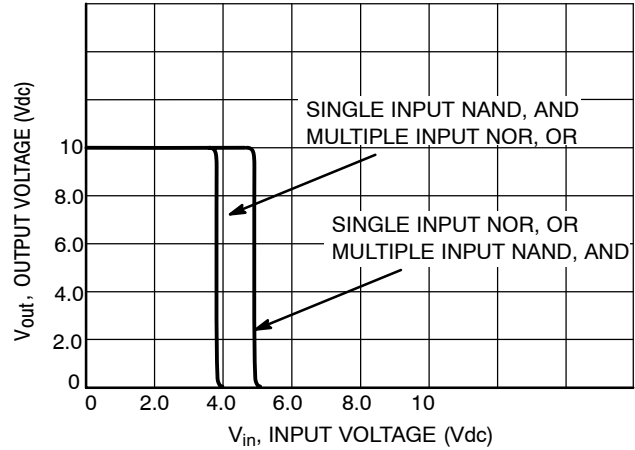
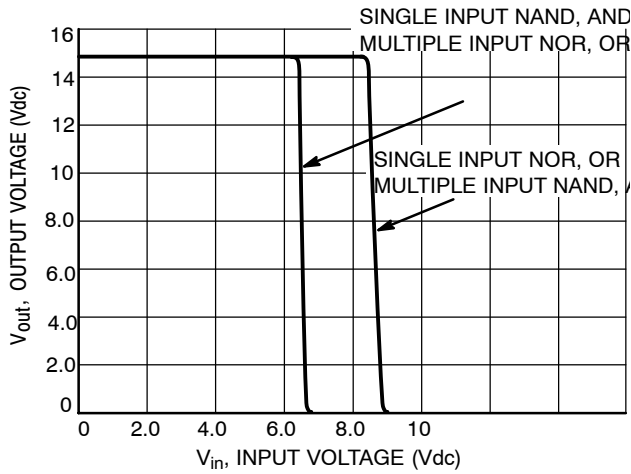
TYPICAL B-SERIES GATE CHARACTERISTICS

Figure 5. $V_{GS} = 5.0$ VdcFigure 6. $V_{GS} = -5.0$ VdcFigure 7. $V_{GS} = 10$ VdcFigure 8. $V_{GS} = -10$ VdcFigure 9. $V_{GS} = 15$ VdcFigure 10. $V_{GS} = -15$ Vdc

These typical curves are not guarantees, but are design aids.
 Caution: The maximum rating for output current is 10 mA per pin.

[查询"MC14012BCP"供应商](#)

VOLTAGE TRANSFER CHARACTERISTICS

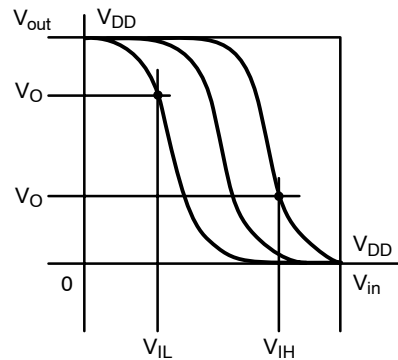
Figure 11. $V_{DD} = 5.0 \text{ Vdc}$ Figure 12. $V_{DD} = 10 \text{ Vdc}$ Figure 13. $V_{DD} = 15 \text{ Vdc}$

DC NOISE MARGIN

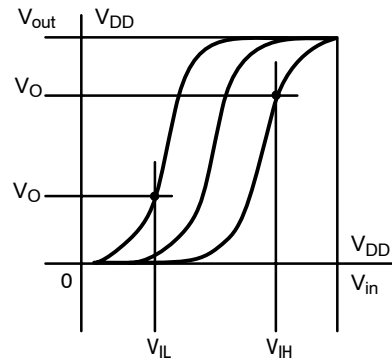
The DC noise margin is defined as the input voltage range from an ideal “1” or “0” input level which does not produce output state change(s). The typical and guaranteed limit values of the input values V_{IL} and V_{IH} for the output(s) to be at a fixed voltage V_O are given in the Electrical Characteristics table. V_{IL} and V_{IH} are presented graphically in Figure 11.

Guaranteed minimum noise margins for both the “1” and “0” levels =

- 1.0 V with a 5.0 V supply
- 2.0 V with a 10.0 V supply
- 2.5 V with a 15.0 V supply



(a) Inverting Function



(b) Non-Inverting Function

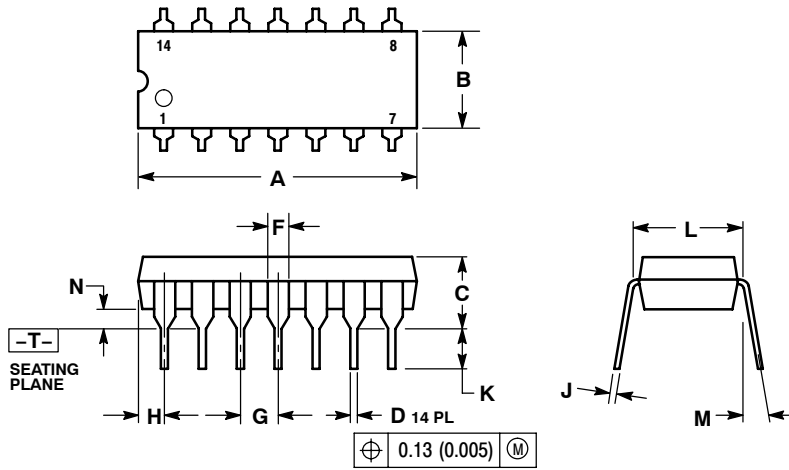
Figure 14. DC Noise Immunity

MC14012B

[查询"MC14012BCP"供应商](#)

PACKAGE DIMENSIONS

PDIP-14
CASE 646-06
ISSUE P



NOTES:

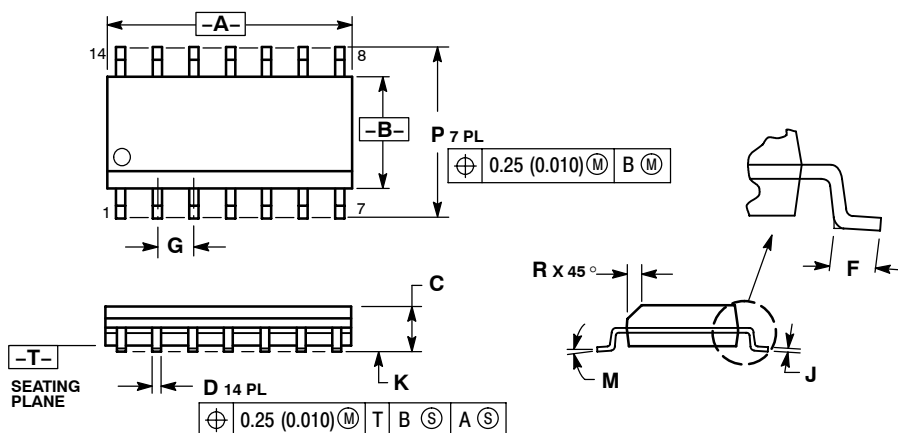
1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: INCH.
3. DIMENSION L TO CENTER OF LEADS WHEN FORMED PARALLEL.
4. DIMENSION B DOES NOT INCLUDE MOLD FLASH.
5. ROUNDED CORNERS OPTIONAL.

DIM	INCHES		MILLIMETERS	
	MIN	MAX	MIN	MAX
A	0.715	0.770	18.16	19.56
B	0.240	0.260	6.10	6.60
C	0.145	0.185	3.69	4.69
D	0.015	0.021	0.38	0.53
F	0.040	0.070	1.02	1.78
G	0.100 BSC		2.54 BSC	
H	0.052	0.095	1.32	2.41
J	0.008	0.015	0.20	0.38
K	0.115	0.135	2.92	3.43
L	0.290	0.310	7.37	7.87
M	---	10 °	---	10 °
N	0.015	0.039	0.38	1.01

查询"MC14012BCP"供应商

PACKAGE DIMENSIONS

SOIC-14
CASE 751A-03
ISSUE H

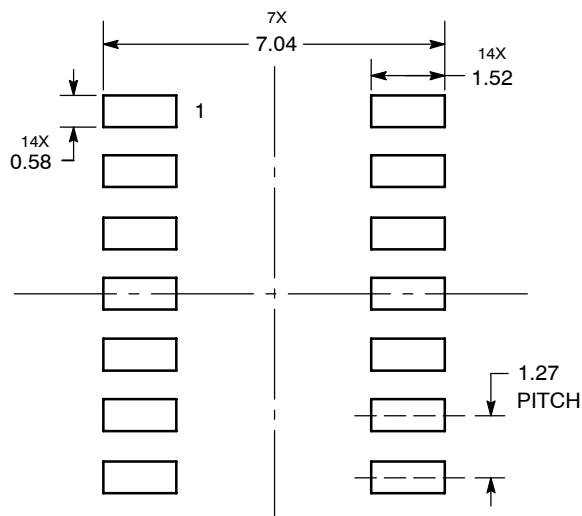


NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS A AND B DO NOT INCLUDE MOLD PROTRUSION.
4. MAXIMUM MOLD PROTRUSION 0.15 (0.006) PER SIDE.
5. DIMENSION D DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.127 (0.005) TOTAL IN EXCESS OF THE D DIMENSION AT MAXIMUM MATERIAL CONDITION.

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	8.55	8.75	0.337	0.344
B	3.80	4.00	0.150	0.157
C	1.35	1.75	0.054	0.068
D	0.35	0.49	0.014	0.019
F	0.40	1.25	0.016	0.049
G	1.27 BSC		0.050 BSC	
J	0.19	0.25	0.008	0.009
K	0.10	0.25	0.004	0.009
M	0 °	7 °	0 °	7 °
P	5.80	6.20	0.228	0.244
R	0.25	0.50	0.010	0.019

SOLDERING FOOTPRINT*



DIMENSIONS: MILLIMETERS

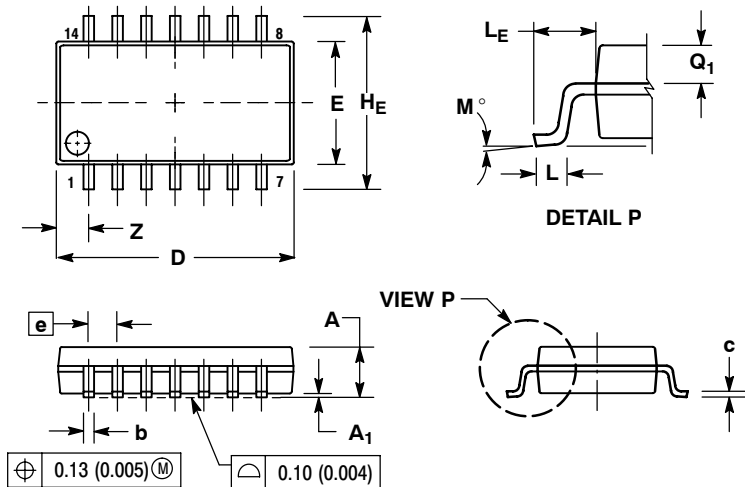
*For additional information on our Pb-Free strategy and soldering details, please download the ON Semiconductor Soldering and Mounting Techniques Reference Manual, SOLDERRM/D.

MC14012B

[查询"MC14012BCP"供应商](#)

PACKAGE DIMENSIONS

SOEIAJ-14
CASE 965-01
ISSUE A



NOTES:

1. DIMENSIONING AND TOLERANCING PER ANSI Y14.5M, 1982.
2. CONTROLLING DIMENSION: MILLIMETER.
3. DIMENSIONS D AND E DO NOT INCLUDE MOLD FLASH OR PROTRUSIONS AND ARE MEASURED AT THE PARTING LINE. MOLD FLASH OR PROTRUSIONS SHALL NOT EXCEED 0.15 (0.006) PER SIDE.
4. TERMINAL NUMBERS ARE SHOWN FOR REFERENCE ONLY.
5. THE LEAD WIDTH DIMENSION (b) DOES NOT INCLUDE DAMBAR PROTRUSION. ALLOWABLE DAMBAR PROTRUSION SHALL BE 0.08 (0.003) TOTAL IN EXCESS OF THE LEAD WIDTH DIMENSION AT MAXIMUM MATERIAL CONDITION. DAMBAR CANNOT BE LOCATED ON THE LOWER RADIUS OR THE FOOT. MINIMUM SPACE BETWEEN PROTRUSIONS AND ADJACENT LEAD TO BE 0.46 (0.018).

DIM	MILLIMETERS		INCHES	
	MIN	MAX	MIN	MAX
A	---	2.05	---	0.081
A ₁	0.05	0.20	0.002	0.008
b	0.35	0.50	0.014	0.020
c	0.10	0.20	0.004	0.008
D	9.90	10.50	0.390	0.413
E	5.10	5.45	0.201	0.215
e	1.27 BSC		0.050 BSC	
H _E	7.40	8.20	0.291	0.323
0.50	0.50	0.85	0.020	0.033
L _E	1.10	1.50	0.043	0.059
M	0°	10°	0°	10°
Q ₁	0.70	0.90	0.028	0.035
Z	---	1.42	---	0.056

ON Semiconductor and  are registered trademarks of Semiconductor Components Industries, LLC (SCILLC). SCILLC reserves the right to make changes without further notice to any products herein. SCILLC makes no warranty, representation or guarantee regarding the suitability of its products for any particular purpose, nor does SCILLC assume any liability arising out of the application or use of any product or circuit, and specifically disclaims any and all liability, including without limitation special, consequential or incidental damages. "Typical" parameters which may be provided in SCILLC data sheets and/or specifications can and do vary in different applications and actual performance may vary over time. All operating parameters, including "Typicals" must be validated for each customer application by customer's technical experts. SCILLC does not convey any license under its patent rights nor the rights of others. SCILLC products are not designed, intended, or authorized for use as components in systems intended for surgical implant into the body, or other applications intended to support or sustain life, or for any other application in which the failure of the SCILLC product could create a situation where personal injury or death may occur. Should Buyer purchase or use SCILLC products for any such unintended or unauthorized application, Buyer shall indemnify and hold SCILLC and its officers, employees, subsidiaries, affiliates, and distributors harmless against all claims, costs, damages, and expenses, and reasonable attorney fees arising out of, directly or indirectly, any claim of personal injury or death associated with such unintended or unauthorized use, even if such claim alleges that SCILLC was negligent regarding the design or manufacture of the part. SCILLC is an Equal Opportunity/Affirmative Action Employer. This literature is subject to all applicable copyright laws and is not for resale in any manner.

PUBLICATION ORDERING INFORMATION

LITERATURE FULFILLMENT:

Literature Distribution Center for ON Semiconductor
P.O. Box 5163, Denver, Colorado 80217 USA
Phone: 303-675-2175 or 800-344-3860 Toll Free USA/Canada
Fax: 303-675-2176 or 800-344-3867 Toll Free USA/Canada
Email: orderlit@onsemi.com

N. American Technical Support: 800-282-9855 Toll Free
USA/Canada

Europe, Middle East and Africa Technical Support:
Phone: 421 33 790 2910

Japan Customer Focus Center
Phone: 81-3-5773-3850

ON Semiconductor Website: www.onsemi.com

Order Literature: <http://www.onsemi.com/orderlit>

For additional information, please contact your local
Sales Representative

MC14012B/D