



## 28-BIT 1:2 REGISTERED BUFFER WITH PARITY

**IDT74SSTU32865**

### FEATURES:

- 1.8V Operation
- SSTL\_18 style clock and data inputs
- Differential CLK input
- Control inputs compatible with LVC MOS levels
- Flow-through architecture for optimum PCB design
- Latch-up performance exceeds 100mA
- ESD >2000V per MIL-STD-883, Method 3015; >200V using machine model (C = 200pF, R = 0)
- Available in 160-pin CTBGA package

### APPLICATIONS:

- Along with CSPU877/A/D DDR2 PLL, provides complete solution for DDR2 DIMMs
- Optimized for DDR2-400/533 (PC2-3200/4300) JEDEC Raw Card D

### DESCRIPTION:

The SSTU32865 is a 28-bit 1:2 configurable registered buffer designed for 1.7V to 1.9V V<sub>DD</sub> operation. All clock and data inputs are compatible with the JEDEC standard for SSTL\_18. The control inputs are LVC MOS. All outputs are 1.8V CMOS drivers that have been optimized to drive the DDR2 DIMM load.

The SSTU32865 operates from a differential clock (CLK and  $\overline{\text{CLK}}$ ). Data are registered at the crossing of CLK going high and  $\overline{\text{CLK}}$  going low.

This device supports low-power standby operation. When the reset input ( $\overline{\text{RESET}}$ ) is low, the differential input receivers are disabled, and undriven (floating) data, clock, and reference voltage (V<sub>REF</sub>) inputs are allowed. In addition, when  $\overline{\text{RESET}}$  is low all registers are reset, and all outputs are forced low. The LVC MOS  $\overline{\text{RESET}}$  and Cx inputs must always be held at a valid logic high or low level.

To ensure defined outputs from the register before a stable clock has been supplied,  $\overline{\text{RESET}}$  must be held in the low state during power up.

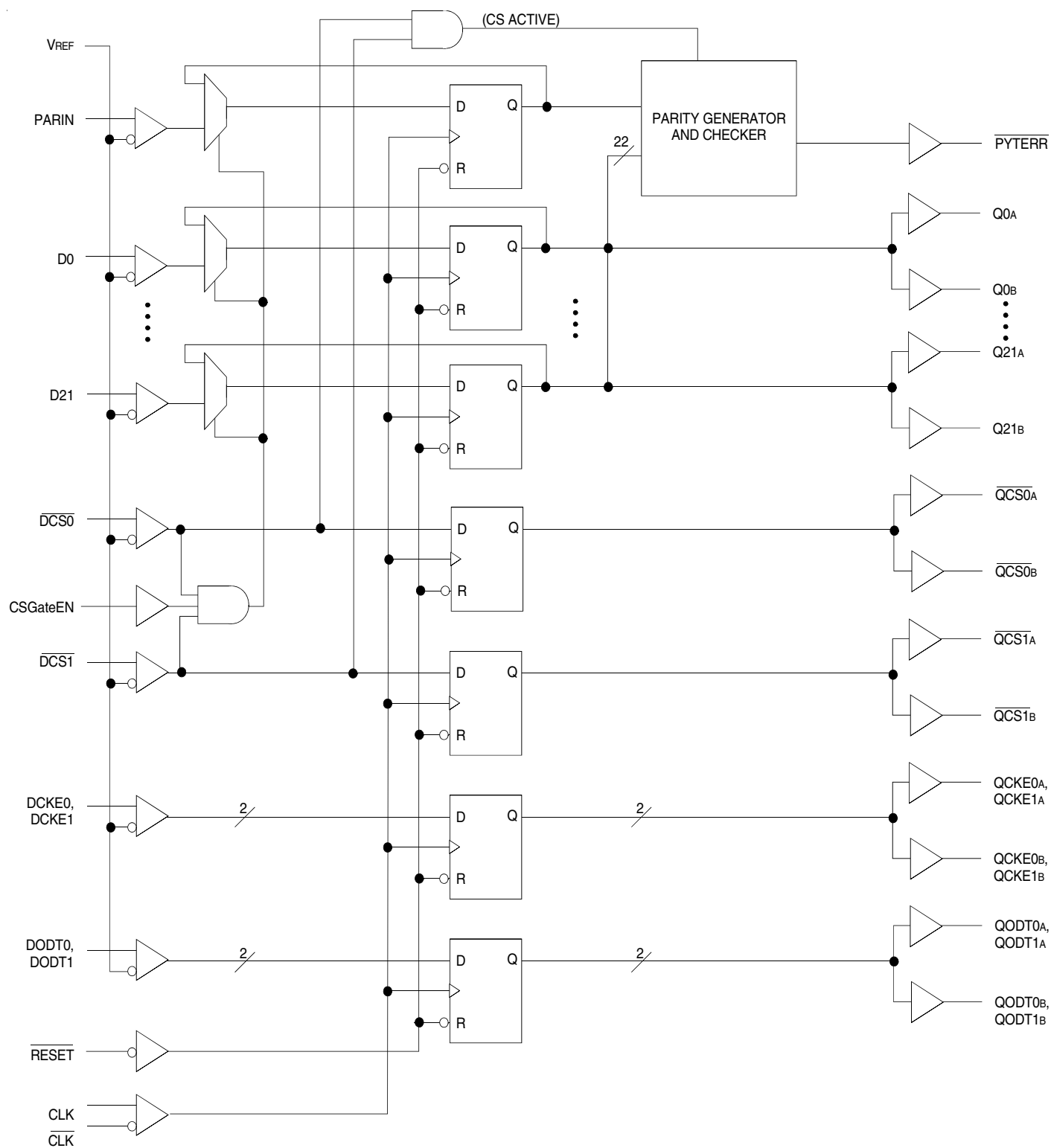
In the DDR2 DIMM application,  $\overline{\text{RESET}}$  is specified to be completely asynchronous with respect to CLK and  $\overline{\text{CLK}}$ . Therefore, no timing relationship can be guaranteed between the two. When entering reset, the register will be cleared and the outputs will be driven low quickly, relative to the time to disable the differential input receivers. However, when coming out of a reset, the register will become active quickly, relative to the time to enable the differential input receivers. As long as the data inputs are low, and the clock is stable during the time from the low-to-high transition of  $\overline{\text{RESET}}$  until the input receivers are fully enabled, the design of the SSTU32865 must ensure that the outputs will remain low, thus ensuring no glitches on the outputs.

The device monitors both  $\overline{\text{DCS0}}$  and  $\overline{\text{DCS1}}$  inputs and will gate the Qn outputs from changing states when both  $\overline{\text{DCS0}}$  and  $\overline{\text{DCS1}}$  are high. If either  $\overline{\text{DCS0}}$  and  $\overline{\text{DCS1}}$  input is low, the Qn outputs will function normally. The  $\overline{\text{RESET}}$  input has priority over the  $\overline{\text{DCS0}}$  and  $\overline{\text{DCS1}}$  control and will force the Qn outputs low and the  $\overline{\text{PYTERR}}$  output high. If the DCS-control functionality is not desired, then the CSGateEnable input can be hard-wired to ground, in which case the set-up time requirement for DCS would be the same as for the other D data inputs.

The SSTU32865 includes a parity checking function. The SSTU32865 accepts a parity bit from the memory controller at its input pin PARIN, compares it with the data received on the D-inputs, and indicates whether a parity error has occurred on its open-drain  $\overline{\text{PYTERR}}$  pin (active low).

[查询“IDT74SSTU32865BKG”供应商](#)

## FUNCTIONAL BLOCK DIAGRAM (1:2)



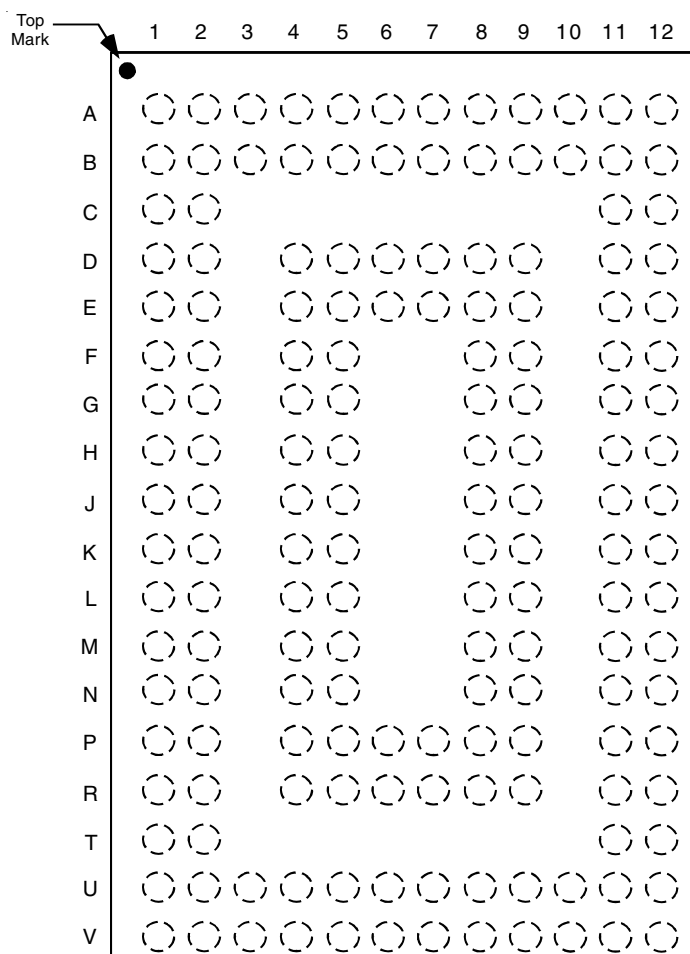
# PIN CONFIGURATION

|   | 1                         | 2                        | 3     | 4                          | 5    | 6      | 7      | 8    | 9    | 10   | 11                        | 12                        |
|---|---------------------------|--------------------------|-------|----------------------------|------|--------|--------|------|------|------|---------------------------|---------------------------|
| A | VREF                      | NC                       | PARIN | NC                         | NC   | QCKE1A | QCKE0A | Q21A | Q19A | Q18A | Q17B                      | Q17A                      |
| B | D1                        | D2                       | NC    | NC                         | NC   | QCKE1B | QCKE0B | Q21B | Q19B | Q18B | QODT0B                    | QODT0A                    |
| C | D3                        | D4                       |       |                            |      |        |        |      |      |      | QODT1B                    | QODT1A                    |
| D | D6                        | D5                       |       | VDDL                       | GND  | NC     | NC     | GND  | GND  |      | Q20B                      | Q20A                      |
| E | D7                        | D8                       |       | VDDL                       | GND  | VDDL   | VDDR   | GND  | GND  |      | Q16B                      | Q16A                      |
| F | D11                       | D9                       |       | VDDL                       | GND  |        |        | VDDR | VDDR |      | Q1B                       | Q1A                       |
| G | D18                       | D12                      |       | VDDL                       | GND  |        |        | VDDR | VDDR |      | Q2B                       | Q2A                       |
| H | CSGate<br>EN              | D15                      |       | VDDL                       | GND  |        |        | GND  | GND  |      | Q5B                       | Q5A                       |
| J | CLK                       | $\overline{\text{DCS0}}$ |       | GND                        | GND  |        |        | VDDR | VDDR |      | $\overline{\text{QCS0B}}$ | $\overline{\text{QCS0A}}$ |
| K | $\overline{\text{CLK}}$   | $\overline{\text{DCS1}}$ |       | VDDL                       | VDDL |        |        | GND  | GND  |      | $\overline{\text{QCS1B}}$ | $\overline{\text{QCS1A}}$ |
| L | $\overline{\text{RESET}}$ | D14                      |       | GND                        | GND  |        |        | VDDR | VDDR |      | Q6B                       | Q6A                       |
| M | D0                        | D10                      |       | GND                        | GND  |        |        | GND  | GND  |      | Q10B                      | Q10A                      |
| N | D17                       | D16                      |       | VDDL                       | VDDL |        |        | VDDR | VDDR |      | Q9B                       | Q9A                       |
| P | D19                       | D21                      |       | GND                        | VDDL | VDDL   | VDDR   | VDDR | GND  |      | Q11B                      | Q11A                      |
| R | D13                       | D20                      |       | GND                        | VDDL | VDDL   | GND    | GND  | GND  |      | Q15B                      | Q15A                      |
| T | DODT1                     | DODT0                    |       |                            |      |        |        |      |      |      | Q14B                      | Q14A                      |
| U | DCKE0                     | DCKE1                    | MCL   | $\overline{\text{PYTERR}}$ | MCH  | Q3B    | Q12B   | Q7B  | Q4B  | Q13B | Q0B                       | Q8B                       |
| V | VREF                      | MCL                      | MCL   | NC                         | MCH  | Q3A    | Q12A   | Q7A  | Q4A  | Q13A | Q0A                       | Q8A                       |

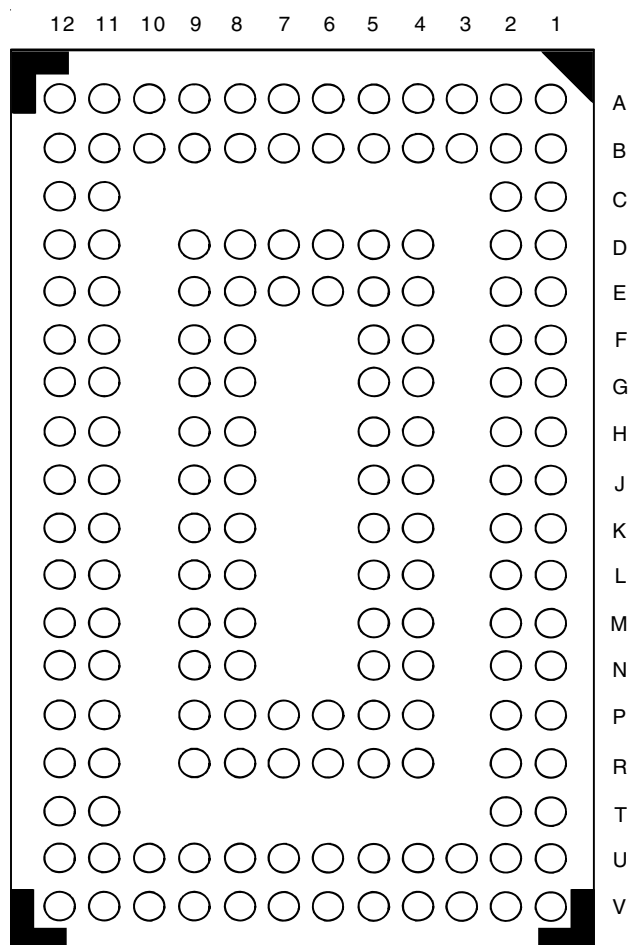
MCL denotes a pin that Must be Connected LOW. MCH denotes a pin that Must be Connected HIGH.

160-BALL CTBGA  
TOP VIEW

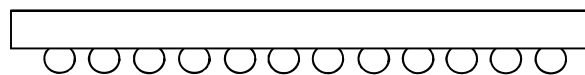
# 160 BALL CTBGA PACKAGE ATTRIBUTES



TOP VIEW



BOTTOM VIEW



SIDE VIEW

[查询"IDT74SSTU32865BKG"供应商](#)

## FUNCTION TABLE (EACH FLIP-FLOP) (1)

| Inputs |               |               |                  |               |               |                     | Outputs     |             |             |
|--------|---------------|---------------|------------------|---------------|---------------|---------------------|-------------|-------------|-------------|
| RESET  | DCS0          | DCS1          | CSGate<br>Enable | CLK           | CLK           | Dn, DODTn,<br>DCKEn | Qn          | QCS         | QODT, QCKE  |
| H      | L             | L             | X                | ↑             | ↓             | L                   | L           | L           | L           |
| H      | L             | L             | X                | ↑             | ↓             | H                   | H           | L           | H           |
| H      | L             | L             | X                | L or H        | L or H        | X                   | $Q_0^{(2)}$ | $Q_0^{(2)}$ | $Q_0^{(2)}$ |
| H      | L             | H             | X                | ↑             | ↓             | L                   | L           | L           | L           |
| H      | L             | H             | X                | ↑             | ↓             | H                   | H           | L           | H           |
| H      | L             | H             | X                | L or H        | L or H        | X                   | $Q_0^{(2)}$ | $Q_0^{(2)}$ | $Q_0^{(2)}$ |
| H      | H             | L             | X                | ↑             | ↓             | L                   | L           | H           | L           |
| H      | H             | L             | X                | ↑             | ↓             | H                   | H           | H           | H           |
| H      | H             | L             | X                | L or H        | L or H        | X                   | $Q_0^{(2)}$ | $Q_0^{(2)}$ | $Q_0^{(2)}$ |
| H      | H             | H             | L                | ↑             | ↓             | L                   | L           | H           | L           |
| H      | H             | H             | L                | ↑             | ↓             | H                   | H           | H           | H           |
| H      | H             | H             | L                | L or H        | L or H        | X                   | $Q_0^{(2)}$ | $Q_0^{(2)}$ | $Q_0^{(2)}$ |
| H      | H             | H             | H                | ↑             | ↓             | L                   | $Q_0^{(2)}$ | H           | L           |
| H      | H             | H             | H                | ↑             | ↓             | H                   | $Q_0^{(2)}$ | H           | H           |
| H      | H             | H             | H                | L or H        | L or H        | X                   | $Q_0^{(2)}$ | $Q_0^{(2)}$ | $Q_0^{(2)}$ |
| L      | X or Floating | X or Floating | X or Floating    | X or Floating | X or Floating | X or Floating       | L           | L           | L           |

## NOTES:

1. H = HIGH Voltage Level

L = LOW Voltage Level

X = Don't Care

↑ = LOW to HIGH

↓ = HIGH to LOW

2. Output level before the indicated steady-state conditions were established.

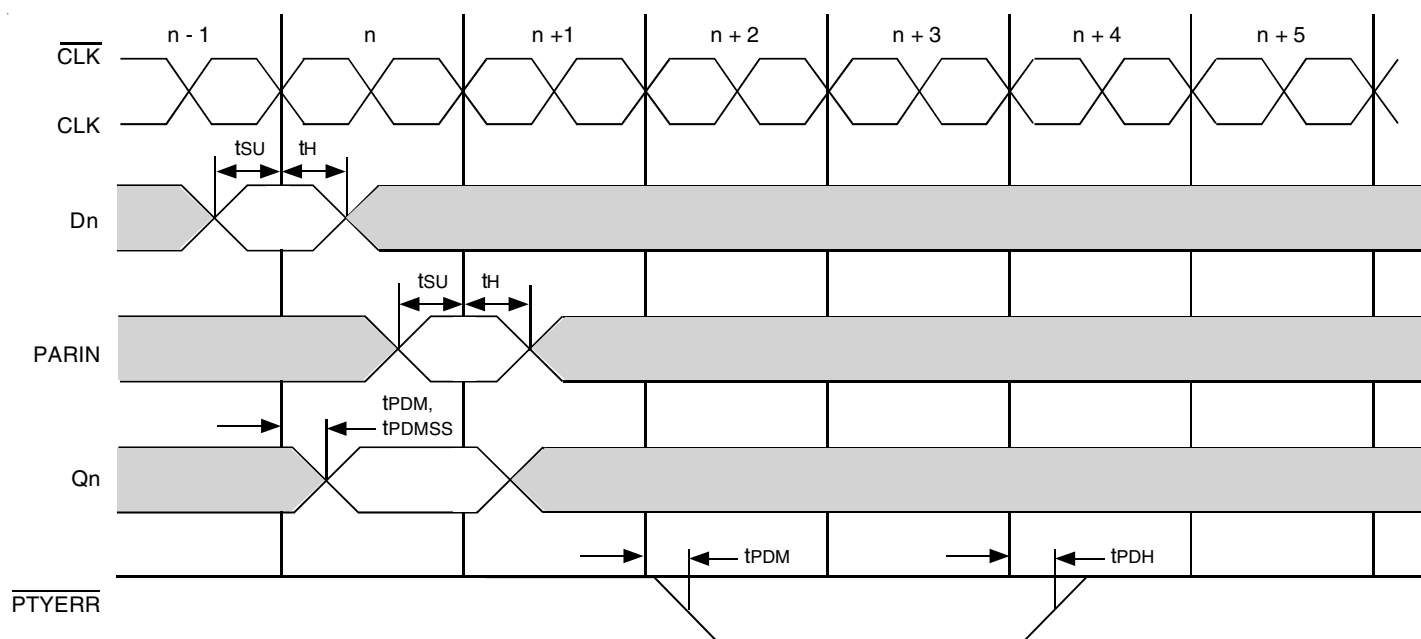
## PARITY AND STANDBY FUNCTION TABLE<sup>(1)</sup>

| Inputs |               |               |               |               |                                   |                      | Output                             |
|--------|---------------|---------------|---------------|---------------|-----------------------------------|----------------------|------------------------------------|
| RESET  | DCS0          | DCS1          | CLK           | CLK           | $\Sigma$ of Inputs = H (D0 - D21) | PARIN <sup>(2)</sup> | PYTERR <sup>(3)</sup>              |
| H      | L             | H             | ↑             | ↓             | Even                              | L                    | H                                  |
| H      | L             | H             | ↑             | ↓             | Odd                               | L                    | L                                  |
| H      | L             | H             | ↑             | ↓             | Even                              | H                    | L                                  |
| H      | L             | H             | ↑             | ↓             | Odd                               | H                    | H                                  |
| H      | H             | L             | ↑             | ↓             | Even                              | L                    | H                                  |
| H      | H             | L             | ↑             | ↓             | Odd                               | L                    | L                                  |
| H      | H             | L             | ↑             | ↓             | Even                              | H                    | L                                  |
| H      | H             | L             | ↑             | ↓             | Odd                               | H                    | H                                  |
| H      | H             | H             | ↑             | ↓             | X                                 | X                    | PYTERR <sub>0</sub> <sup>(4)</sup> |
| H      | X             | X             | L or H        | L or H        | X                                 | X                    | PYTERR <sub>0</sub> <sup>(4)</sup> |
| L      | X or Floating | X or Floating | X or Floating | X or Floating | X or Floating                     | X or Floating        | H                                  |

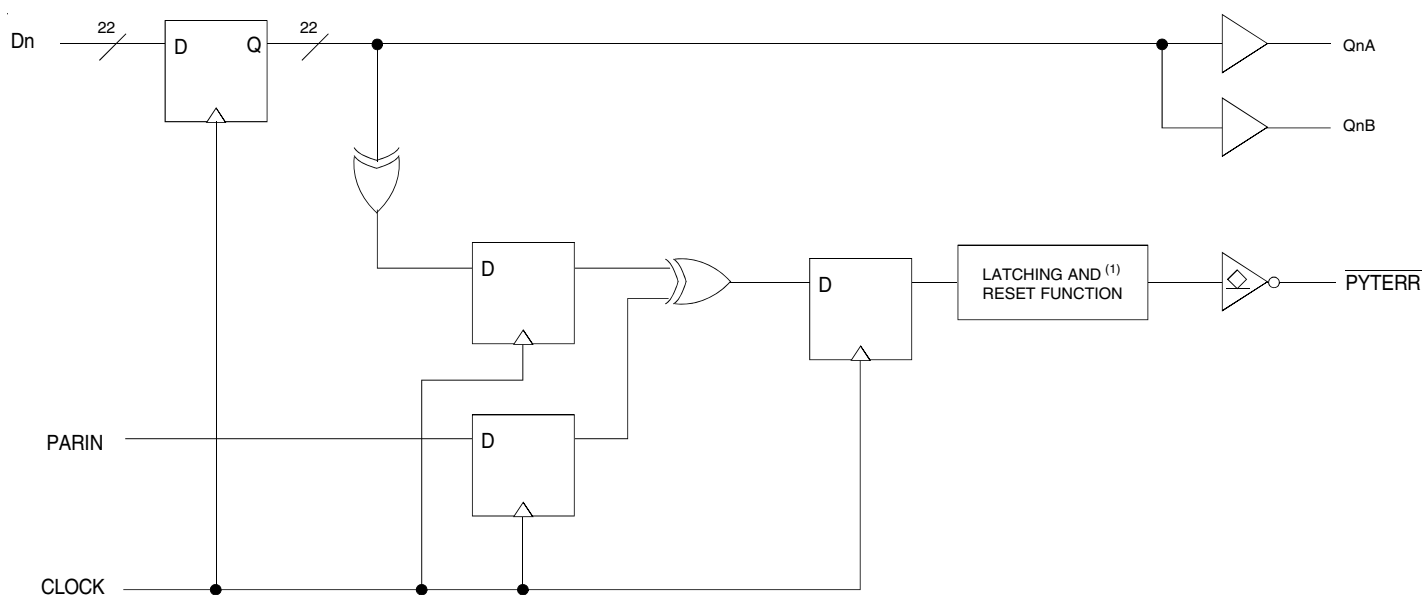
### NOTES:

- H = HIGH Voltage Level  
 L = LOW Voltage Level  
 X = Don't Care  
 ↑ = LOW to HIGH  
 ↓ = HIGH to LOW
- PARIN arrives one clock cycle after the data to which it applies
- This transition assumes PYTERR is HIGH at the crossing of CLK going HIGH and CLK going LOW. If PYTERR is LOW, it stays latched LOW for two clock cycles, or until RESET is driven LOW.
- Output level before the indicated steady-state conditions were established.

## REGISTER TIMING



## PARITY LOGIC DIAGRAM



### NOTE:

1. This function holds the error for two cycles. See REGISTER TIMING diagram.

## ABSOLUTE MAXIMUM RATINGS (1)

| Symbol               | Description                                                         | Max.                         | Unit |
|----------------------|---------------------------------------------------------------------|------------------------------|------|
| V <sub>DD</sub>      | Supply Voltage Range                                                | −0.5 to 2.5                  | V    |
| V <sub>I</sub> (2,3) | Input Voltage Range                                                 | −0.5 to 2.5                  | V    |
| V <sub>O</sub> (2,3) | Output Voltage Range                                                | −0.5 to V <sub>DD</sub> +0.5 | V    |
| I <sub>IK</sub>      | Input Clamp Current                                                 | ±50                          | mA   |
|                      | $V_I < 0$                                                           |                              |      |
|                      | $V_I > V_{DD}$                                                      |                              |      |
| I <sub>OK</sub>      | Output Clamp Current                                                | ±50                          | mA   |
|                      | $V_O < 0$                                                           |                              |      |
|                      | $V_O > V_{DD}$                                                      |                              |      |
| I <sub>O</sub>       | Continuous Output Current,<br>V <sub>O</sub> = 0 to V <sub>DD</sub> | ±50                          | mA   |
| V <sub>DD</sub>      | Continuous Current through each<br>V <sub>DD</sub> or GND           | ±100                         | mA   |
| T <sub>STG</sub>     | Storage Temperature Range                                           | −65 to +150                  | °C   |

### NOTES:

- Stresses greater than those listed under ABSOLUTE MAXIMUM RATINGS may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.
- The input and output negative voltage ratings may be exceeded if the ratings of the I/P and O/P clamp current are observed.
- This value is limited to 2.5V maximum.

## TIMING REQUIREMENTS OVER RECOMMENDED OPERATING FREE-AIR TEMPERATURE RANGE

| Symbol                   | Parameter                                                | V <sub>DD</sub> = 1.8V ± 0.1V                                                                               |      | Unit |
|--------------------------|----------------------------------------------------------|-------------------------------------------------------------------------------------------------------------|------|------|
|                          |                                                          | Min.                                                                                                        | Max. |      |
| f <sub>CLOCK</sub>       | Clock Frequency                                          | —                                                                                                           | 270  | MHz  |
| t <sub>w</sub>           | Pulse Duration, CLK, $\overline{\text{CLK}}$ HIGH or LOW | 1                                                                                                           | —    | ns   |
| t <sub>ACT</sub> (1,2)   | Differential Inputs Active Time                          | —                                                                                                           | 10   | ns   |
| t <sub>INACT</sub> (1,3) | Differential Inputs Inactive Time                        | —                                                                                                           | 15   | ns   |
| t <sub>SU</sub>          | Setup Time                                               | $\overline{\text{DCS}}\text{n}$ before CLK↑, $\overline{\text{CLK}}\downarrow$                              | 0.7  | ns   |
|                          |                                                          | Data, PARIN, DODT, and DCKE before CLK↑, $\overline{\text{CLK}}\downarrow$                                  | 0.5  |      |
| t <sub>H</sub>           | Hold Time                                                | Data, $\overline{\text{DCS}}\text{n}$ , PARIN, DCKE, and DODT after CLK↑, $\overline{\text{CLK}}\downarrow$ | 0.5  | ns   |

### NOTES:

- This parameter is not production tested.
- Data and V<sub>REF</sub> inputs must be low a minimum time of t<sub>ACT</sub> max, after  $\overline{\text{RESET}}$  is taken HIGH.
- Data, V<sub>REF</sub>, and clock inputs must be held at valid levels (not floating) a minimum time of t<sub>INACT</sub> max, after  $\overline{\text{RESET}}$  is taken LOW.

## TERMINAL FUNCTIONS

| Signal Group             | Terminal Name                                                                  | Type         | Description                                                                                                                                                                                                                                                                                                                                        |
|--------------------------|--------------------------------------------------------------------------------|--------------|----------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|
| Ungated Inputs           | DCKE0, DCKE1<br>DODT0, DODT1                                                   | SSTL_18      | DRAM function pins not associated with Chip Select                                                                                                                                                                                                                                                                                                 |
| Chip Select Gated Inputs | D0:D21                                                                         | SSTL_18      | DRAM inputs, re-driven only when Chip Select is LOW                                                                                                                                                                                                                                                                                                |
| Chip Select Inputs       | $\overline{DCS0}$ , $\overline{DCS1}$                                          | SSTL_18      | DRAM Chip Select signals. These pins initiate DRAM address/command decodes, and as such at least one will be LOW when a valid address/command is present. The register can be programmed to re-drive all D-inputs only (CSGateEN HIGH) when at least one Chip Select input is LOW.                                                                 |
| Re-Driven Outputs        | Q0A:Q21A<br>Q0B:Q21B<br>$\overline{QCS0}$ -1A, B<br>QCKE0-1A, B<br>QODT0-1A, B | SSTL_18      | Outputs of the register, valid after the specified clock count and immediately following a rising edge of the clock                                                                                                                                                                                                                                |
| Parity Input             | PARIN                                                                          | SSTL_18      | Input parity is received on pin PARIN, and should maintain odd parity across the D0:D21 inputs, at the rising edge of the clock                                                                                                                                                                                                                    |
| Parity Error Output      | $\overline{PTYERR}$                                                            | Open Drain   | When LOW, this output indicates that a parity error was identified associated with the address and/or command inputs. $\overline{PTYERR}$ will be active for two clock cycles, and delayed by an additional clock cycle for compatibility with final parity out timing on the industry-standard DDR-II register with parity (in JEDEC definition). |
| Program Inputs           | CSGateEN                                                                       | 1.8V LVCMOS  | Chip Select Gate Enable. When HIGH, the D0:D21 inputs will be latched only when at least one Chip Select input is LOW during the rising edge of the clock. When LOW, the D0:D21 inputs will be latched and redriven on every rising edge of the clock.                                                                                             |
| Clock Inputs             | CLK, $\overline{CLK}$                                                          | SSTL_18      | Differential master clock input pair to the register. The register operation is triggered by a rising edge on the positive clock input (CLK).                                                                                                                                                                                                      |
| Miscellaneous Inputs     | MCL, MCH                                                                       |              | Must be connected to a Logic LOW or HIGH.                                                                                                                                                                                                                                                                                                          |
|                          | $\overline{RESET}$                                                             | 1.8V LVCMOS  | Asynchronous Reset Input. When LOW, it causes a reset of the internal latches, thereby forcing the outputs LOW. $\overline{RESET}$ also resets the $\overline{PTYERR}$ signal.                                                                                                                                                                     |
|                          | VREF                                                                           | 0.9V nominal | Input reference voltage for SSTL_18 inputs. Two pins (internally tied together) are used for increased reliability.                                                                                                                                                                                                                                |

## OPERATING CHARACTERISTICS, $T_A = 25^{\circ}\text{C}$ (1,2)

| Symbol    | Parameter                      | Min.                           | Typ.                     | Max.                     | Unit               |
|-----------|--------------------------------|--------------------------------|--------------------------|--------------------------|--------------------|
| $V_{DD}$  | Supply Voltage                 | 1.7                            | —                        | 1.9                      | V                  |
| $V_{REF}$ | Reference Voltage              | $0.49 * V_{DD}$                | $0.5 * V_{DD}$           | $0.51 * V_{DD}$          | V                  |
| $V_{TT}$  | Termination Voltage            | $V_{REF} - 40\text{mV}$        | $V_{REF}$                | $V_{REF} + 40\text{mV}$  | V                  |
| $V_I$     | Input Voltage                  | 0                              | —                        | $V_{DD}$                 | V                  |
| $V_{IH}$  | AC High-Level Input Voltage    | Data Inputs                    | $V_{REF} + 250\text{mV}$ | —                        | V                  |
| $V_{IL}$  | AC Low-Level Input Voltage     | Data Inputs                    | —                        | $V_{REF} - 250\text{mV}$ | V                  |
| $V_{IH}$  | DC High-Level Input Voltage    | Data Inputs                    | $V_{REF} + 125\text{mV}$ | —                        | V                  |
| $V_{IL}$  | DC Low-Level Input Voltage     | Data Inputs                    | —                        | $V_{REF} - 125\text{mV}$ | V                  |
| $V_{IH}$  | High-Level Input Voltage       | $\overline{\text{RESET}}$ , Cx | $0.65 * V_{DD}$          | —                        | V                  |
| $V_{IL}$  | Low-Level Input Voltage        | $\overline{\text{RESET}}$ , Cx | —                        | $0.35 * V_{DD}$          | V                  |
| $V_{ICR}$ | Common Mode Input Voltage      | CLK, $\overline{\text{CLK}}$   | 0.675                    | 1.125                    | V                  |
| $V_{ID}$  | Differential Input Voltage     | CLK, $\overline{\text{CLK}}$   | 600                      | —                        | mV                 |
| $I_{OH}$  | High-Level Output Current      | —                              | —                        | -8                       | mA                 |
| $I_{OL}$  | Low-Level Output Current       | —                              | —                        | 8                        | mA                 |
| $T_A$     | Operating Free-Air Temperature | 0                              | —                        | 70                       | $^{\circ}\text{C}$ |

### NOTES:

1. The  $\overline{\text{RESET}}$  and Cx inputs of the device must be held at valid levels (not floating) to ensure proper device operation.
2. The differential inputs must not be floating unless  $\overline{\text{RESET}}$  is LOW.

## DC ELECTRICAL CHARACTERISTICS OVER OPERATING RANGE

Following Conditions Apply Unless Otherwise Specified:

Operating Condition:  $T_A = 0^{\circ}\text{C}$  to  $+70^{\circ}\text{C}$ ,  $V_{DD} = 1.8\text{V} \pm 0.1\text{V}$

| Symbol    | Parameter                                   | Test Conditions                                                                                                                                                                                                                                             | Min.     | Typ. | Max.    | Unit                                      |
|-----------|---------------------------------------------|-------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------------|----------|------|---------|-------------------------------------------|
| $V_{OH}$  |                                             | $V_{DD} = 1.7\text{V}$ to $1.9\text{V}$ , $I_{OH} = -6\text{mA}$                                                                                                                                                                                            | 1.2      | —    | —       | V                                         |
| $V_{OL}$  |                                             | $V_{DD} = 1.7\text{V}$ to $1.9\text{V}$ , $I_{OL} = 6\text{mA}$                                                                                                                                                                                             | —        | —    | 0.5     | V                                         |
| $I_I$     | All Inputs                                  | $V_I = V_{DD}$ or GND                                                                                                                                                                                                                                       | —        | —    | $\pm 5$ | $\mu\text{A}$                             |
| $I_{DD}$  | Static Standby                              | $I_O = 0$ , $V_{DD} = 1.9\text{V}$ , $\overline{\text{RESET}} = \text{GND}$                                                                                                                                                                                 | —        | —    | 200     | $\mu\text{A}$                             |
|           | Static Operating                            | $I_O = 0$ , $V_{DD} = 1.9\text{V}$ , $\overline{\text{RESET}} = V_{DD}$ , $V_I = V_{IH}(\text{AC})$ or $V_{IL}(\text{AC})$                                                                                                                                  | —        | —    | 40      | mA                                        |
| $I_{DDO}$ | Dynamic Operating (Clock Only)              | $I_O = 0$ , $V_{DD} = 1.8\text{V}$ , $\overline{\text{RESET}} = V_{DD}$ , $V_I = V_{IH}(\text{AC})$ or $V_{IL}(\text{AC})$ , CLK and $\overline{\text{CLK}}$ Switching 50% Duty Cycle.                                                                      | —        | —    | —       | $\mu\text{A}/\text{Clock MHz}$            |
|           | Dynamic Operating (Per Each Data Input)     | $I_O = 0$ , $V_{DD} = 1.8\text{V}$ , $\overline{\text{RESET}} = V_{DD}$ , $V_I = V_{IH}(\text{AC})$ or $V_{IL}(\text{AC})$ , CLK and $\overline{\text{CLK}}$ Switching at 50% Duty Cycle. One Data Input Switching at Half Clock Frequency, 50% Duty Cycle. | 1:1 Mode | —    | —       | $\mu\text{A}/\text{Clock MHz/Data Input}$ |
|           |                                             |                                                                                                                                                                                                                                                             | 1:2 Mode | —    | —       |                                           |
| $C_I$     | Dn                                          | $V_I = V_{REF} \pm 250\text{mV}$ , $V_{DD} = 1.8\text{V}$                                                                                                                                                                                                   | 2.5      | —    | 3.5     | pF                                        |
|           | $\overline{\text{DCSn}}$ and CS Gate Enable |                                                                                                                                                                                                                                                             | 4        | —    | 6       |                                           |
|           | CLK and $\overline{\text{CLK}}$             | $V_{ICR} = 0.9\text{V}$ , $V_{ID} = 600\text{mV}$ , $V_{DD} = 1.8\text{V}$                                                                                                                                                                                  | 4        | —    | 6       |                                           |
|           | $\overline{\text{RESET}}$                   | $V_I = V_{DD}$ or GND, $V_{DD} = 1.8\text{V}$                                                                                                                                                                                                               | 2        | —    | 6       |                                           |

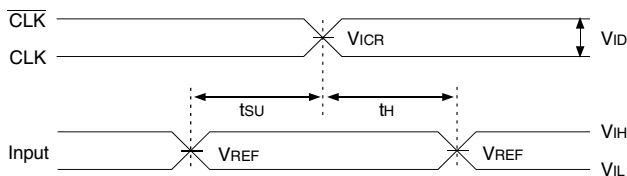
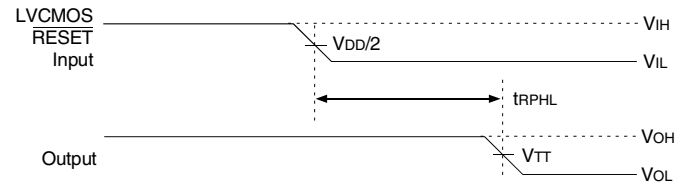
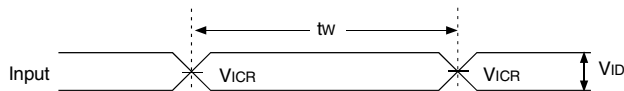
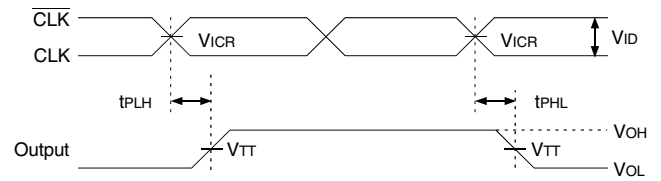
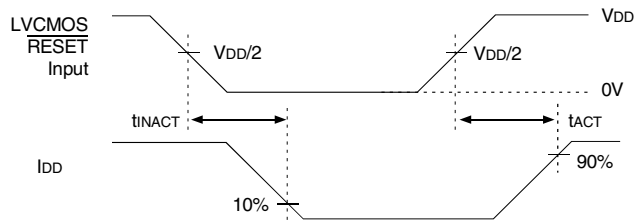
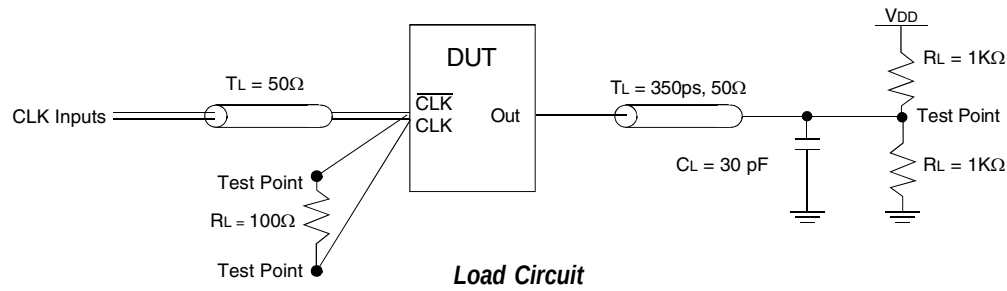
# SWITCHING CHARACTERISTICS OVER RECOMMENDED FREE-AIR OPERATING RANGE (UNLESS OTHERWISE NOTED) <sup>(1)</sup>

| Symbol                              | Parameter                                                                              | V <sub>DD</sub> = 1.8V ± 0.1V |      | Unit |
|-------------------------------------|----------------------------------------------------------------------------------------|-------------------------------|------|------|
|                                     |                                                                                        | Min                           | Max. |      |
| f <sub>MAX</sub>                    |                                                                                        | 270                           | —    | MHz  |
| t <sub>PDM</sub> <sup>(2)</sup>     | CLK and $\overline{\text{CLK}}$ to Q                                                   | 1.41                          | 2.15 | ns   |
| t <sub>LH</sub>                     | LOW to HIGH Delay, CLK and $\overline{\text{CLK}}$ to $\overline{\text{PYTERR}}$       | 1.2                           | 3    | ns   |
| t <sub>HL</sub>                     | HIGH to LOW Delay, CLK and $\overline{\text{CLK}}$ to $\overline{\text{PYTERR}}$       | 1                             | 3    | ns   |
| t <sub>PLH</sub>                    | LOW to HIGH Propagation Delay, $\overline{\text{RESET}}$ to $\overline{\text{PYTERR}}$ | —                             | 3    | ns   |
| t <sub>PDMSS</sub> <sup>(2,3)</sup> | CLK and $\overline{\text{CLK}}$ to Q (simultaneous switching)                          | —                             | 2.35 | ns   |
| t <sub>RPHL</sub>                   | $\overline{\text{RESET}}$ to Q                                                         | —                             | 3    | ns   |
| dV/dt <sub>r</sub>                  | Output slew rate from 20% to 80%                                                       | 1                             | 4    | V/ns |
| dV/dt <sub>f</sub>                  | Output slew rate from 20% to 80%                                                       | 1                             | 4    | V/ns |
| dV/dt <sub>Δ</sub> <sup>(4)</sup>   | Output slew rate from 20% to 80%                                                       | —                             | 1    | V/ns |

## NOTES:

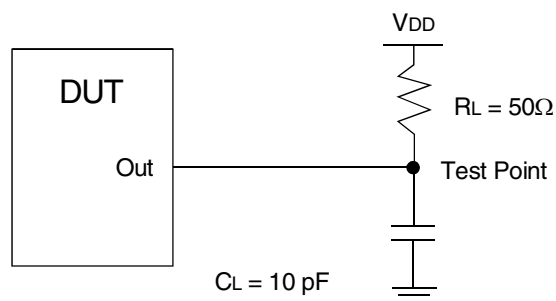
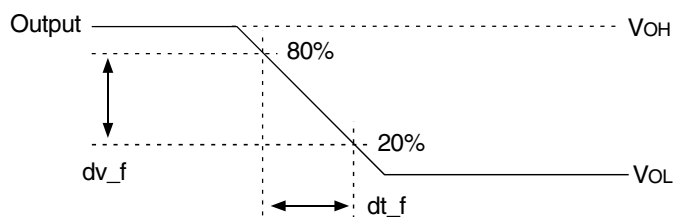
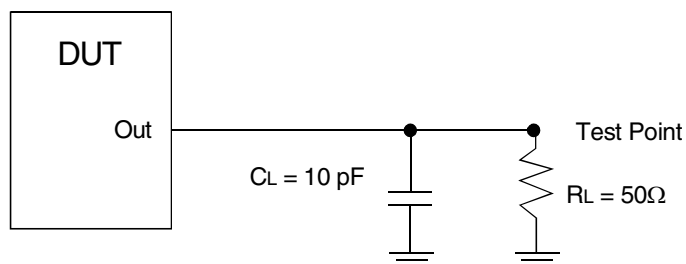
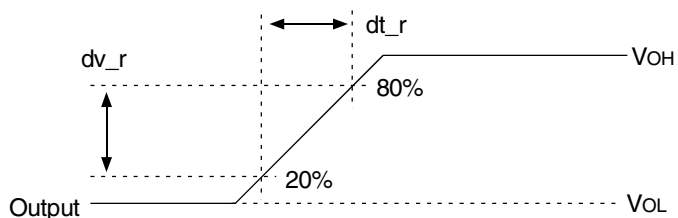
1. See TEST CIRCUITS AND WAVEFORMS.
2. Includes 350ps of test load transmission line delay.
3. This parameter is not production tested.
4. Difference between dV/dt<sub>r</sub> (rising edge rate) and dV/dt<sub>f</sub> (falling edge rate).

## TEST CIRCUITS AND WAVEFORMS ( $V_{DD} = 1.8V \pm 0.1V$ )



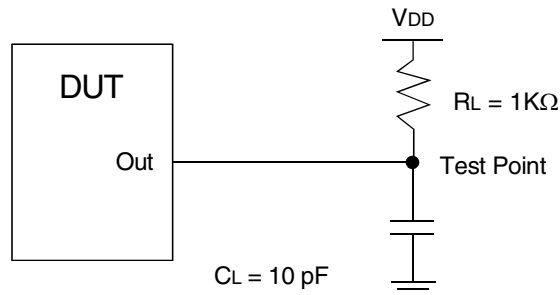
### NOTES:

1.  $C_L$  includes probe and jig capacitance.
2.  $I_{DD}$  tested with clock and data inputs held at  $V_{DD}$  or GND, and  $I_O = 0mA$
3. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10MHz$ ,  $Z_o = 50\Omega$ , input slew rate =  $1 V/ns \pm 20\%$  (unless otherwise specified).
4. The outputs are measured one at a time with one transition per measurement.
5.  $V_{TT} = V_{REF} = V_{DD}/2$
6.  $V_{IH} = V_{REF} + 250mV$  (AC voltage levels) for differential inputs.  $V_{IH} = V_{DD}$  for LVC MOS input.
7.  $V_{IL} = V_{REF} - 250mV$  (AC voltage levels) for differential inputs.  $V_{IL} = GND$  for LVC MOS input.
8.  $V_{ID} = 600mV$ .
9.  $t_{PLH}$  and  $t_{PHL}$  are the same as  $t_{PDM}$ .

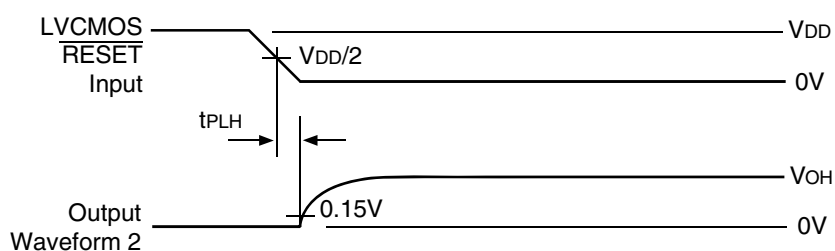
[查询"IDT74SSTU32865BKG"供应商](#)
TEST CIRCUITS AND WAVEFORMS ( $V_{DD} = 1.8V \pm 0.1V$ )**Load Circuit: High-to-Low Slew-Rate****Voltage Waveforms: High-to-Low Slew-Rate****Load Circuit: Low-to-High Slew-Rate****Voltage Waveforms: Low-to-High Slew-Rate****NOTES:**

1.  $C_L$  includes probe and jig capacitance.
2. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10\text{ MHz}$ ,  $Z_o = 50\Omega$ , input slew rate =  $1\text{ V/ns} \pm 20\%$  (unless otherwise specified).

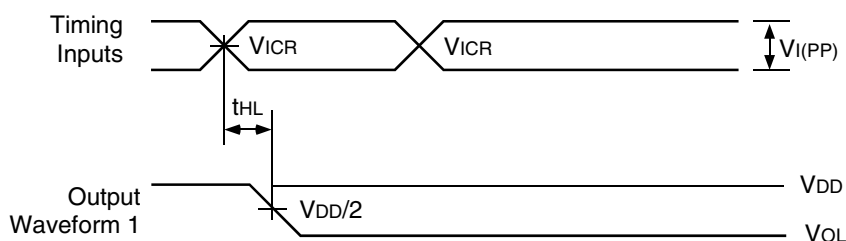
## TEST CIRCUITS AND WAVEFORMS ( $V_{DD} = 1.8V \pm 0.1V$ )



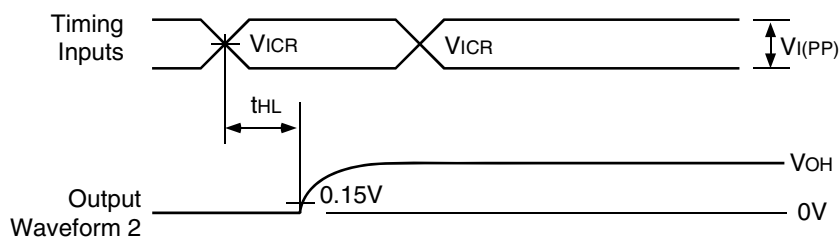
*Load Circuit: High-to-Low Slew-Rate*



*Voltage Waveforms: Open Drain Output Low-to-High Transition Time (with Respect to **RESET** Input)*



*Voltage Waveforms: Open Drain Output High-to-Low Transition Time (with Respect to Clock Inputs)*



*Voltage Waveforms: Open Drain Output Low-to-High Transition Time (with Respect to Clock Inputs)*

### NOTES:

1.  $C_L$  includes probe and jig capacitance.
2. All input pulses are supplied by generators having the following characteristics:  $PRR \leq 10\text{MHz}$ ,  $Z_o = 50\Omega$ , input slew rate =  $1\text{ V/ns} \pm 20\%$  (unless otherwise specified).

[查询"IDT74SSTU32865BKG"供应商](#)

## ORDERING INFORMATION

| IDT | XX          | SSTU32 | XXX         | XX      |                                                   |
|-----|-------------|--------|-------------|---------|---------------------------------------------------|
|     | Temp. Range |        | Device Type | Package |                                                   |
|     |             |        |             | BKG     | Thin Profile, Fine Pitch, Ball Grid Array - Green |
|     |             |        |             | 865     | 28-Bit 1:2 Registered Buffer with Parity          |
|     |             |        |             | 74      | 0°C to +70°C                                      |



**CORPORATE HEADQUARTERS**  
6024 Silver Creek Valley Road  
San Jose, CA 95138

**for SALES:**  
800-345-7015 or 408-284-8200  
fax: 408-284-2775  
[www.idt.com](http://www.idt.com)