

Octal D-type flip-flop with 5-volt tolerant inputs/outputs, positive edge-trigger (3-State)

74LVC374A

FEATURES

- 5-volt tolerant inputs/outputs, for interfacing with 5-volt logic
- Supply voltage range of 2.7V to 3.6V
- Complies with JEDEC standard no. 8-1A
- CMOS low power consumption
- Direct interface with TTL levels
- High impedance when $V_{CC} = 0V$
- 8-bit positive edge-triggered register
- Independent register and 3-State buffer operation

DESCRIPTION

The 74LVC374A is a high-performance, low-power, low-voltage, Si-gate CMOS device, superior to most advanced CMOS compatible TTL families.

Inputs can be driven from either 3.3V or 5V devices. In 3-State operation, outputs can handle 5V. This feature allows the use of these devices as translators in a mixed 3.3V/5V environment.

The 74LVC374A is an octal D-type flip-flop featuring separate D-type inputs for each flip-flop and 3-State outputs for bus-oriented applications. A clock (CP) and an output enable (\overline{OE}) input are common to all flip-flops.

The eight flip-flops will store the state of their individual D-inputs that meet the setup and hold times requirements on the LOW-to-HIGH CP transition.

When \overline{OE} is LOW, the contents of the eight flip-flops is available at the outputs. When \overline{OE} is HIGH, the outputs go to the high impedance OFF-state. Operation of the \overline{OE} input does not affect the state of the flip-flops.

The '374' is functionally identical to the '574', but the '574' has a different pin arrangement.

QUICK REFERENCE DATA

GND = 0V; $T_{amb} = 25^{\circ}C$; $t_r = t_f \leq 2.5ns$

| SYMBOL | PARAMETER | CONDITIONS | TYPICAL | UNIT |
|-------------------|---|---------------------------------|---------|------|
| t_{PHL}/t_{PLH} | Propagation delay CP to Q_n | $C_L = 50pF$ $V_{CC} = 3.3V$ | 4.8 | ns |
| f_{max} | maximum clock frequency | | 150 | MHz |
| C_I | Input capacitance | | 5.0 | pF |
| C_{PD} | Power dissipation capacitance per flip-flop | Notes 1 and 2 | 20 | pF |

NOTE:

1. C_{PD} is used to determine the dynamic power dissipation (P_D in μW):
 $P_D = C_{PD} \times V_{CC}^2 \times f_i + \sum (C_L \times V_{CC}^2 \times f_o)$ where:
 f_i = input frequency in MHz; C_L = output load capacity in pF;
 f_o = output frequency in MHz; V_{CC} = supply voltage in V;
 $\sum (C_L \times V_{CC}^2 \times f_o)$ = sum of outputs.
2. The condition is $V_I = GND$ to V_{CC}

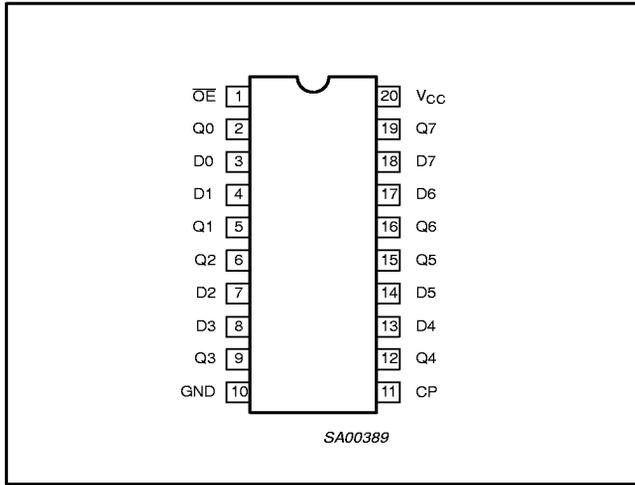
ORDERING INFORMATION

| PACKAGES | TEMPERATURE RANGE | OUTSIDE NORTH AMERICA | NORTH AMERICA | PKG. DWG. # |
|---|-------------------|-----------------------|---------------|-------------|
| 20-Pin Plastic Shrink Small Outline (SO) | -40°C to +85°C | 74LVC374A D | 74LVC374A D | SOT163-1 |
| 20-Pin Plastic Shrink Small Outline (SSOP) Type II | -40°C to +85°C | 74LVC374A DB | 74LVC374A DB | SOT339-1 |
| 20-Pin Plastic Thin Shrink Small Outline (TSSOP) Type I | -40°C to +85°C | 74LVC374A PW | 7LVC374APW DH | SOT360-1 |

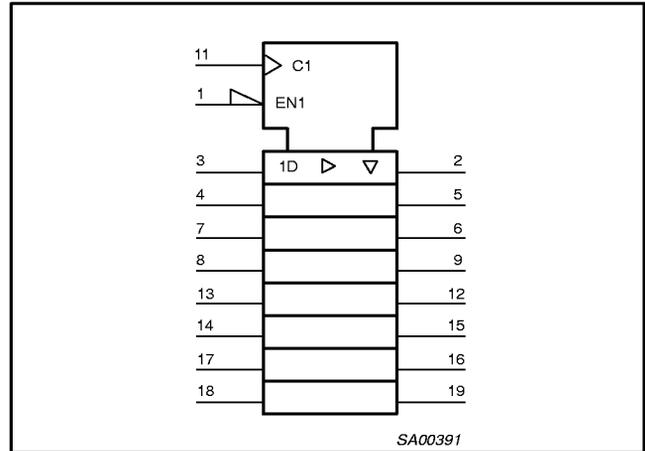
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PIN CONFIGURATION



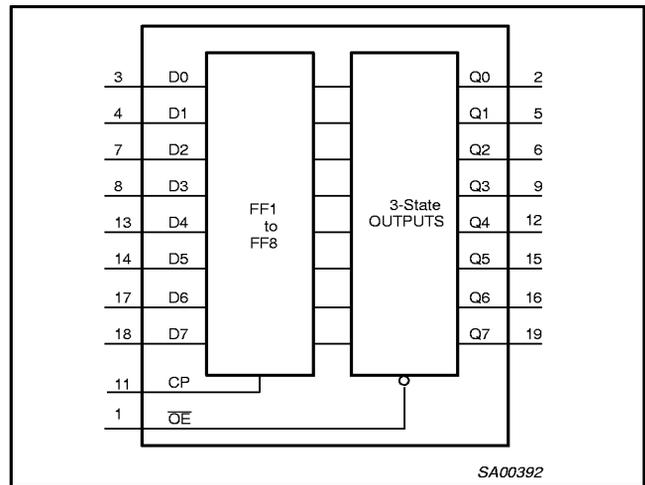
LOGIC SYMBOL (IEEE/IEC)



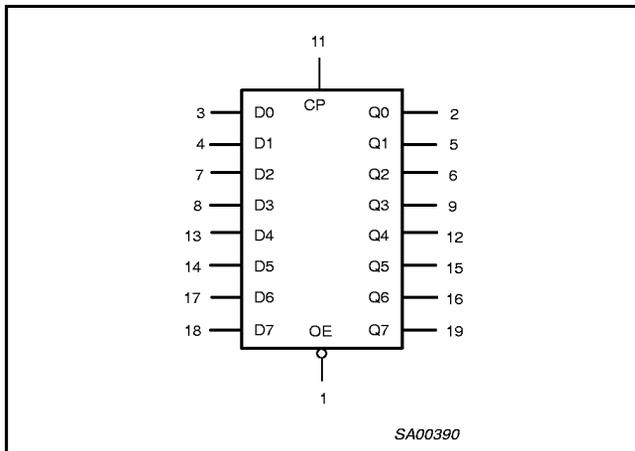
PIN DESCRIPTION

| PIN NUMBER | SYMBOL | FUNCTION |
|----------------------------|-----------------|---|
| 1 | \overline{OE} | Output enable input (active-Low) |
| 3, 4, 7, 8, 13, 14, 17, 18 | D0-D7 | Data inputs |
| 2, 5, 6, 9, 12, 15, 16, 19 | Q0-Q7 | 3-state flip-flop outputs |
| 11 | CP | Clock input (LOW-to-HIGH, edge-triggered) |
| 10 | GND | Ground (0V) |
| 20 | V _{CC} | Positive supply voltage |

FUNCTIONAL DIAGRAM



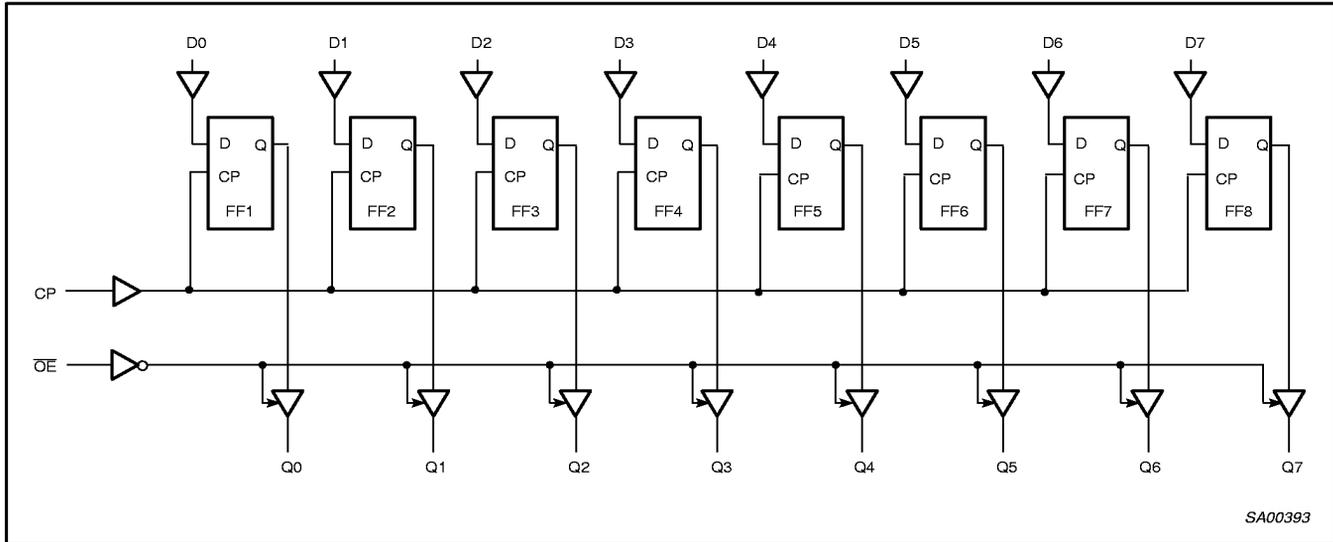
LOGIC SYMBOL



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LOGIC DIAGRAM



FUNCTION TABLE

| OPERATING MODES | INPUTS | | | INTERNAL FLIP-FLOPS | OUTPUTS |
|-----------------------------------|--------|----|----------------|---------------------|----------------------------------|
| | OE | LE | D _n | | Q ₀ to Q ₇ |
| Load and read register | L | ↑ | l | L | L |
| | L | ↑ | h | H | H |
| Load register and disable outputs | H | ↑ | l | L | Z |
| | H | ↑ | h | H | Z |

- H = HIGH voltage level
- h = HIGH voltage level one setup time prior to the LOW-to-HIGH CP transition
- L = LOW voltage level
- l = LOW voltage level one setup time prior to the LOW-to-HIGH CP transition
- Z = High impedance OFF-state
- ↑ = LOW-to-HIGH clock transition

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RECOMMENDED OPERATING CONDITIONS

| SYMBOL | PARAMETER | CONDITIONS | LIMITS | | UNIT |
|---------------------------------|---|-------------------------------|--------|-----------------|------|
| | | | MIN | MAX | |
| V _{CC} | DC supply voltage (for max. speed performance) | | 2.7 | 3.6 | V |
| | DC supply voltage (for low-voltage applications) | | 1.2 | 3.6 | |
| V _I | DC input voltage range | | 0 | 5.5 | V |
| V _O | DC output voltage range; output HIGH or LOW state | | 0 | V _{CC} | V |
| | DC output voltage range; output 3-State | | 0 | 5.5 | |
| T _{amb} | Operating ambient temperature range in free-air | | -40 | +85 | °C |
| t _r , t _f | Input rise and fall times | V _{CC} = 1.2 to 2.7V | 0 | 20 | ns/V |
| | | V _{CC} = 2.7 to 3.6V | 0 | 10 | |

ABSOLUTE MAXIMUM RATINGS¹

In accordance with the Absolute Maximum Rating System (IEC 134)

Voltages are referenced to GND (ground = 0V)

| SYMBOL | PARAMETER | CONDITIONS | RATING | UNIT |
|------------------------------------|--|--|------------------------------|------|
| V _{CC} | DC supply voltage | | -0.5 to +6.5 | V |
| I _{IK} | DC input diode current | V _I < 0 | -50 | mA |
| V _I | DC input voltage | Note 2 | -0.5 to +6.5 | V |
| I _{OK} | DC output diode current | V _O > V _{CC} or V _O < 0 | ± 50 | mA |
| V _O | DC output voltage; output HIGH or LOW state | Note 2 | -0.5 to V _{CC} +0.5 | V |
| | DC output voltage; output 3-State | Note 2 | -0.5 to 6.5 | |
| I _O | DC output source or sink current | V _O = 0 to V _{CC} | ± 50 | mA |
| I _{GND} , I _{CC} | DC V _{CC} or GND current | | ± 100 | mA |
| T _{stg} | Storage temperature range | | -65 to +150 | °C |
| P _{TOT} | Power dissipation per package - plastic mini-pack (SO) - plastic shrink mini-pack (SSOP and TSSOP) | above +70°C derate linearly with 8 mW/K | 500 | mW |
| | | above +60°C derate linearly with 5.5 mW/K | 500 | |

NOTES:

- Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
- The input and output voltage ratings may be exceeded if the input and output current ratings are observed.

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DC ELECTRICAL CHARACTERISTICS

Over recommended operating conditions voltages are referenced to GND (ground = 0V)

| SYMBOL | PARAMETER | TEST CONDITIONS | LIMITS | | | UNIT |
|------------------|---|--|-----------------------|------------------|------|------|
| | | | Temp = -40°C to +85°C | | | |
| | | | MIN | TYP ¹ | MAX | |
| V _{IH} | HIGH level Input voltage | V _{CC} = 1.2V | V _{CC} | | | V |
| | | V _{CC} = 2.7 to 3.6V | 2.0 | | | |
| V _{IL} | LOW level Input voltage | V _{CC} = 1.2V | | | GND | V |
| | | V _{CC} = 2.7 to 3.6V | | | 0.8 | |
| V _{OH} | HIGH level output voltage | V _{CC} = 2.7V; V _I = V _{IH} or V _{IL} ; I _O = -12mA | V _{CC} - 0.5 | | | V |
| | | V _{CC} = 3.0V; V _I = V _{IH} or V _{IL} ; I _O = -100µA | V _{CC} - 0.2 | V _{CC} | | |
| | | V _{CC} = 3.0V; V _I = V _{IH} or V _{IL} ; I _O = -18mA | V _{CC} - 0.6 | | | |
| | | V _{CC} = 3.0V; V _I = V _{IH} or V _{IL} ; I _O = -24mA | V _{CC} - 0.8 | | | |
| V _{OL} | LOW level output voltage | V _{CC} = 2.7V; V _I = V _{IH} or V _{IL} ; I _O = 12mA | | | 0.40 | V |
| | | V _{CC} = 3.0V; V _I = V _{IH} or V _{IL} ; I _O = 100µA | | GND | 0.20 | |
| | | V _{CC} = 3.0V; V _I = V _{IH} or V _{IL} ; I _O = 24mA | | | 0.55 | |
| I _I | Input leakage current ² | V _{CC} = 3.6V; V _I = 5.5V or GND | | ±0.1 | ±5 | µA |
| I _{OZ} | 3-State output OFF-state current | V _{CC} = 3.6V; V _I = V _{IH} or V _{IL} ; V _O = 5.5V or GND | | 0.1 | ±10 | µA |
| I _{off} | Power off leakage supply | V _{CC} = 0.0V; V _I or V _O = 5.5V | | 0.1 | ±10 | µA |
| I _{CC} | Quiescent supply current | V _{CC} = 3.6V; V _I = V _{CC} or GND; I _O = 0 | | 0.1 | 10 | µA |
| ΔI _{CC} | Additional quiescent supply current per input pin | V _{CC} = 2.7V to 3.6V; V _I = V _{CC} - 0.6V; I _O = 0 | | 5 | 500 | µA |

NOTES:

- All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.
- The specified overdrive current at the data input forces the data input to the opposite logic input state.

AC CHARACTERISTICS

GND = 0V; t_r = t_f ≤ 2.5ns; C_L = 50pF; R_L = 500Ω; T_{amb} = -40°C to +85°C.

| SYMBOL | PARAMETER | WAVEFORM | LIMITS | | | | | | UNIT |
|--------------------------------------|---|----------|------------------------------|------------------|-----|------------------------|-----|------------------------|------|
| | | | V _{CC} = 3.3V ±0.3V | | | V _{CC} = 2.7V | | V _{CC} = 1.2V | |
| | | | MIN | TYP ¹ | MAX | MIN | MAX | TYP | |
| t _{PHL} t _{PLH} | Propagation delay CP to Q _n | 1, 4 | 1.5 | 4.8 | 7.0 | 1.5 | 8.0 | 21 | ns |
| t _{PZH} t _{PZL} | 3-State output enable time OE to Q _n | 2, 4 | 1.5 | 4.8 | 7.5 | 1.5 | 8.5 | 22 | ns |
| t _{PHZ} t _{PLZ} | 3-State output disable time OE to Q _n | 2, 4 | 1.5 | 4.3 | 6.0 | 1.5 | 7.0 | 15 | ns |
| t _w | Clock pulse width HIGH or LOW | 1 | 3.0 | 1.5 | – | 3.0 | – | – | ns |
| t _{SU} | Setup time D _n to CP | 3 | 2.0 | 0 | – | 2.0 | – | – | ns |
| t _H | Hold time D _n to CP | 3 | 1.5 | 0.6 | – | 1.5 | – | – | ns |
| f _{max} | maximum clock pulse frequency | 1 | 100 | – | – | 80 | – | – | MHz |

NOTE:

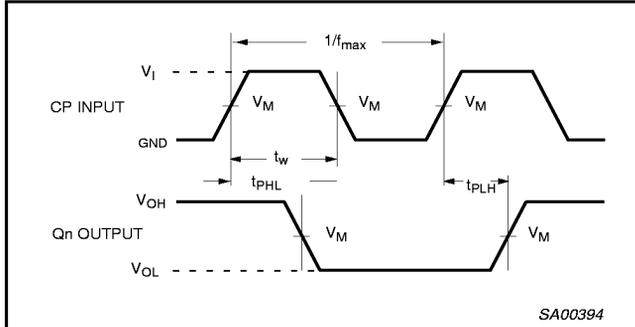
- Unless otherwise stated, all typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

Octal D-type flip-flop with 5-volt tolerant inputs/outputs, positive edge-trigger (3-State)

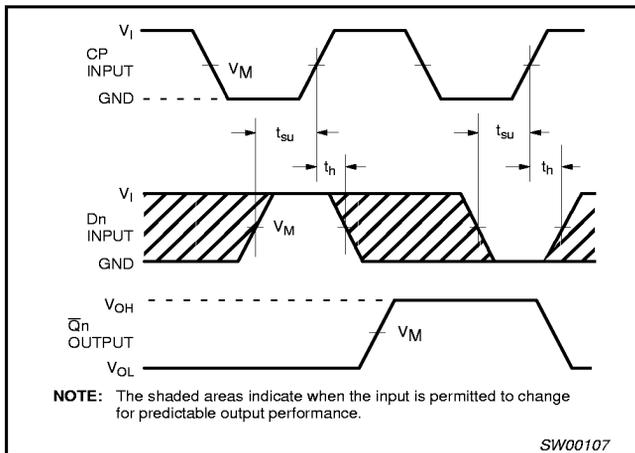
74LVC374A

AC WAVEFORMS

$V_M = 1.5V$ at $V_{CC} \geq 2.7V$; $V_M = 0.5 V_{CC}$ at $V_{CC} < 2.7V$.
 V_{OL} and V_{OH} are the typical output voltage drop that occur with the output load.
 $V_X = V_{OL} + 0.3V$ at $V_{CC} \geq 2.7V$; $V_X = V_{OL} + 0.1 V_{CC}$ at $V_{CC} < 2.7V$
 $V_Y = V_{OH} - 0.3V$ at $V_{CC} \geq 2.7V$; $V_Y = V_{OH} - 0.1 V_{CC}$ at $V_{CC} < 2.7V$

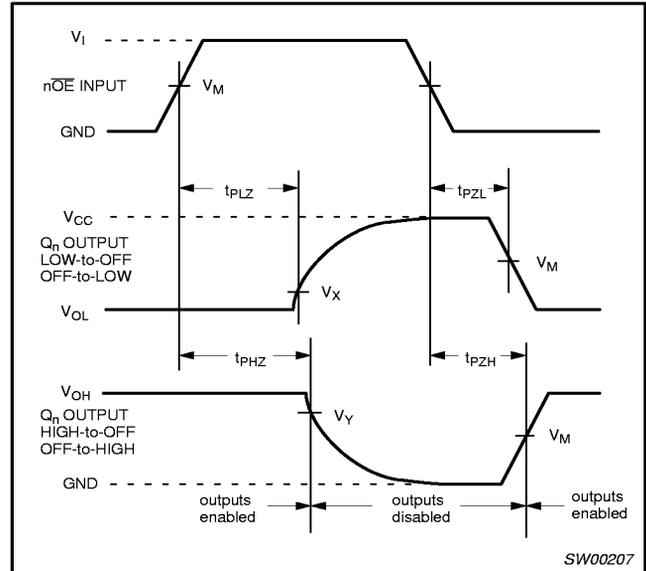


Waveform 1. Clock (CP) to output (Q_n) propagation delays, the clock pulse width, output transition times and the maximum clock pulse frequency.



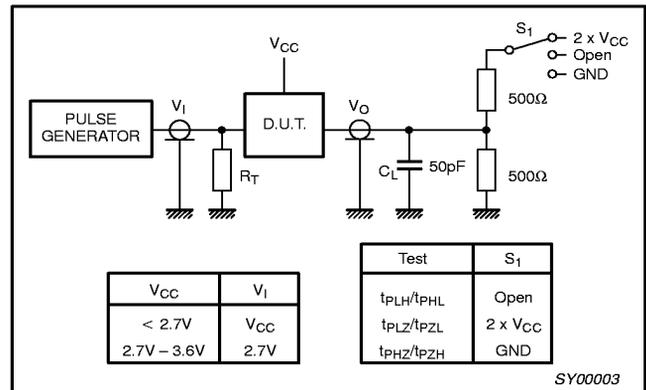
NOTE: The shaded areas indicate when the input is permitted to change for predictable output performance.

Waveform 2. Data setup and hold times for the D_n input to the CP input.



Waveform 3. 3-State enable and disable times.

TEST CIRCUIT



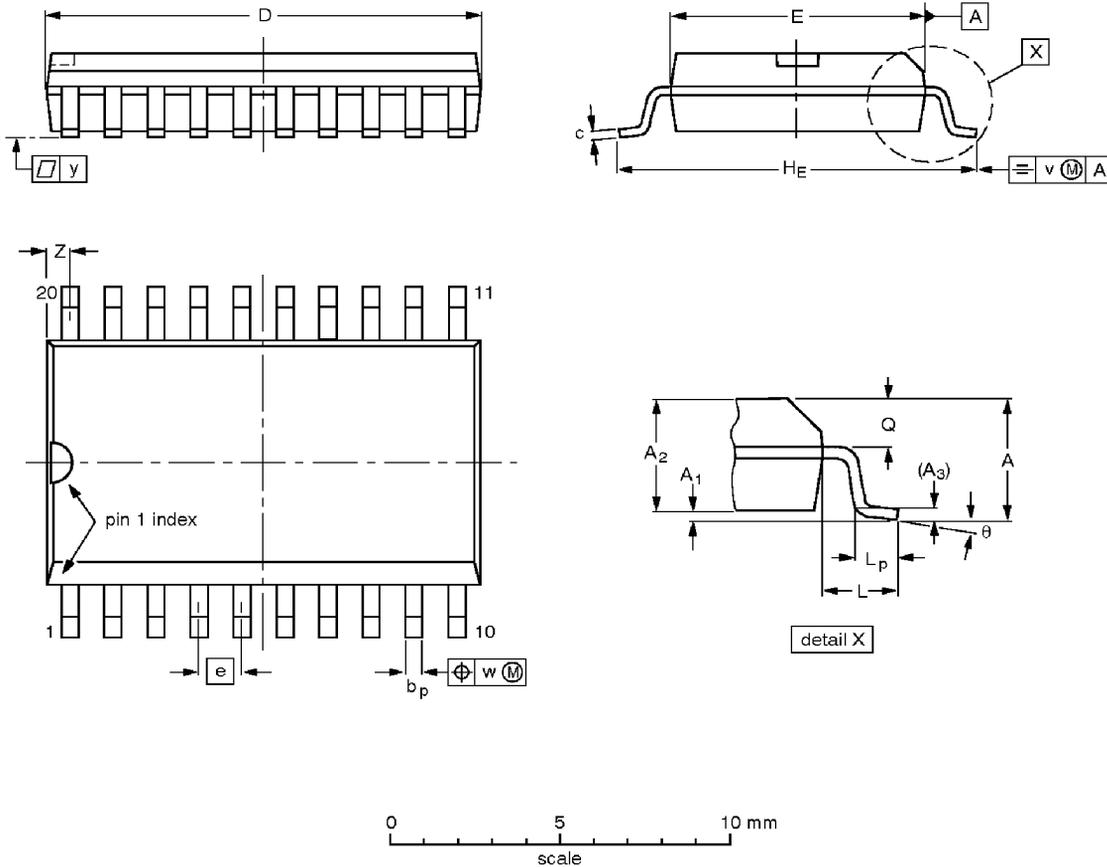
Waveform 4. Load circuitry for switching times.

Octal D-type flip-flop with 5-volt tolerant
 inputs/outputs, positive edge-trigger

74LVC374A

SO20: plastic small outline package; 20 leads; body width 7.5 mm

SOT163-1



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

| UNIT | A max. | A ₁ | A ₂ | A ₃ | b _p | c | D ⁽¹⁾ | E ⁽¹⁾ | e | H _E | L | L _p | Q | v | w | y | Z ⁽¹⁾ | θ |
|--------|--------|----------------|----------------|----------------|----------------|----------------|------------------|------------------|-------|----------------|-------|----------------|----------------|------|------|-------|------------------|----------|
| mm | 2.65 | 0.30 0.10 | 2.45 2.25 | 0.25 | 0.49 0.36 | 0.32 0.23 | 13.0 12.6 | 7.6 7.4 | 1.27 | 10.65 10.00 | 1.4 | 1.1 0.4 | 1.1 1.0 | 0.25 | 0.25 | 0.1 | 0.9 0.4 | 8° 0° |
| inches | 0.10 | 0.012 0.004 | 0.096 0.089 | 0.01 | 0.019 0.014 | 0.013 0.009 | 0.51 0.49 | 0.30 0.29 | 0.050 | 0.419 0.394 | 0.055 | 0.043 0.016 | 0.043 0.039 | 0.01 | 0.01 | 0.004 | 0.035 0.016 | |

Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

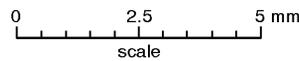
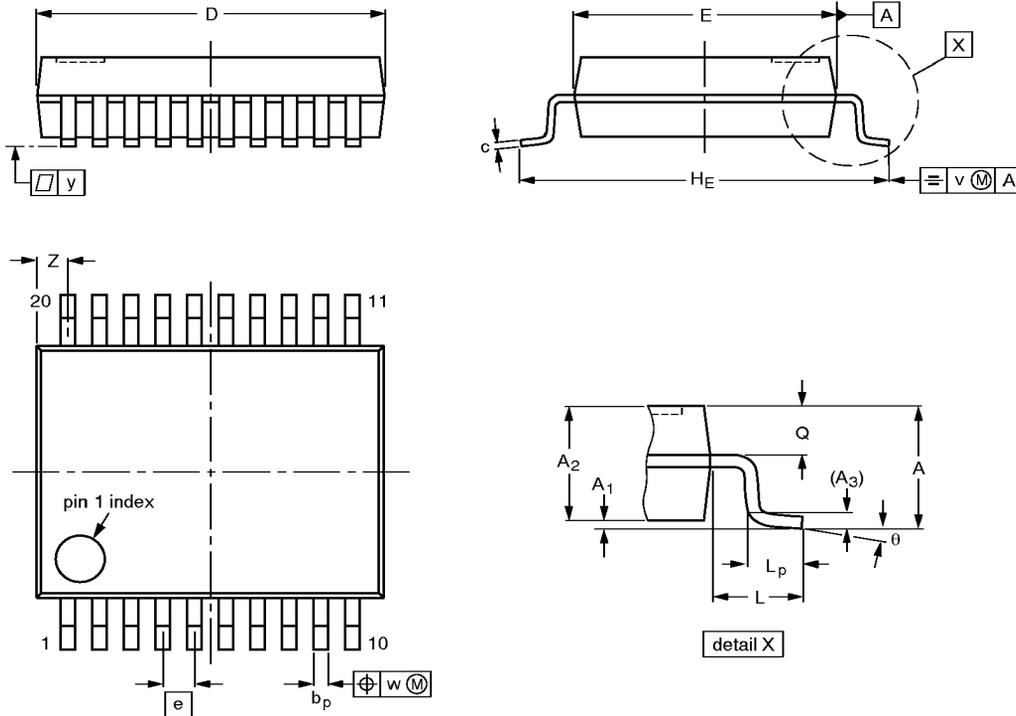
| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|-----------------|------------|----------|------|--|---------------------|----------------------|
| | IEC | JEDEC | EIAJ | | | |
| SOT163-1 | 075E04 | MS-013AC | | | | 95-01-24 97-05-22 |

Octal D-type flip-flop with 5-volt tolerant
 inputs/outputs, positive edge-trigger (3-State)

74LVC374A

SSOP20: plastic shrink small outline package; 20 leads; body width 5.3 mm

SOT339-1



DIMENSIONS (mm are the original dimensions)

| UNIT | A max. | A ₁ | A ₂ | A ₃ | b _p | c | D ⁽¹⁾ | E ⁽¹⁾ | e | H _E | L | L _p | Q | v | w | y | Z ⁽¹⁾ | θ |
|------|--------|----------------|----------------|----------------|----------------|--------------|------------------|------------------|------|----------------|------|----------------|------------|-----|------|-----|------------------|----------|
| mm | 2.0 | 0.21 0.05 | 1.80 1.65 | 0.25 | 0.38 0.25 | 0.20 0.09 | 7.4 7.0 | 5.4 5.2 | 0.65 | 7.9 7.6 | 1.25 | 1.03 0.63 | 0.9 0.7 | 0.2 | 0.13 | 0.1 | 0.9 0.5 | 8° 0° |

Note

1. Plastic or metal protrusions of 0.20 mm maximum per side are not included.

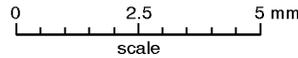
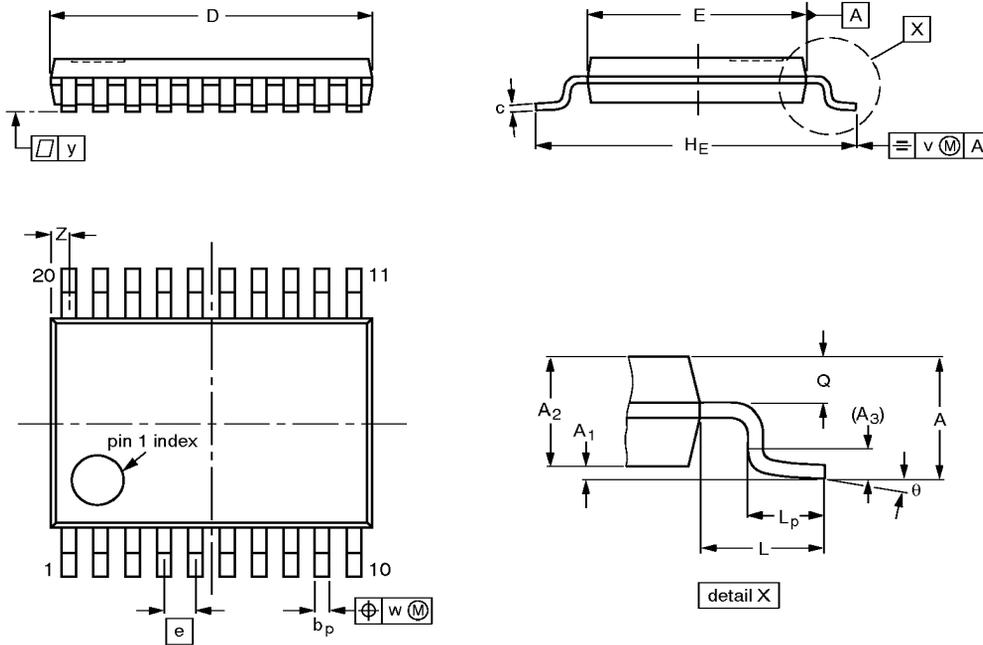
| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|-----------------|------------|----------|------|--|---------------------|----------------------|
| | IEC | JEDEC | EIAJ | | | |
| SOT339-1 | | MO-150AE | | | | 93-09-08 95-02-04 |

Octal D-type flip-flop with 5-volt tolerant
 inputs/outputs, positive edge-trigger
[http://www.icminer.com/Products/74LVC374A](#)

74LVC374A

TSSOP20: plastic thin shrink small outline package; 20 leads; body width 4.4 mm

SOT360-1



DIMENSIONS (mm are the original dimensions)

| UNIT | A max. | A ₁ | A ₂ | A ₃ | b _p | c | D ⁽¹⁾ | E ⁽²⁾ | e | H _E | L | L _p | Q | v | w | y | Z ⁽¹⁾ | θ |
|------|--------|----------------|----------------|----------------|----------------|------------|------------------|------------------|------|----------------|-----|----------------|------------|-----|------|-----|------------------|----------|
| mm | 1.10 | 0.15 0.05 | 0.95 0.80 | 0.25 | 0.30 0.19 | 0.2 0.1 | 6.6 6.4 | 4.5 4.3 | 0.65 | 6.6 6.2 | 1.0 | 0.75 0.50 | 0.4 0.3 | 0.2 | 0.13 | 0.1 | 0.5 0.2 | 8° 0° |

Notes

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.
2. Plastic interlead protrusions of 0.25 mm maximum per side are not included.

| OUTLINE VERSION | REFERENCES | | | | EUROPEAN PROJECTION | ISSUE DATE |
|-----------------|------------|----------|------|--|---------------------|----------------------|
| | IEC | JEDEC | EIAJ | | | |
| SOT360-1 | | MO-153AC | | | | 93-06-16 95-02-04 |