N-Channel NexFET™ Power MOSFETs

Check for Samples: CSD16411Q3

FEATURES

- Ultra Low Qg and Qgd
- Low Thermal Resistance
- Avalanche Rated
- Pb Free Terminal Plating
- RoHS Compliant
- Halogen Free
- SON 3.3mm x 3.3mm Plastic Package

APPLICATIONS

- Point-of-Load Synchronous Buck Converter for Applications in Networking, Telecom and Computing Systems
- Optimized for Control FET Applications

DESCRIPTION

The NexFET™ power MOSFET has been designed to minimize losses in power conversion applications.

PRODUCT SUMMARY

V_{DS}	Drain to Source Voltage	25		V
Q_g	Gate Charge Total (4.5V)	2.9		nC
Q_{gd}	Gate Charge Gate to Drain	0.7		nC
$R_{DS(on)}$	Drain to Source On Resistance	V_{GS} = 4.5V	12	mΩ
		V_{GS} = 10V	8	mΩ
$V_{GS(th)}$	Threshold Voltage	2		V

ORDERING INFORMATION

Device	Package	Media	Qty	Ship
CSD16411Q3	SON 3.3×3.3 Plastic Package	13-inch reel	2500	Tape and Reel

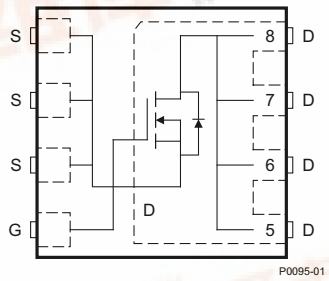
ABSOLUTE MAXIMUM RATINGS

T_A = 25°C unless otherwise stated		VALUE	UNIT
V_{DS}	Drain to Source Voltage	25	V
V_{GS}	Gate to Source Voltage	+16 / –12	V
I_D	Continuous Drain Current, T_C = 25°C	56	A
	Continuous Drain Current(1)	14	A
I_{DM}	Pulsed Drain Current, T_A = 25°C(2)	138	A
P_D	Power Dissipation(1)	2.7	W
T_J, T_{STG}	Operating Junction and Storage Temperature Range	–55 to 150	°C
E_{AS}	Avalanche Energy, single pulse I_D = 18A, L = 0.1mH, R_G = 25Ω	16	mJ

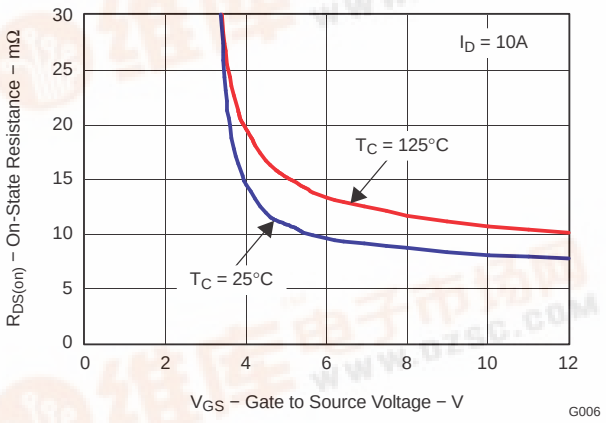
(1) $R_{\theta JA}$ = 47°C/W on 1in^2 Cu (2 oz.) on 0.060" thick FR4 PCB.

(2) Pulse width ≤300μs, duty cycle ≤2%

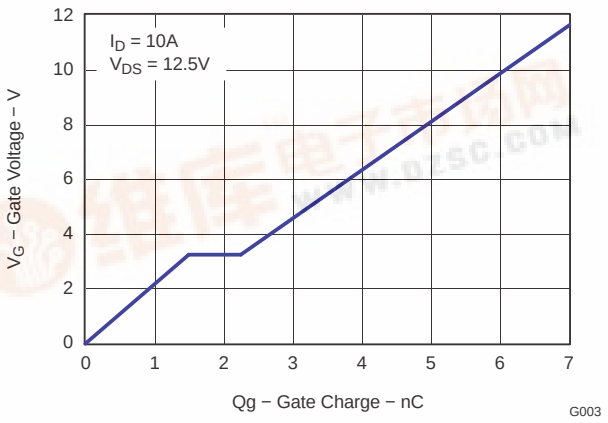
Top View



$R_{DS(ON)}$ vs V_{GS}



Gate Charge



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ELECTRICAL CHARACTERISTICS

(T_A = 25°C unless otherwise stated)

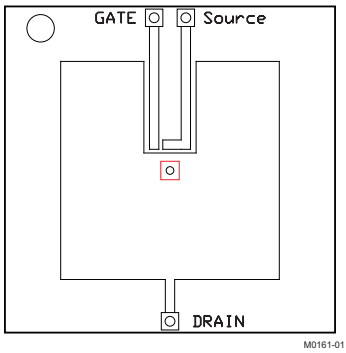
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Static Characteristics						
BV_{DSS}	Drain to Source Voltage	V_{GS} = 0V, I_D = 250μA	25			V
I_{DSS}	Drain to Source Leakage Current	V_{GS} = 0V, V_{DS} = 20V			1	μA
I_{GSS}	Gate to Source Leakage Current	V_{DS} = 0V, V_{GS} = +16 / –12			100	nA
$V_{GS(th)}$	Gate to Source Threshold Voltage	V_{DS} = V_{GS}, I_D = 250μA	1.7	2	2.3	V
$R_{DS(on)}$	Drain to Source On Resistance	V_{GS} = 4.5V, I_D = 10A		12	15	mΩ
		V_{GS} = 10V, I_D = 10A		8	10	mΩ
g_{fs}	Transconductance	V_{DS} = 15V, I_D = 10A		30		S
Dynamic Characteristics						
C_{ISS}	Input Capacitance	V_{GS} = 0V, V_{DS} = 12.5V, f = 1MHz		440	570	pF
C_{OSS}	Output Capacitance			330	430	pF
C_{RSS}	Reverse Transfer Capacitance			33	43	pF
R_g	Series Gate Resistance			0.8	1.6	Ω
Q_g	Gate Charge Total (4.5V)	V_{DS} = 12.5V, I_D = 10A		2.9	3.8	nC
Q_{gd}	Gate Charge Gate to Drain			0.7		nC
Q_{gs}	Gate Charge Gate to Source			1.5		nC
Qg(th)	Gate Charge at Vth			0.9		nC
Q_{OSS}	Output Charge	V_{DS} = 12.5V, V_{GS} = 0V		6.5		nC
$t_{d(on)}$	Turn On Delay Time	V_{DS} = 12.5V, V_{GS} = 4.5V, I_D = 10A R_G = 2Ω		5.3		ns
t_r	Rise Time			7.8		ns
$t_{d(off)}$	Turn Off Delay Time			6		ns
t_f	Fall Time			3.1		ns
Diode Characteristics						
V_{SD}	Diode Forward Voltage	I_S = 10A, V_{GS} = 0V		0.85	1	V
Q_{rr}	Reverse Recovery Charge	V_{DD} = 12.5V, I_F = 10A, di/dt = 300A/μs		11.7		nC
t_{rr}	Reverse Recovery Time	V_{DD} = 12.5V, I_F = 10A, di/dt = 300A/μs		15.5		ns

THERMAL CHARACTERISTICS

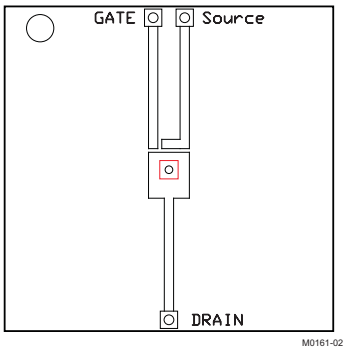
(T_A = 25°C unless otherwise stated)

PARAMETER		MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Thermal Resistance Junction to Case(1)			3.5	°C/W
$R_{\theta JA}$	Thermal Resistance Junction to Ambient(1) (2)			59	°C/W

(1) $R_{\theta JC}$ is determined with the device mounted on a 1 inch square 2 oz. Cu pad on a 1.5 × 1.5 in .060 inch thick FR4 board. $R_{\theta JC}$ is specified by design while $R_{\theta JA}$ is determined by the user's board design.
(2) Device mounted on FR4 Material with 1 $inch^2$ of 2 oz. Cu.



Max $R_{\theta JA}$ = 59°C/W when mounted on 1inch^2 of 2 oz. Cu.



Max $R_{\theta JA}$ = 165°C/W when mounted on minimum pad area of 2 oz. Cu.

TYPICAL MOSFET CHARACTERISTICS

(T_A = 25°C unless otherwise stated)

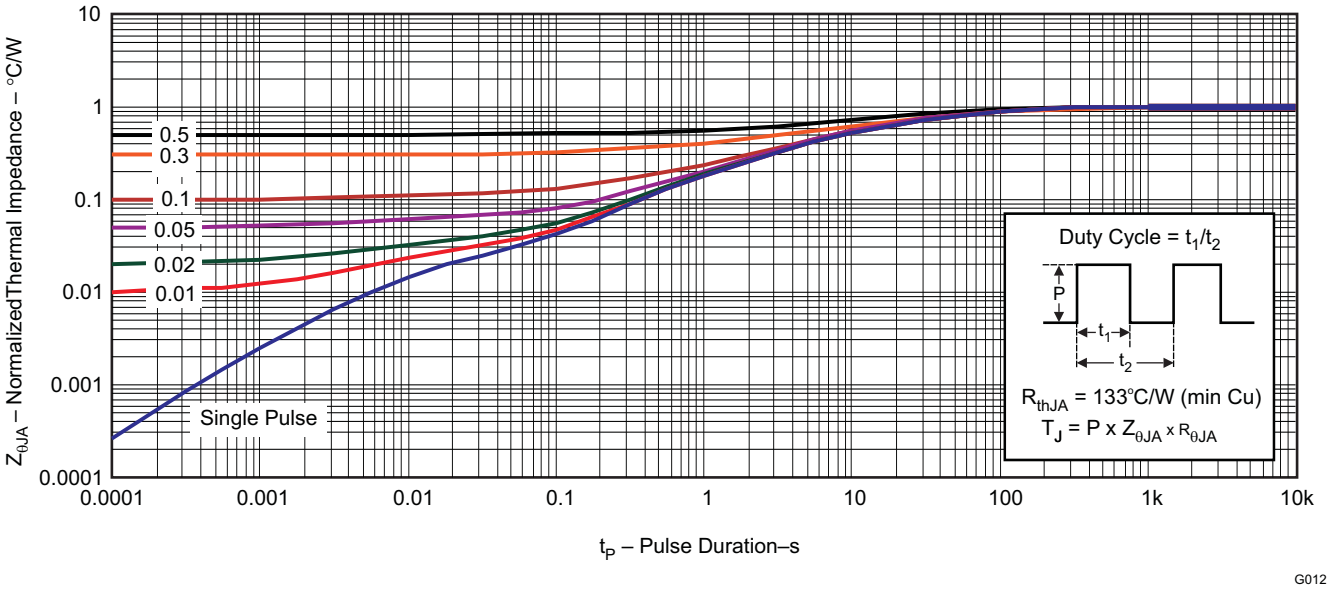


Figure 1. Transient Thermal Impedance

TYPICAL MOSFET CHARACTERISTICS (continued)

(T_A = 25°C unless otherwise stated)

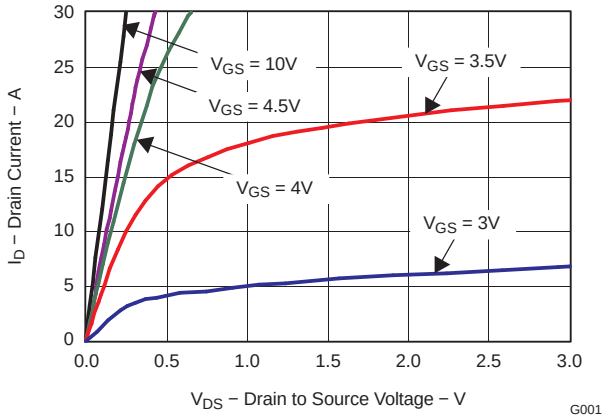


Figure 2. Saturation Characteristics

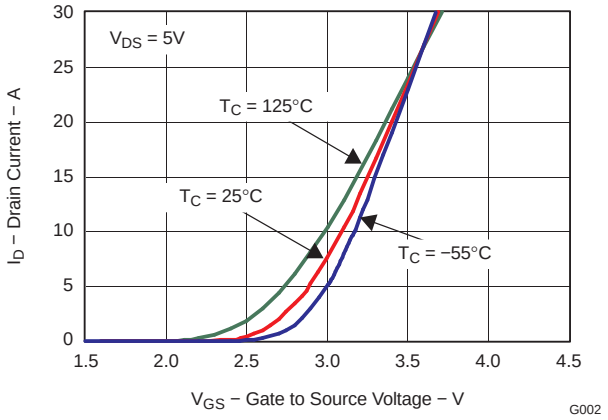


Figure 3. Transfer Characteristics

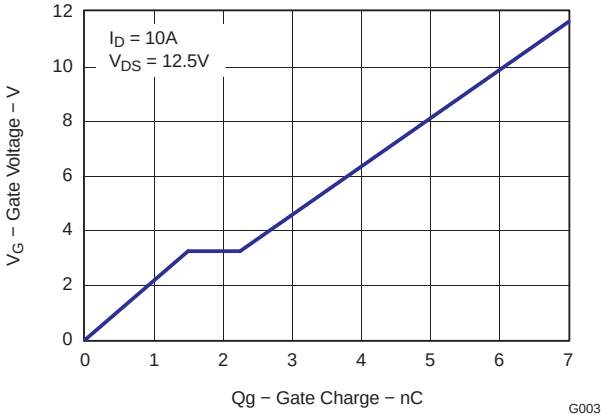


Figure 4. Gate Charge

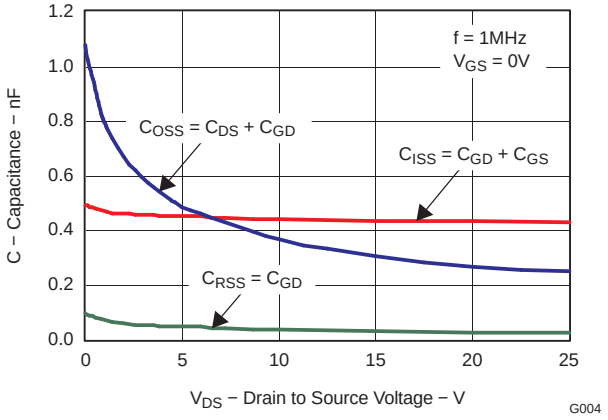


Figure 5. Capacitance

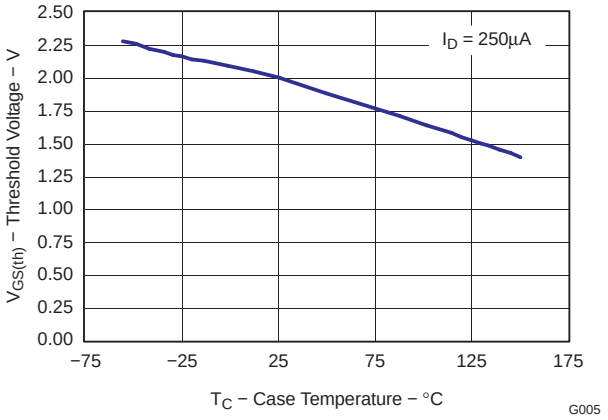


Figure 6. Threshold Voltage vs. Temperature

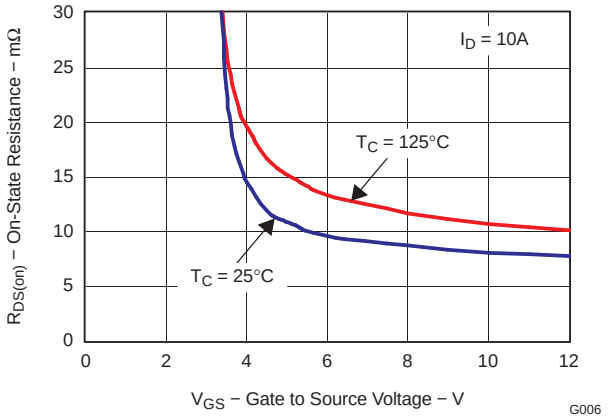


Figure 7. On Resistance vs. Gate Voltage

TYPICAL MOSFET CHARACTERISTICS (continued)

(T_A = 25°C unless otherwise stated)

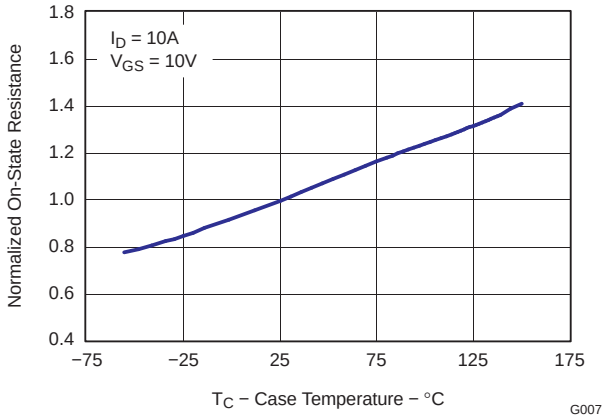


Figure 8. On Resistance vs. Temperature

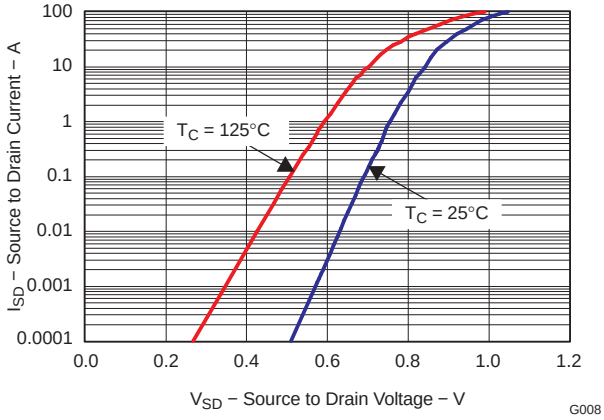


Figure 9. Typical Diode Forward Voltage

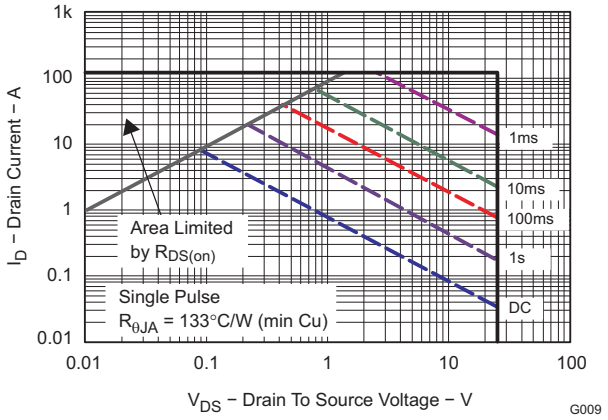


Figure 10. Maximum Safe Operating Area

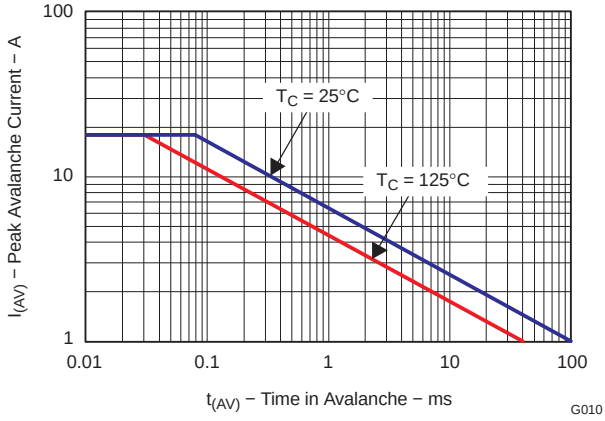


Figure 11. Single Pulse Unclamped Inductive Switching

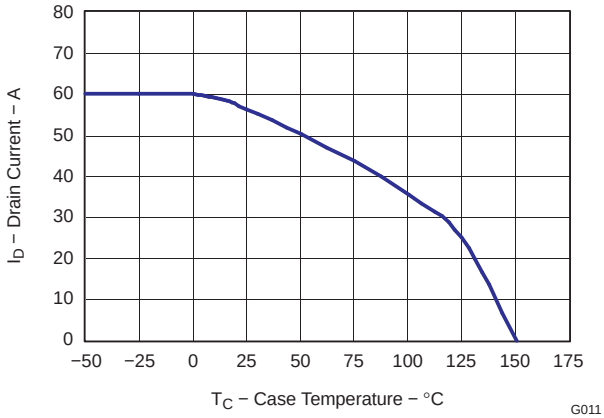
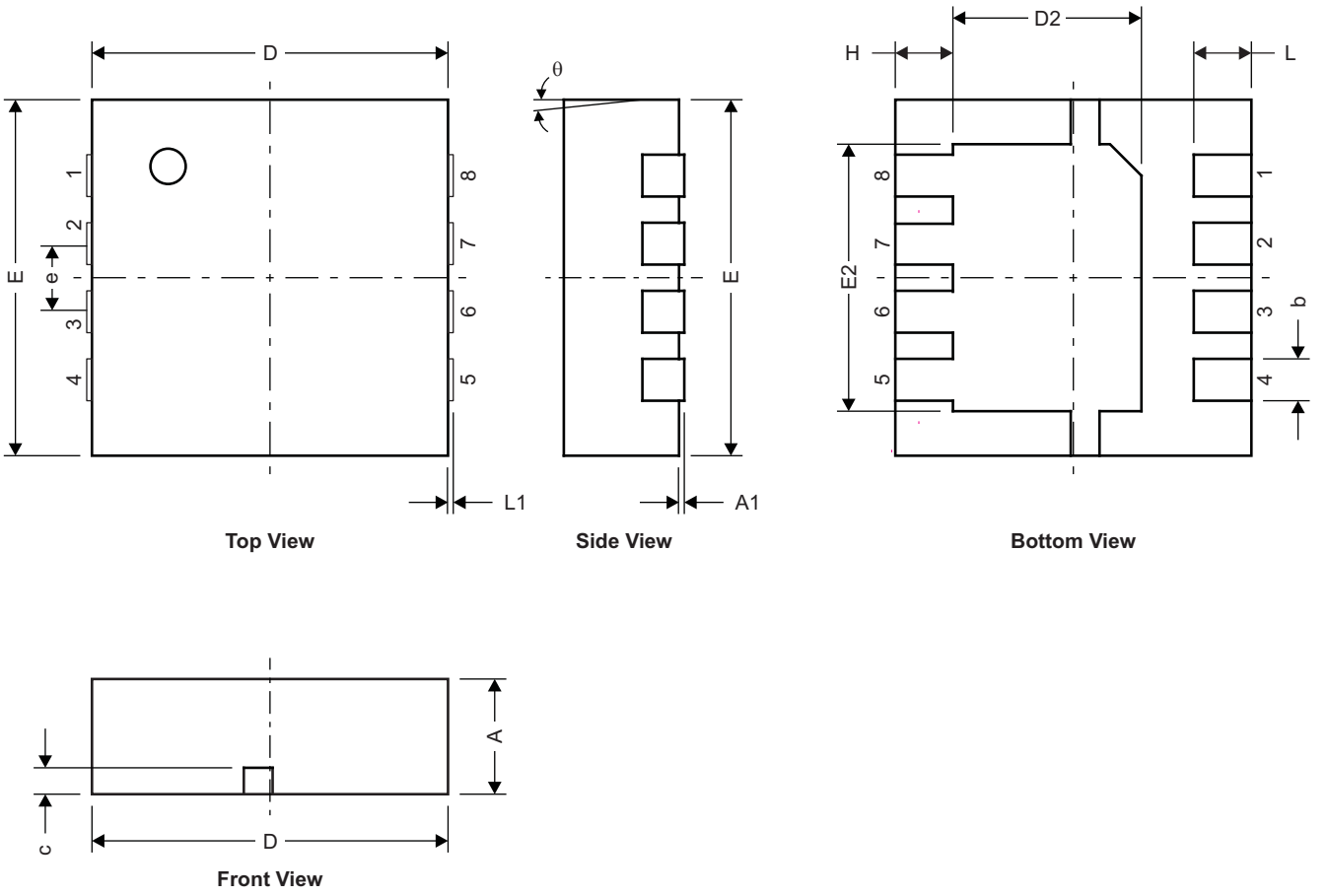


Figure 12. Maximum Drain Current vs. Temperature

MECHANICAL DATA

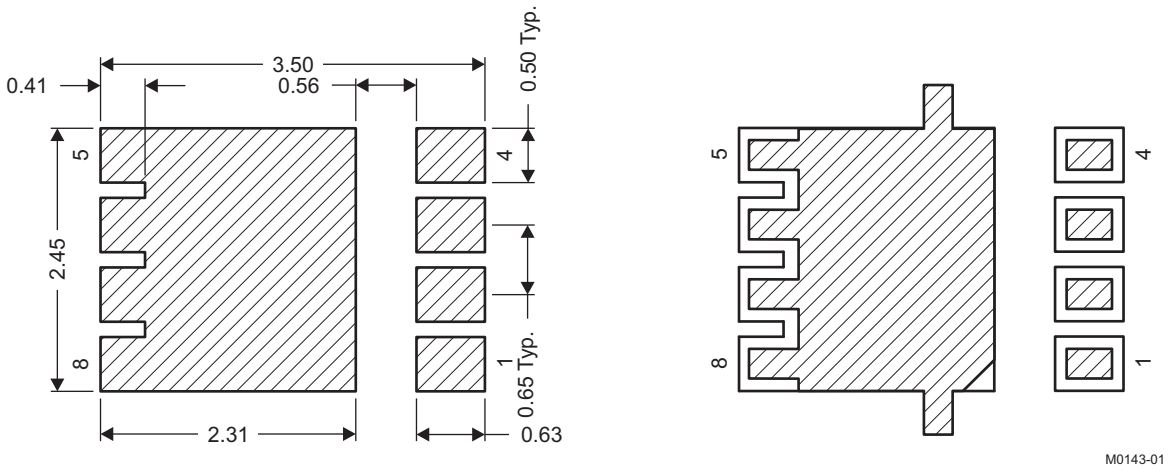
Q3 Package Dimensions



M0142-01

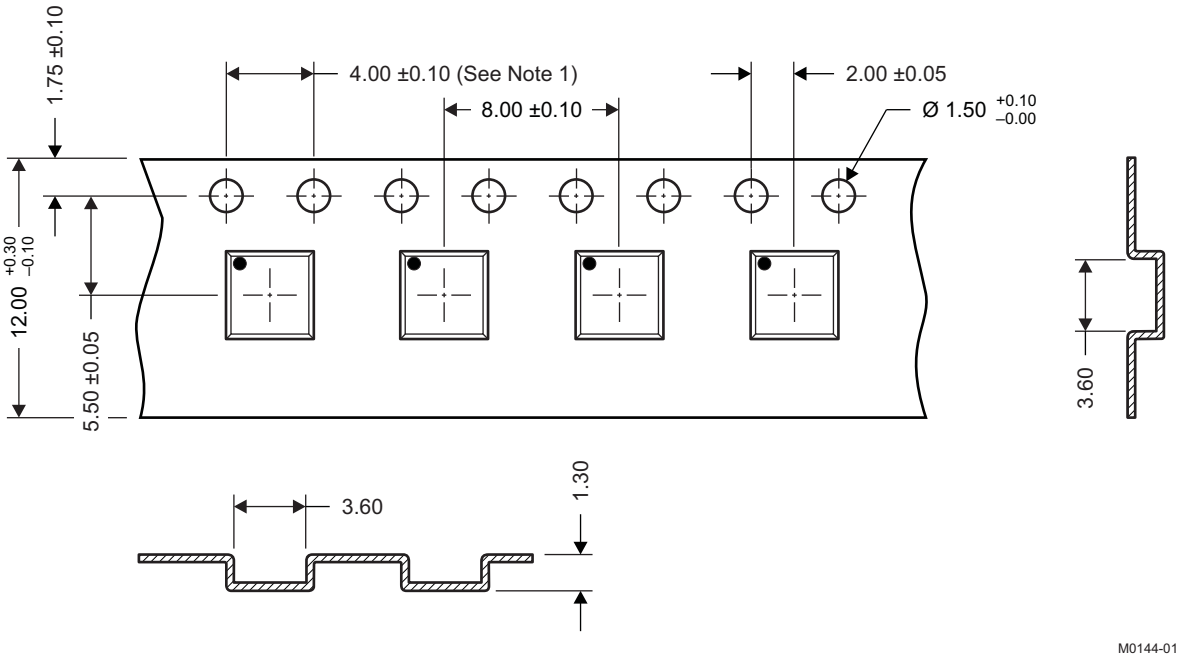
DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.950	1.000	1.100	0.037	0.039	0.043
A1	0.000	0.000	0.050	0.000	0.000	0.002
b	0.280	0.340	0.400	0.011	0.013	0.016
c	0.150	0.200	0.250	0.006	0.008	0.010
D	3.200	3.300	3.400	0.126	0.130	0.134
D1	–	–	–	–	–	–
D2	1.650	1.750	1.800	0.065	0.069	0.071
E	3.200	3.300	3.400	0.126	0.130	0.134
E1	–	–	–	–	–	–
E2	2.350	2.450	2.550	0.093	0.096	0.100
e	0.650 TYP			0.026		
H	0.35	0.450	0.550	0.014	0.018	0.022
L	0.35	0.450	0.550	0.014	0.018	0.022
L1	–	–	–	–	–	–
θ	–	–	–	–	–	–

Recommended PCB Pattern



For recommended circuit layout for PCB designs, see application note SLPA005 – *Reducing Ringing Through PCB Layout Techniques*.

Q3 Tape and Reel Information



Notes:

1. 10 sprocket hole pitch cumulative tolerance ±0.2
2. Camber not to exceed 1mm IN 100mm, noncumulative over 250mm
3. Material:black static dissipative polystyrene
4. All dimensions are in mm (unless otherwise specified)
5. Thickness: 0.30 ±0.05mm
6. MSL1 260°C (IR and Convection) PbF Reflow Compatible

REVISION HISTORY

Changes from Original (August 2009) to Revision A	Page
• the Package Marking Information section	7

www.ti.com

PACKAGING INFORMATION

Orderable Device	Status (1)	Package Type	Package Drawing	Pins	Package Qty	Eco Plan (2)	Lead/ Ball Finish	MSL Pea
CSD16411Q3	ACTIVE	SON	DQG	8	2500	Pb-Free (RoHS Exempt)	CU SN	Level-1-260

(1) The marketing status values are defined as follows:
ACTIVE: Product device recommended for new designs.
LIFEBUY: TI has announced that the device will be discontinued, and a lifetime-buy period is in effect.
NRND: Not recommended for new designs. Device is in production to support existing customers, but TI does not recommend using this part in a new
PREVIEW: Device has been announced but is not in production. Samples may or may not be available.
OBSOLETE: TI has discontinued the production of the device.

(2) Eco Plan - The planned eco-friendly classification: Pb-Free (RoHS), Pb-Free (RoHS Exempt), or Green (RoHS & no Sb/Br) - please check http://www.
information and additional product content details.
TBD: The Pb-Free/Green conversion plan has not been defined.
Pb-Free (RoHS): TI's terms "Lead-Free" or "Pb-Free" mean semiconductor products that are compatible with the current RoHS requirements for all
lead not exceed 0.1% by weight in homogeneous materials. Where designed to be soldered at high temperatures, TI Pb-Free products are suitable fo
Pb-Free (RoHS Exempt): This component has a RoHS exemption for either 1) lead-based flip-chip solder bumps used between the die and package,
the die and leadframe. The component is otherwise considered Pb-Free (RoHS compatible) as defined above.
Green (RoHS & no Sb/Br): TI defines "Green" to mean Pb-Free (RoHS compatible), and free of Bromine (Br) and Antimony (Sb) based flame retard
in homogeneous material)

(3) MSL, Peak Temp. -- The Moisture Sensitivity Level rating according to the JEDEC industry standard classifications, and peak solder temperature.

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Mailing Address: Texas Instruments, Post Office Box 655303, Dallas, Texas 75265