

3.3V 16-bit inverting buffer/driver with 30Ω termination resistors (3-State)

74LVT162240A

FEATURES

- 16-bit bus interface
- 3-State buffers
- Output capability: +12mA/-12mA
- TTL input and output switching levels
- Input and output interface capability to systems at 5V supply
- Bus-hold data inputs eliminate the need for external pull-up resistors to hold unused inputs
- Live insertion/extraction permitted
- Outputs include series resistance of 30Ω making external termination resistors unnecessary
- Power-up 3-State
- No bus current loading when output is tied to 5V bus
- Latch-up protection exceeds 500mA per JEDEC Std 17
- ESD protection exceeds 2000V per MIL STD 883 Method 3015 and 200V per Machine Model
- Same part as 74LVT16240A-1

DESCRIPTION

The 74LVT162240A is a high-performance BiCMOS product designed for V_{CC} operation at 3.3V.

This device is an inverting 16-bit buffer that is ideal for driving bus lines. The device features four Output Enables (1 \overline{OE} , 2 \overline{OE} , 3 \overline{OE} , 4 \overline{OE}), each controlling four of the 3-State outputs.

The 74LVT162240A is designed with 30Ω series resistance in both the pull-up and pull-down output structures. This design reduces line noise in applications such as memory address drivers, clock drivers, and bus receivers/transmitters.

The 74LVT162240A is the same as the 74LVT16240A-1. The part number has been changed to reflect industry standards.

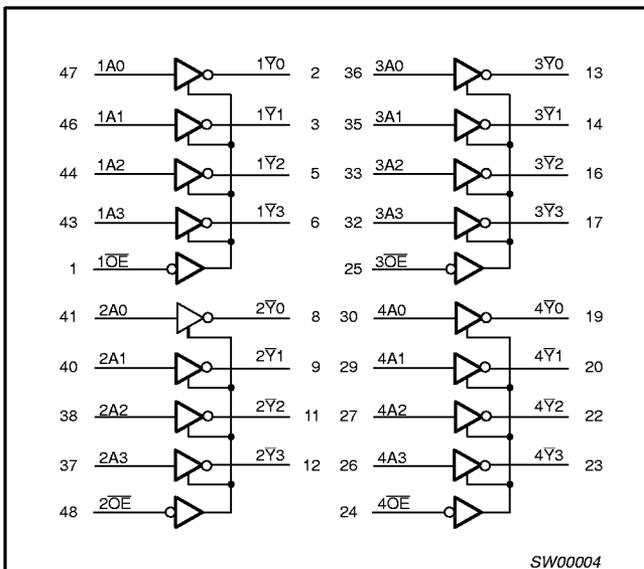
QUICK REFERENCE DATA

SYMBOL	PARAMETER	CONDITIONS T _{amb} = 25°C	TYPICAL	UNIT
t _{PLH} t _{PHL}	Propagation delay nAx to nYx	C _L = 50pF; V _{CC} = 3.3V	2.6	ns
C _{IN}	Input capacitance n \overline{OE}	V _I = 0V or 3.0V	3	pF
C _{OUT}	Output capacitance	V _O = 0V or 3.0V	9	pF
I _{CCZ}	Total supply current	Outputs disabled; V _{CC} = 3.6V	70	μA

ORDERING INFORMATION

PACKAGES	TEMPERATURE RANGE	OUTSIDE NORTH AMERICA	NORTH AMERICA	DWG NUMBER
48-Pin Plastic SSOP Type III	-40°C to +85°C	74LVT162240A DL	VT162240A DL	SOT370-1
48-Pin Plastic TSSOP Type II	-40°C to +85°C	74LVT162240A DGG	VT162240A DGG	SOT362-1

LOGIC SYMBOL



PIN DESCRIPTION

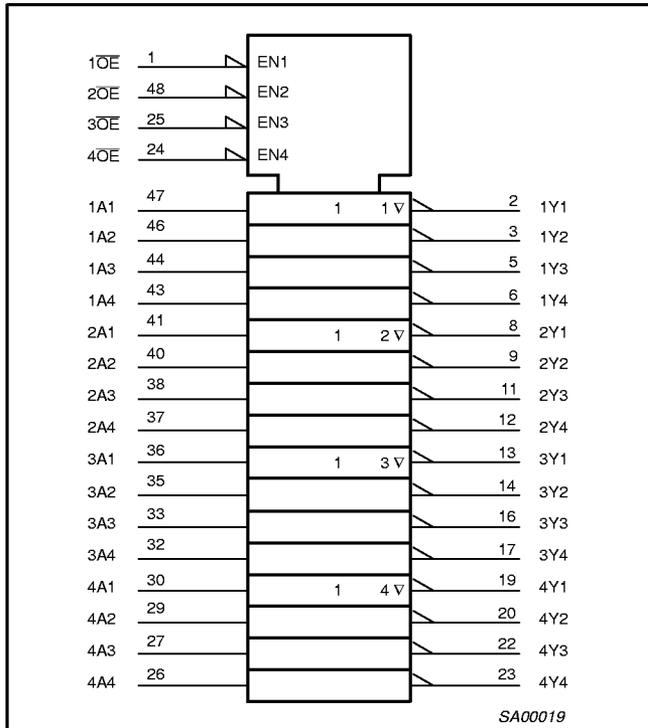
PIN NUMBER	SYMBOL	NAME AND FUNCTION
47, 46, 44, 43, 41, 40, 38, 37, 36, 35, 33, 32, 30, 29, 27, 26	1A0 - 1A3 2A0 - 2A3 3A0 - 3A3 4A0 - 4A3	Data inputs
2, 3, 5, 6, 8, 9, 11, 12, 13, 14, 16, 17, 19, 20, 22, 23	1 \overline{Y} 0 - 1 \overline{Y} 3 2 \overline{Y} 0 - 2 \overline{Y} 3 3 \overline{Y} 0 - 3 \overline{Y} 3 4 \overline{Y} 0 - 4 \overline{Y} 3	Data outputs
1, 48 25, 24	1 \overline{OE} , 2 \overline{OE} , 3 \overline{OE} , 4 \overline{OE}	Output enables
4, 10, 15, 21, 28, 34, 39, 45	GND	Ground (0V)
7, 18, 31, 42	V _{CC}	Positive supply voltage

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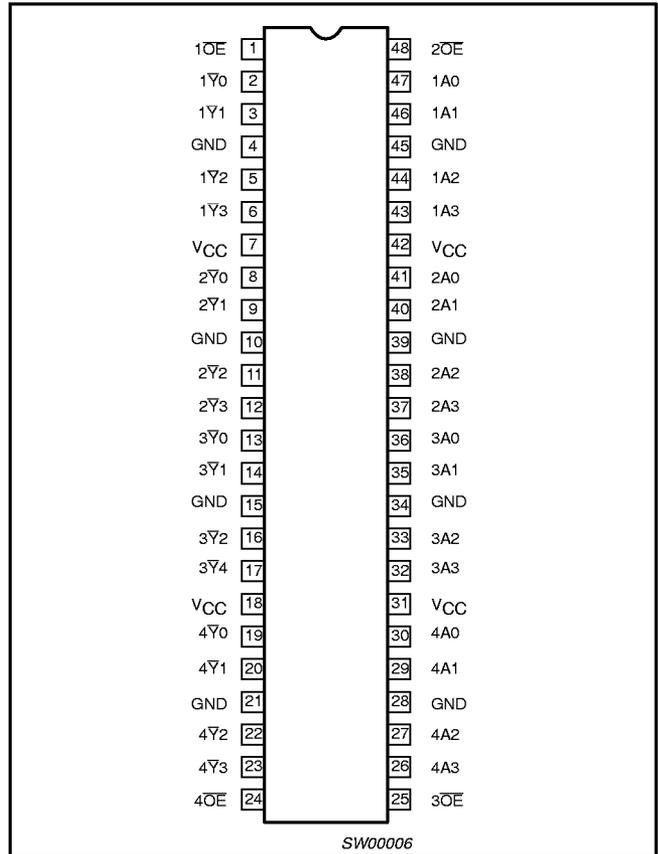
74LVT162240A

[Termination resistors \(3-State\)](#)

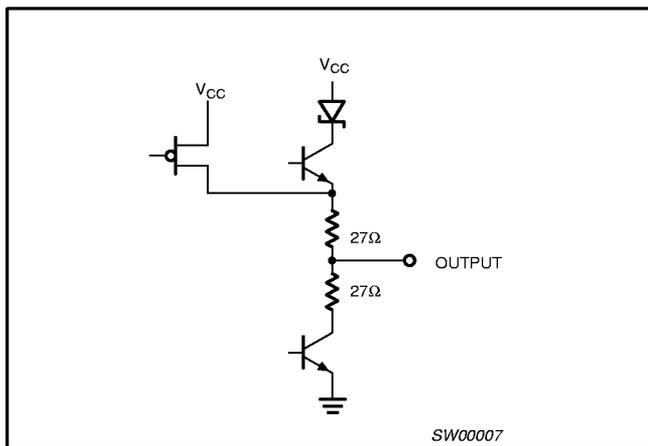
LOGIC SYMBOL (IEEE/IEC)



PIN CONFIGURATION



SCHEMATIC OF EACH OUTPUT



FUNCTION TABLE

INPUTS		OUTPUTS
nOE	nAx	nYx
L	L	H
L	H	L
H	X	Z

H = High voltage level
 L = Low voltage level
 X = Don't care
 Z = High Impedance "off" state

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Termination resistors (0-State)

ABSOLUTE MAXIMUM RATINGS^{1, 2}

SYMBOL	PARAMETER	CONDITIONS	RATING	UNIT
V _{CC}	DC supply voltage		-0.5 to +4.6	V
I _{IK}	DC input diode current	V _I < 0	-50	mA
V _I	DC input voltage ³		-0.5 to +7.0	V
I _{OK}	DC output diode current	V _O < 0	-50	mA
V _{OUT}	DC output voltage ³	Output in Off or High state	-0.5 to +7.0	V
I _{OUT}	DC output current	Output in Low state	128	mA
		Output in High state	-64	
T _{stg}	Storage temperature range		-65 to +150	°C

NOTES:

1. Stresses beyond those listed may cause permanent damage to the device. These are stress ratings only and functional operation of the device at these or any other conditions beyond those indicated under "recommended operating conditions" is not implied. Exposure to absolute-maximum-rated conditions for extended periods may affect device reliability.
2. The performance capability of a high-performance integrated circuit in conjunction with its thermal environment can create junction temperatures which are detrimental to reliability. The maximum junction temperature of this integrated circuit should not exceed 150°C.
3. The input and output negative voltage ratings may be exceeded if the input and output clamp current ratings are observed.

RECOMMENDED OPERATING CONDITIONS

SYMBOL	PARAMETER	LIMITS		UNIT
		MIN	MAX	
V _{CC}	DC supply voltage	2.7	3.6	V
V _I	Input voltage	0	5.5	V
V _{IH}	High-level input voltage	2.0		V
V _{IL}	Input voltage		0.8	V
I _{OH}	High-level output current		-12	mA
I _{OL}	Low-level output current		12	mA
Δt/Δv	Input transition rise or fall rate; Outputs enabled		10	ns/V
T _{amb}	Operating free-air temperature range	-40	+85	°C

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Termination resistors (3-State)

DC ELECTRICAL CHARACTERISTICS

SYMBOL	PARAMETER	TEST CONDITIONS	LIMITS			UNIT	
			Temp = -40°C to +85°C				
			MIN	TYP ¹	MAX		
V _{IK}	Input clamp voltage	V _{CC} = 2.7V; I _{IK} = -18mA		-0.85	1.2	V	
V _{OH}	High-level output voltage	V _{CC} = 3.0V; I _{OH} = -12mA	2.0			V	
V _{OL}	Low-level output voltage	V _{CC} = 3.0V; I _{OL} = 12mA			0.8	V	
I _I	Input leakage current	V _{CC} = 3.6V; V _I = V _{CC} or GND	Control pins		0.1	±1	μA
		V _{CC} = 0 or 3.6V; V _I = 5.5V			0.4	10	
		V _{CC} = 3.6V; V _I = V _{CC}	Data pins ⁴		0.1	1	
		V _{CC} = 3.6V; V _I = 0		-0.4	-5		
I _{OFF}	Output off current	V _{CC} = 0V; V _I or V _O = 0 to 4.5V		0.1	±100	μA	
I _{HOLD}	Bus Hold current A outputs ⁶	V _{CC} = 3V; V _I = 0.8V	75	135		μA	
		V _{CC} = 3V; V _I = 2.0V	-75	-135			
		V _{CC} = 0V to 3.6V; V _{CC} = 3.6V	±500				
I _{EX}	Current into an output in the High state when V _O > V _{CC}	V _O = 5.5V; V _{CC} = 3.0V		50	125	μA	
I _{PU/PD}	Power up/down 3-State output current ³	V _{CC} ≤ 1.2V; V _O = 0.5V to V _{CC} ; V _I = GND or V _{CC} OE/OE = Don't care		1	±100	μA	
I _{OZH}	3-State output High current	V _{CC} = 3.6V; V _O = 3.0V; V _I = V _{IL} or V _{IH}		0.5	5	μA	
I _{OZL}	3-State output Low current	V _{CC} = 3.6V; V _O = 0.5V; V _I = V _{IL} or V _{IH}		0.5	-5	μA	
I _{CCH}	Quiescent supply current	V _{CC} = 3.6V; Outputs High, V _I = GND or V _{CC} , I _O = 0		0.07	0.12	mA	
I _{CCL}		V _{CC} = 3.6V; Outputs Low, V _I = GND or V _{CC} , I _O = 0		4.0	6		
I _{CCZ}		V _{CC} = 3.6V; Outputs Disabled; V _I = GND or V _{CC} , I _O = 0 ⁵		0.07	0.12		
ΔI _{CC}	Additional supply current per input pin ²	V _{CC} = 3V to 3.6V; One input at V _{CC} -0.6V, Other inputs at V _{CC} or GND		0.1	0.20	mA	

NOTES:

- All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.
- This is the increase in supply current for each input at the specified voltage level other than V_{CC} or GND
- This parameter is valid for any V_{CC} between 0V and 1.2V with a transition time of up to 10msec. From V_{CC} = 1.2V to V_{CC} = 3.3V ± 0.3V a transition time of 100μsec is permitted. This parameter is valid for T_{amb} = 25°C only.
- Unused pins at V_{CC} or GND.
- I_{CCZ} is measured with outputs pulled to V_{CC} or GND.
- This is the bus hold overdrive current required to force the input to the opposite logic state.

AC CHARACTERISTICS

GND = 0V; t_R = t_F = 2.5ns; C_L = 50pF; R_L = 500Ω; T_{amb} = -40°C to +85°C.

SYMBOL	PARAMETER	WAVEFORM	LIMITS				UNIT
			V _{CC} = 3.3V ± 0.3V			V _{CC} = 2.7V	
			MIN	TYP ¹	MAX	MAX	
t _{PLH} t _{PHL}	Propagation delay nAx to nYx	1	0.5 0.5	2.6 2.6	4.2 4.2	5.0 5.0	ns
t _{PZH} t _{PZL}	Output enable time to High and Low level	2	1.0 1.0	3.3 3.0	5.5 5.0	6.5 5.5	ns
t _{PHZ} t _{PLZ}	Output disable time from High and Low Level	2	1.0 1.0	3.5 3.2	5.0 4.5	5.5 4.5	ns

NOTE:

- All typical values are at V_{CC} = 3.3V and T_{amb} = 25°C.

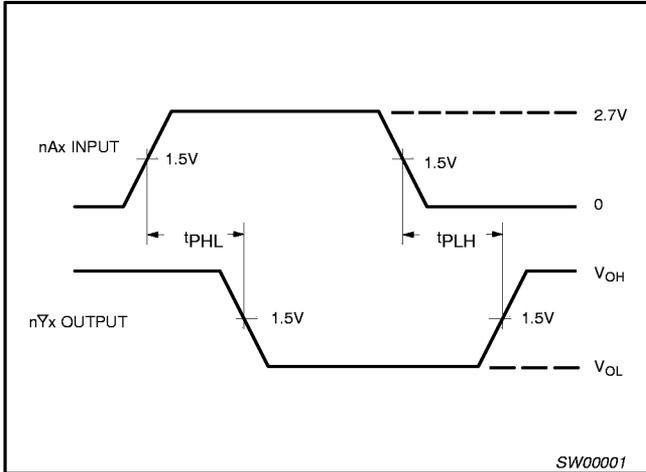
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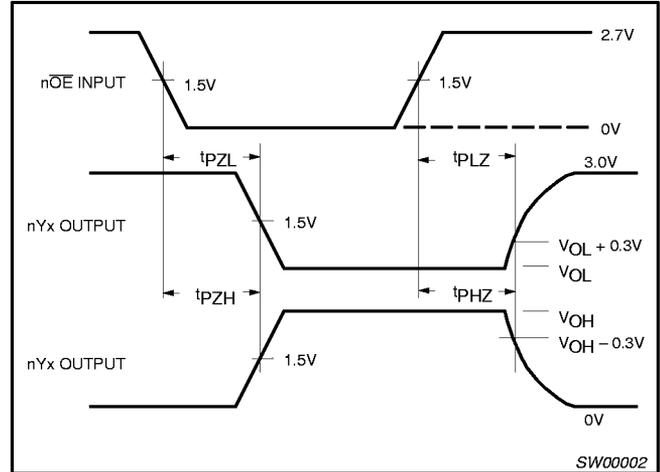
Termination resistors (3-State)

AC WAVEFORMS

$V_M = 1.5V, V_{IN} = GND \text{ to } 2.7V$



Waveform 1. Input (nAx) to Output (nYx) Propagation Delays



Waveform 2. 3-State Output Enable and Disable Times

TEST CIRCUIT AND WAVEFORMS

Test Circuit for 3-State Outputs

SWITCH POSITION

TEST	SWITCH
t_{PHZ}/t_{PZH}	GND
t_{PLZ}/t_{PZL}	6V
t_{PLH}/t_{PHL}	open

DEFINITIONS

R_L = Load resistor; see AC CHARACTERISTICS for value.

C_L = Load capacitance includes jig and probe capacitance; see AC CHARACTERISTICS for value.

R_T = Termination resistance should be equal to Z_{OUT} of pulse generators.

**$V_M = 1.5V$
Input Pulse Definition**

FAMILY	INPUT PULSE REQUIREMENTS				
	Amplitude	Rep. Rate	t_W	t_R	t_F
74LVT16	2.7V	$\leq 10\text{MHz}$	500ns	$\leq 2.5\text{ns}$	$\leq 2.5\text{ns}$

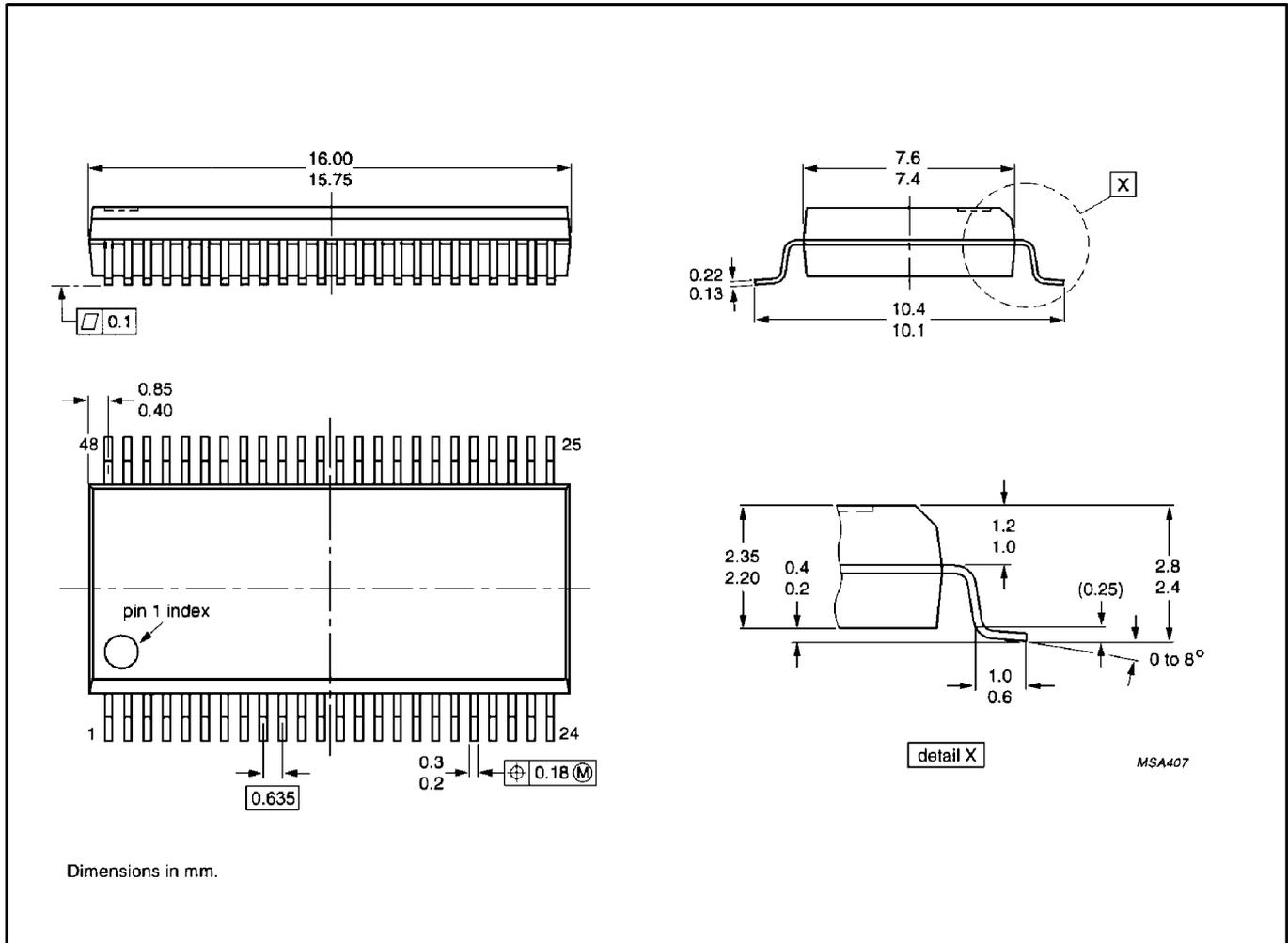
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3.3V LVT 16-bit inverting buffer/driver with 30Ω termination resistors (0-State)

74LVT162240A

SSOP48: plastic shrink small outline package; 48 leads; body width 7.5mm

SOT370-1



3.3V LVT 16-bit inverting buffer/driver with 30Ω termination resistors (0-State)

74LVT162240A

TSSOP48: plastic thin shrink small outline package; 48 leads; body width 6.1mm

SOT362-1

