

30V N-Channel NexFET™ Power MOSFETs

Check for Samples: [CSD17309Q3](#)

FEATURES

- Optimized for 5V Gate Drive
- Ultra Low Q_g and Q_{gd}
- Low Thermal Resistance
- Avalanche Rated
- Pb Free Terminal Plating
- RoHS Compliant
- Halogen Free
- SON 3.3-mm x 3.3-mm Plastic Package

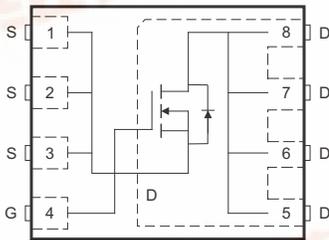
APPLICATIONS

- Notebook Point of Load
- Point-of-Load Synchronous Buck in Networking, Telecom, and Computing Systems

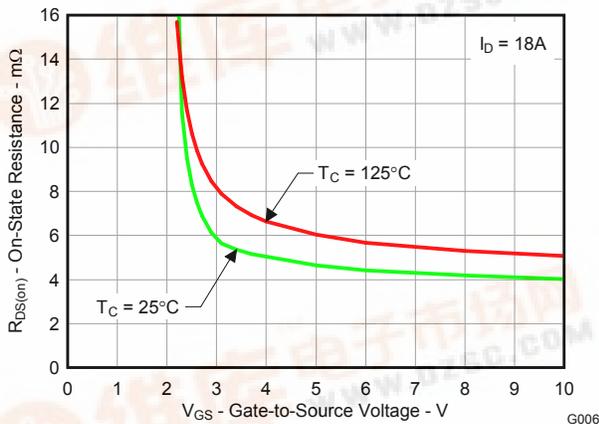
DESCRIPTION

The NexFET™ power MOSFET has been designed to minimize losses in power conversion applications and optimized for 5V gate drive applications.

Top View



$R_{DS(on)}$ vs V_{GS}



PRODUCT SUMMARY

V_{DS}	Drain to Source Voltage	30	V
Q_g	Gate Charge Total (4.5V)	7.5	nC
Q_{gd}	Gate Charge Gate to Drain	1.7	nC
$R_{DS(on)}$	Drain to Source On Resistance	$V_{GS} = 3V$	6.3 mΩ
		$V_{GS} = 4.5V$	4.9 mΩ
		$V_{GS} = 8V$	4.2 mΩ
$V_{GS(th)}$	Threshold Voltage	1.2	V

ORDERING INFORMATION

Device	Package	Media	Qty	Ship
CSD17309Q3	SON 3.3-mm x 3.3-mm Plastic Package	13-Inch Reel	2500	Tape and Reel

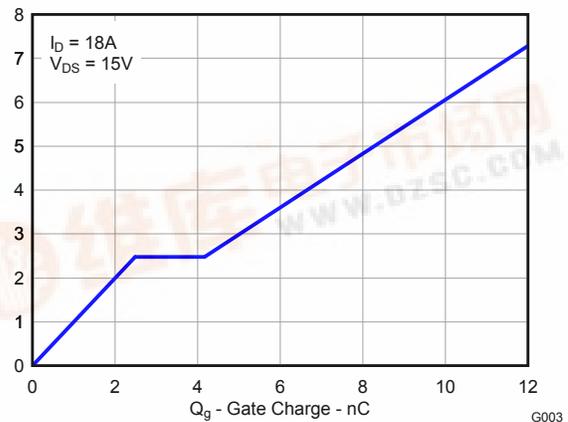
ABSOLUTE MAXIMUM RATINGS

$T_A = 25^\circ\text{C}$ unless otherwise stated		VALUE	UNIT
V_{DS}	Drain to Source Voltage	30	V
V_{GS}	Gate to Source Voltage	+10 / -8	V
I_D	Continuous Drain Current, $T_C = 25^\circ\text{C}$	60	A
	Continuous Drain Current ⁽¹⁾	20	A
I_{DM}	Pulsed Drain Current, $T_A = 25^\circ\text{C}$ ⁽²⁾	112	A
P_D	Power Dissipation ⁽¹⁾	2.8	W
T_J, T_{STG}	Operating Junction and Storage Temperature Range	-55 to 150	$^\circ\text{C}$
E_{AS}	Avalanche Energy, Single Pulse $I_D = 57A, L = 0.1\text{mH}, R_G = 25\Omega$	162	mJ

(1) Typical $R_{\theta JA} = 45^\circ\text{C/W}$ when mounted on a 1-inch² (6.45-cm²), 2-oz. (0.071-mm thick) Cu pad on a 0.06-inch (1.52-mm) thick FR4 PCB.

(2) Pulse duration $\leq 300\mu\text{s}$, duty cycle $\leq 2\%$

GATE CHARGE



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PRODUCTION DATA information is current as of publication date. Products conform to specifications per the terms of the Texas Instruments standard warranty. Production processing does not necessarily include testing of all parameters.

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These devices have limited built-in ESD protection. The leads should be shorted together or the device placed in conductive foam during storage or handling to prevent electrostatic damage to the MOS gates.

ELECTRICAL CHARACTERISTICS

($T_A = 25^\circ\text{C}$ unless otherwise stated)

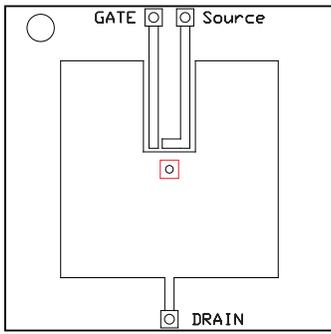
PARAMETER		TEST CONDITIONS	MIN	TYP	MAX	UNIT
Static Characteristics						
BV_{DSS}	Drain to Source Voltage	$V_{GS} = 0V, I_D = 250\mu A$	30			V
I_{DSS}	Drain to Source Leakage Current	$V_{GS} = 0V, V_{DS} = 24V$			1	μA
I_{GSS}	Gate to Source Leakage Current	$V_{DS} = 0V, V_{GS} = +10 / -8V$			100	nA
$V_{GS(th)}$	Gate to Source Threshold Voltage	$V_{DS} = V_{GS}, I_D = 250\mu A$	0.9	1.2	1.7	V
$R_{DS(on)}$	Drain to Source On Resistance	$V_{GS} = 3.0V, I_D = 18A$		6.3	8.5	m Ω
		$V_{GS} = 4.5V, I_D = 18A$		4.9	6.3	m Ω
		$V_{GS} = 8V, I_D = 18A$		4.2	5.4	m Ω
g_{fs}	Transconductance	$V_{DS} = 15V, I_D = 18A$		67		S
Dynamic Characteristics						
C_{ISS}	Input Capacitance	$V_{GS} = 0V, V_{DS} = 15V,$ $f = 1MHz$		1150	1440	pF
C_{OSS}	Output Capacitance			580	750	pF
C_{RSS}	Reverse Transfer Capacitance			43	56	pF
R_g	Series Gate Resistance			1.2	2.4	Ω
Q_g	Gate Charge Total (4.5V)	$V_{DS} = 15V, I_D = 18A$		7.5	10	nC
Q_{gd}	Gate Charge Gate to Drain			1.7		nC
Q_{gs}	Gate Charge Gate to Source			2.5		nC
$Q_{g(th)}$	Gate Charge at V_{th}			1.3		nC
Q_{OSS}	Output Charge	$V_{DS} = 13V, V_{GS} = 0V$		15		nC
$t_{d(on)}$	Turn On Delay Time	$V_{DS} = 15V, V_{GS} = 4.5V,$ $I_D = 18A, R_G = 2\Omega$		6.1		ns
t_r	Rise Time			9.9		ns
$t_{d(off)}$	Turn Off Delay Time			13.2		ns
t_f	Fall Time			3.6		ns
Diode Characteristics						
V_{SD}	Diode Forward Voltage	$I_{DS} = 18A, V_{GS} = 0V$		0.85	1	V
Q_{rr}	Reverse Recovery Charge	$V_{DD} = 13V, I_F = 18A,$ $di/dt = 300A/\mu s$		30		nC
t_{rr}	Reverse Recovery Time			23		ns

THERMAL CHARACTERISTICS

($T_A = 25^\circ\text{C}$ unless otherwise stated)

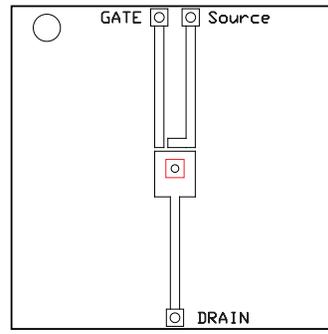
PARAMETER		MIN	TYP	MAX	UNIT
$R_{\theta JC}$	Thermal Resistance Junction to Case ⁽¹⁾			2	$^\circ\text{C/W}$
$R_{\theta JA}$	Thermal Resistance Junction to Ambient ⁽¹⁾⁽²⁾			57	$^\circ\text{C/W}$

- (1) $R_{\theta JC}$ is determined with the device mounted on a 1-inch² (6.45-cm²), Cu pad on a 1.5-inch x 1.5-inch thick FR4 PCB. $R_{\theta JC}$ is specified by design, whereas $R_{\theta JA}$ is determined by the user's board design.
- (2) Device mounted on FR4 material with 1-inch² 2-oz.Cu.



Max $R_{\theta JA} = 57^{\circ}\text{C/W}$
when mounted on
1 inch² (6.45 cm²) of
2-oz. (0.071-mm thick)
Cu.

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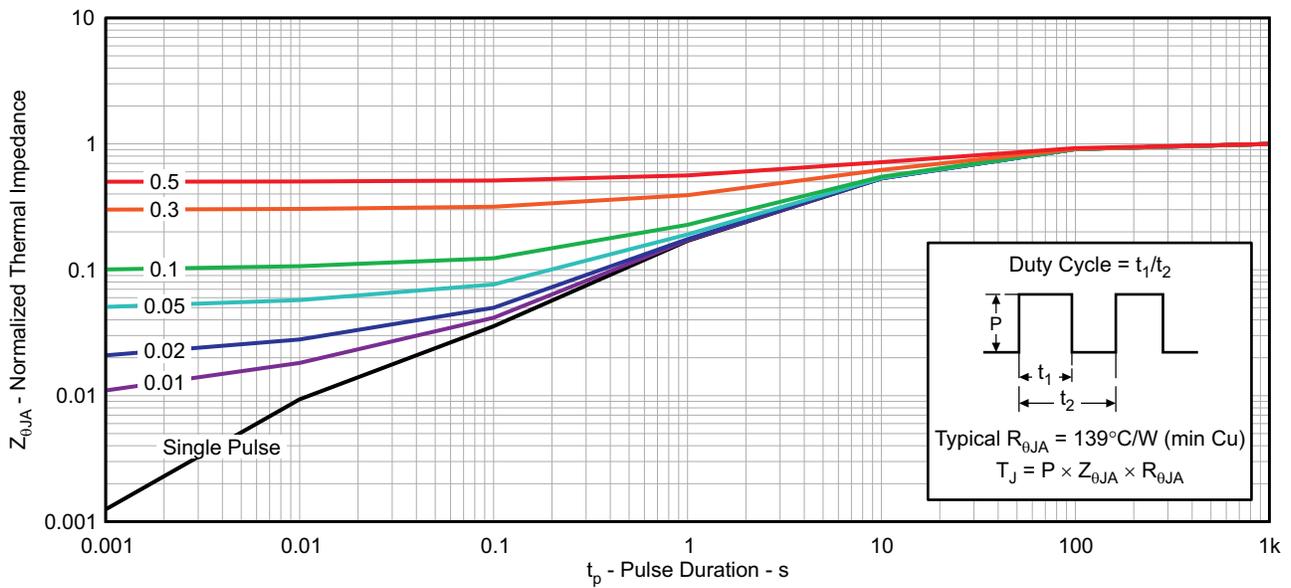


Max $R_{\theta JA} = 174^{\circ}\text{C/W}$
when mounted on a
minimum pad area of
2-oz. (0.071-mm thick)
Cu.

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TYPICAL MOSFET CHARACTERISTICS

($T_A = 25^{\circ}\text{C}$ unless otherwise stated)



G012

Figure 1. Transient Thermal Impedance

TYPICAL MOSFET CHARACTERISTICS (continued)

($T_A = 25^\circ\text{C}$ unless otherwise stated)

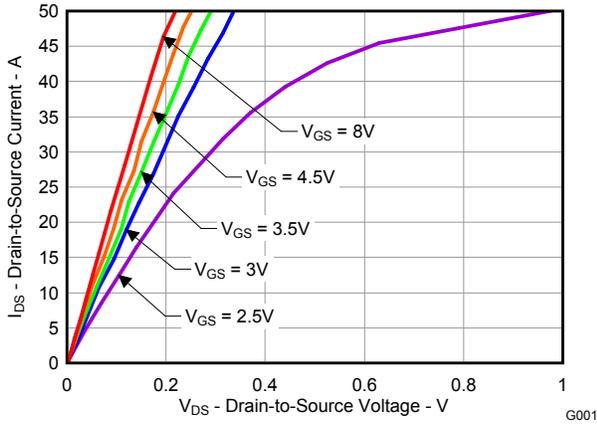


Figure 2. Saturation Characteristics

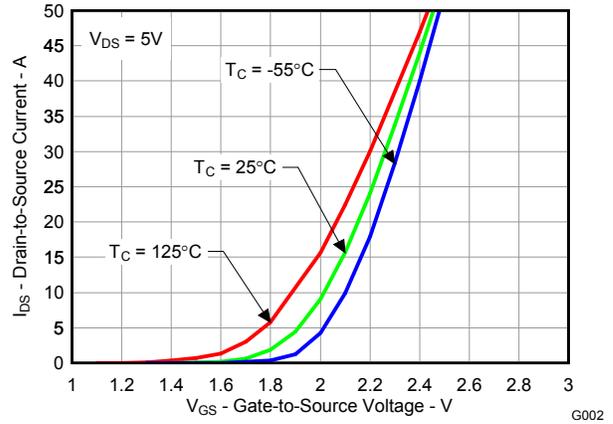


Figure 3. Transfer Characteristics

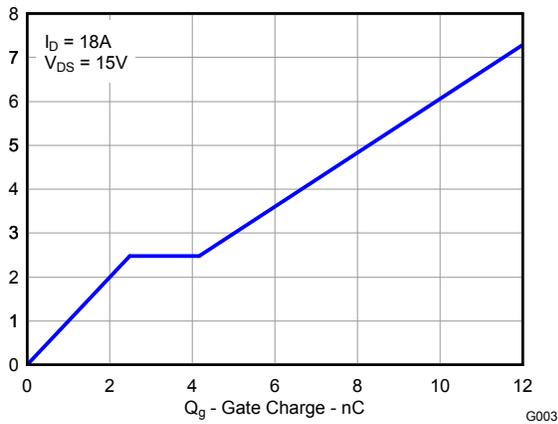


Figure 4. Gate Charge

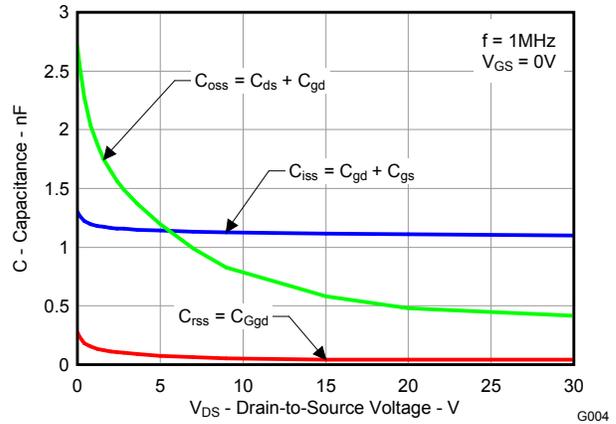


Figure 5. Capacitance

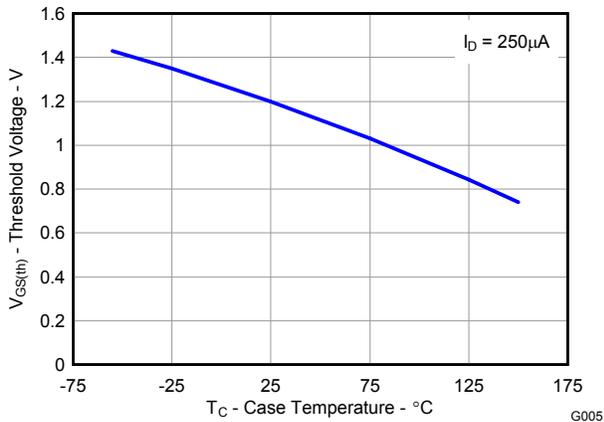


Figure 6. Threshold Voltage vs. Temperature

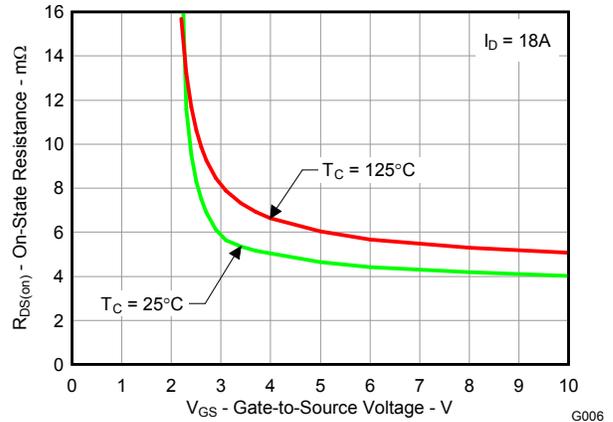


Figure 7. On-State Resistance vs. Gate-to-Source Voltage

TYPICAL MOSFET CHARACTERISTICS (continued)

($T_A = 25^\circ\text{C}$ unless otherwise stated)

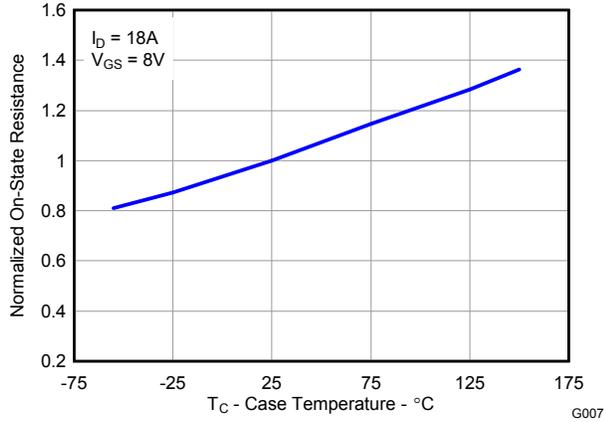


Figure 8. Normalized On-State Resistance vs. Temperature

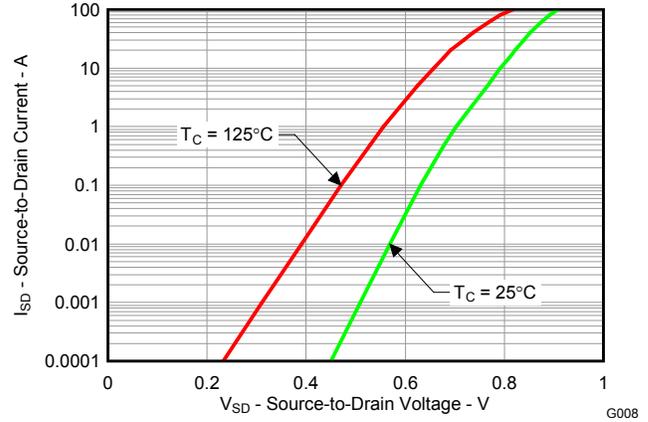


Figure 9. Typical Diode Forward Voltage

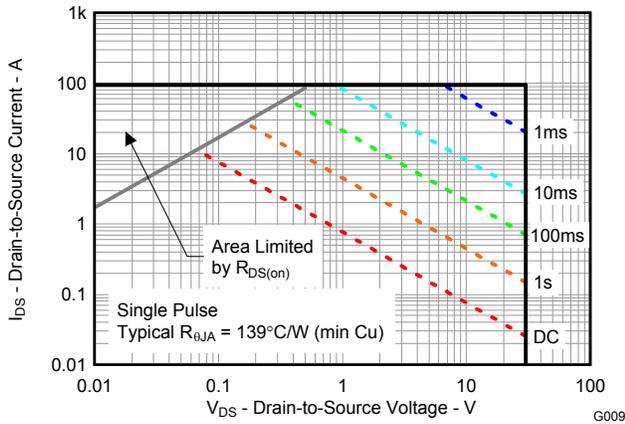


Figure 10. Maximum Safe Operating Area

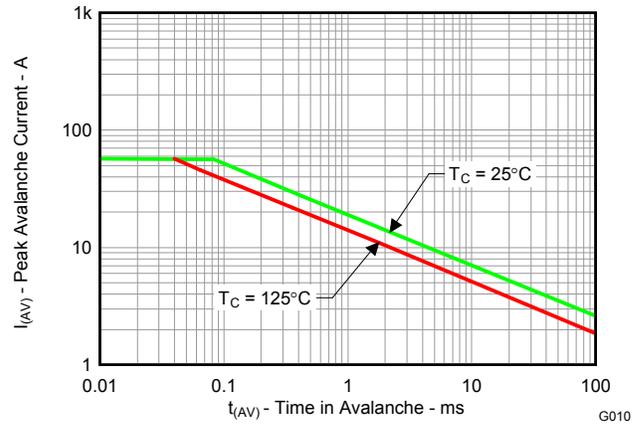


Figure 11. Single Pulse Unclamped Inductive Switching

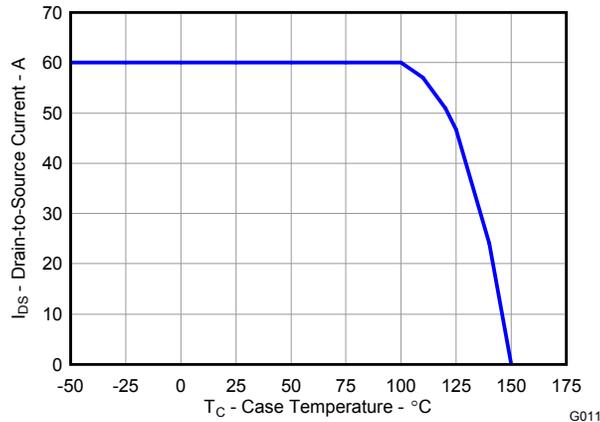
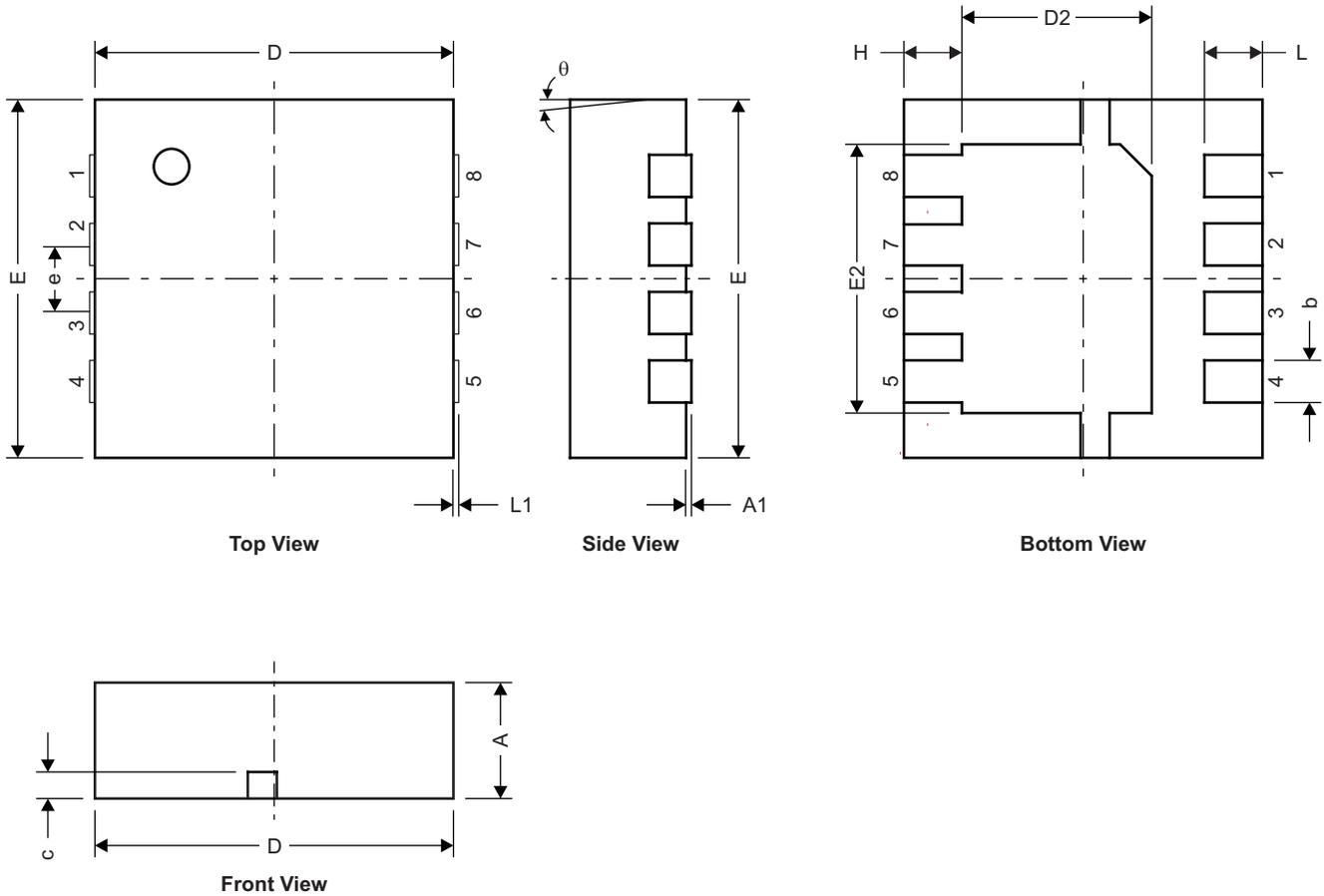


Figure 12. Maximum Drain Current vs. Temperature

MECHANICAL DATA

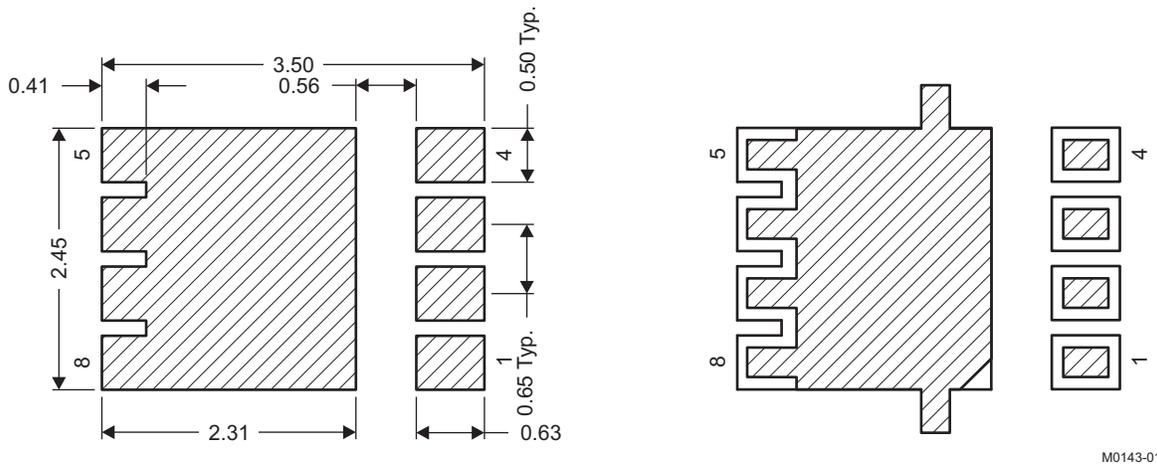
Q3 Package Dimensions



M0142-01

DIM	MILLIMETERS			INCHES		
	MIN	NOM	MAX	MIN	NOM	MAX
A	0.950	1.000	1.100	0.037	0.039	0.043
A1	0.000	0.000	0.050	0.000	0.000	0.002
b	0.280	0.340	0.400	0.011	0.013	0.016
c	0.150	0.200	0.250	0.006	0.008	0.010
D	3.200	3.300	3.400	0.126	0.130	0.134
D1	-	-	-	-	-	-
D2	1.650	1.750	1.800	0.065	0.069	0.071
E	3.200	3.300	3.400	0.126	0.130	0.134
E1	-	-	-	-	-	-
E2	2.350	2.450	2.550	0.093	0.096	0.100
e	0.650 TYP			0.026		
H	0.35	0.450	0.550	0.014	0.018	0.022
L	0.35	0.450	0.550	0.014	0.018	0.022
L1	-	-	-	-	-	-
θ	-	-	-	-	-	-

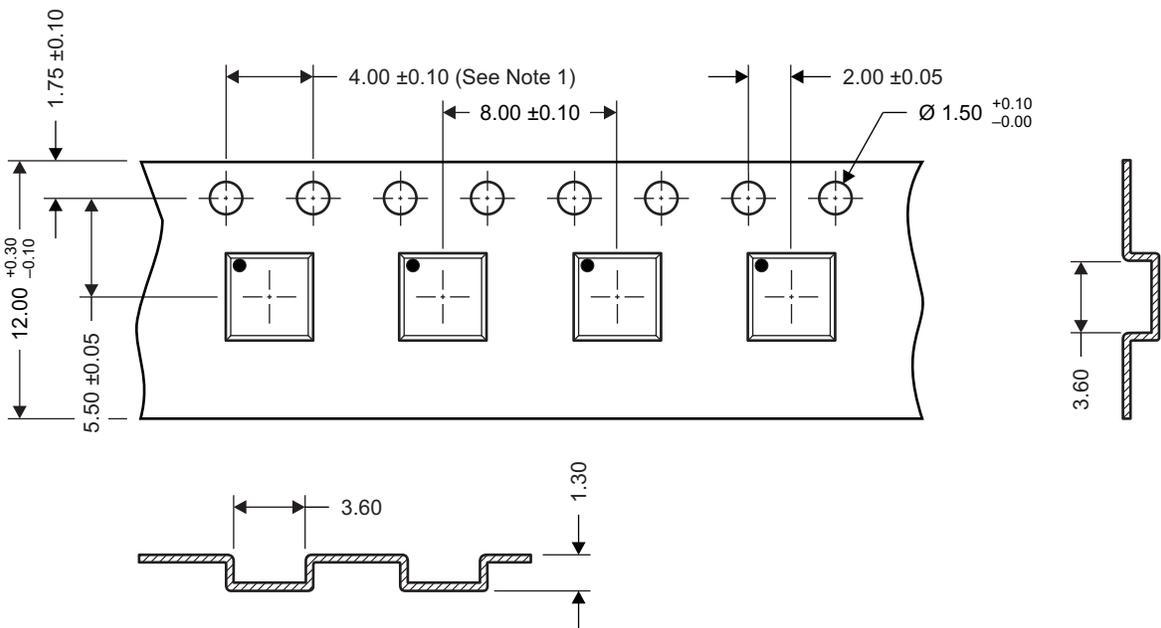
Recommended PCB Pattern



M0143-01

For recommended circuit layout for PCB designs, see application note [SLPA005 – Reducing Ringing Through PCB Layout Techniques](#).

Q3 Tape and Reel Information



M0144-01

- Notes:
1. 10-sprocket hole-pitch cumulative tolerance ± 0.2
 2. Camber not to exceed 1mm in 100mm, noncumulative over 250mm
 3. Material: black static-dissipative polystyrene
 4. All dimensions are in mm, unless otherwise specified.
 5. Thickness: 0.30 ± 0.05 mm
 6. MSL1 260°C (IR and convection) PbF reflow compatible

[查询 CSD17309Q3 价格](#)

REVISION HISTORY

Changes from Original (March 2010) to Revision A	Page
• Deleted the Package Marking Information section	7

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